AH322

2W High Linearity InGaP HBT Amplifier

Product Features

- 400 – 2700 MHz
- +33 dBm P1dB
- +50 dBm Output IP3
- 13.4 dB Gain @ 2140 MHz
- 500 mA Quiescent Current
- +5 V Single Supply
- MTTF > 100 Years
- Lead-free/RoHS-compliant SOIC-8 Package

Applications

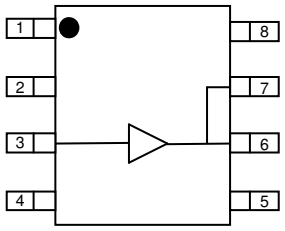
- Final stage amplifiers for Repeaters
- High Power Amplifiers
- Mobile Infrastructure
- LTE / WCDMA / EDGE / CDMA

Product Description

The AH322 is a high dynamic range driver amplifier in a low-cost surface mount package. The InGaP/GaAs HBT is able to achieve high performance for various narrowband-tuned application circuits with up to +50 OIP3 and +33 dBm of compressed 1dB power. It is housed in a lead-free/RoHS-compliant SOIC-8 package. All devices are 100% RF and DC tested.

The AH322 is targeted for use as a driver amplifier in wireless infrastructure where high linearity and medium power is required. The AH322 is ideal for the final stage of small repeaters or as driver stages for high power amplifiers. In addition, the amplifier can be used for a wide variety of other applications within the 400 to 2700 MHz frequency band.

Functional Diagram



Function	Pin No.
Iref	8
Input	3
Output / Vcc	6, 7
Vbias	1
GND	Backside Paddle
GND	2, 4, 5

Specifications (1)

Parameter	Units	Min	Typ	Max
Operational Bandwidth	MHz	400		2700
Test Frequency	MHz		2140	
Gain	dB		13.4	
Input R.L.	dB		14.7	
Output R.L.	dB		7.8	
Output P1dB	dBm		+33	
Output IP3 (2)	dBm		+50	
WCDMA Channel Power (3) @ -50 dBc ACLR	dBm		+24.1	
Noise Figure	dB		4.8	
Vcc, Vbias	V		+5	
Quiescent Collector Current (4)	mA		500	
Iref	mA		30	

1. Test conditions unless otherwise noted: 25ºC, +5V Vsupply, 2140 MHz, in tuned application circuit.
2. 3OIP measured with two tones at an output power of +21 dBm / tone separated by 1 MHz, 940 MHz. OIP3 measured with two tones at an output power of +24 dBm / tone separated by 1 MHz, 1960 MHz and 2140 MHz respectively. The suppression on the largest IM3 product is used to calculate the OIP3 using a 2:1 rule.
3. 3GPP WCDMA, TM1+64DPCH, ±5 MHz Offset, no clipping, PAR = 10.2 dB @ 0.01% Probability.
4. This corresponds to the quiescent current or operating current under small-signal conditions into pins 6 and 7.

Typical Performance

Parameter	Units	Typical		
Frequency	MHz	940	1960	2140
Gain	dB	19.4	14.1	13.4
Input Return Loss	dB	18	11.3	14.7
Output Return Loss	dB	8.5	11.8	7.8
WCDMA Channel Power (3) @ -50 dBc ACLR	dBm	+23.6	+24.4	+24.1
Output P1dB	dBm	+33.0	+33.3	+33
Output IP3 (2)	dBm	+47.6	+50.2	+50
Noise Figure	dB	8.5	4.5	4.8
Vcc, Vbias	V		+5	
Iref	mA		30	
Quiescent Collector Current	mA	600	500	500

Absolute Maximum Rating

Parameter	Rating
Storage Temperature	-65 to +150 °C
RF Input Power, CW, 50 Ω, T = 25ºC	Input P_{10} dB
Device Voltage, Vcc, Vbias	+8 V
Device Current	1400 mA
Device Power	8 W
Thermal Resistance, Rth	18.6 °C / W
Junction Temperature, Tj	+200 °C

Operation of this device above any of these parameters may cause permanent damage.

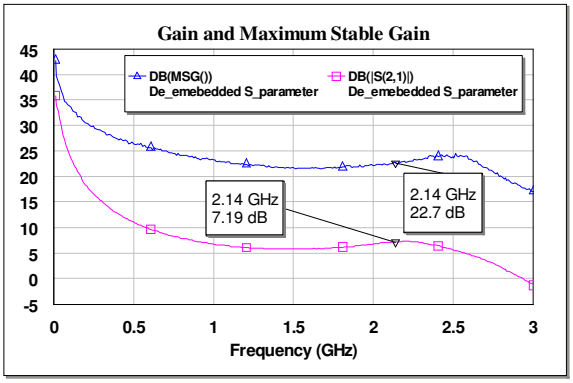
Ordering Information

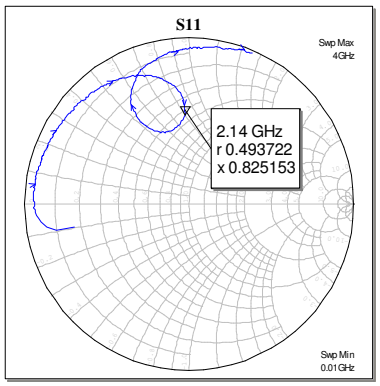
Part No.	Description
AH322-S8G	2W High Linearity InGaP HBT Amplifier (lead-free/RoHS-compliant SOIC-8 Pkg)
AH322-S8PCB900	920 - 960 MHz Evaluation Board
AH322-S8PCB1960	1930 - 1990 MHz Evaluation Board
AH322-S8PCB2140	2110 - 2170 MHz Evaluation Board

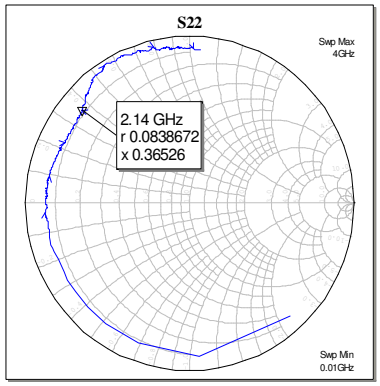
Standard T/R size = 1000 pieces on a 7" reel.

Typical Device Data

S-Parameters (Vcc = +5 V, I_{cq} = 500 mA, T = 25 °C, calibrated to device leads)





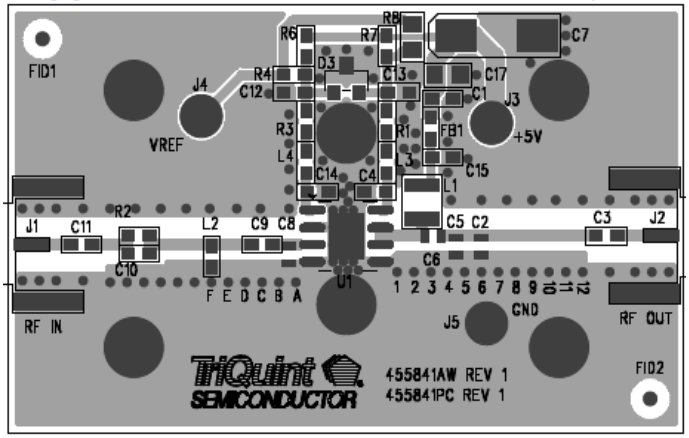


Notes:
The gain for the unmatched device in 50 ohm system is shown as the trace in pink color, [DB (S (2, 1)]. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the blue line [DB (GMAX)].
The impedance plots are shown from 0.01 – 4 GHz, with markers placed in 0.5 GHz increments.

S-Parameters (V_{cc} = +5 V, I_{cq} = 500 mA, T = 25 °C, unmatched 50 ohm system, calibrated to device leads)

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-0.74	-174.58	29.75	109.51	-43.47	25.51	-1.15	-135.3
100	-0.53	-179.31	24.21	98.59	-43.22	17.83	-1.22	-157.31
200	-0.45	176.71	18.46	89.55	-42.49	8.135	-1.19	-170.3
400	-0.44	170.07	12.77	80.82	-42.04	5.31	-1.22	-178.39
600	-0.56	163.11	9.78	73.71	-41.41	10.52	-1.18	176.07
700	-0.61	159.9	8.73	69.49	-41.21	11.31	-1.12	173.93
800	-0.64	156.03	7.94	65.68	-40.26	12.5	-1.17	171.69
1000	-0.78	147.66	6.8	56.95	-39.65	7.88	-1.22	166.82
1200	-0.87	138.49	6.11	46.99	-38.34	2.45	-1.26	162.15
1400	-1.08	128.32	5.8	36.79	-37.99	-3.1	-1.33	157.29
1600	-1.4	117.39	5.83	25.05	-37.52	-14.57	-1.49	152.31
1800	-1.94	106.19	6.17	10.83	-37.39	-27.07	-1.46	147.31
2000	-3.2	95.9	6.8	-7.89	-37.45	-42.22	-1.41	143.05
2200	-5.84	94.01	7.36	-33.75	-38.56	-69.38	-1.21	138.4
2400	-6.52	112.96	6.5	-64.88	-41.93	-115.31	-0.9	133.24
2600	-4.45	121.06	4.77	-92.83	-41.83	167.17	-0.4	126.56
2800	-2.44	117.78	2.24	-121.06	-38.13	103.07	-0.27	119.41
3000	-1.26	108.49	-1.12	-142.85	-34.99	62.15	-0.35	112.36

Application Circuit PC Board Layout



Circuit Board Material: Top RF layer is .014" Getek, ϵ_r = 4.0, 4 total layers (0.062" thick) for mechanical rigidity
1 oz copper, Microstrip line details: width = .026", spacing = .026"
The silk screen markers 'A', 'B', 'C', etc. and '1', '2', '3', etc. are used as placemarkers for the input and output tuning shunt capacitors – C8, C5 and C2. The markers and vias are spaced in .050" increments.

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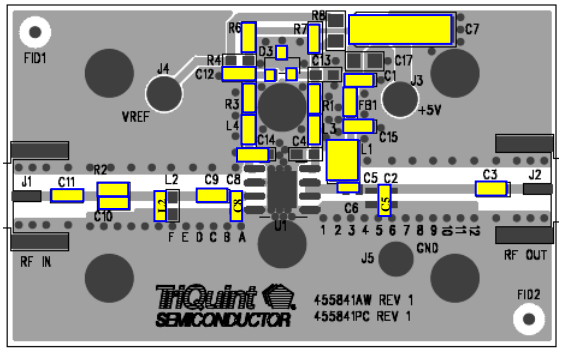
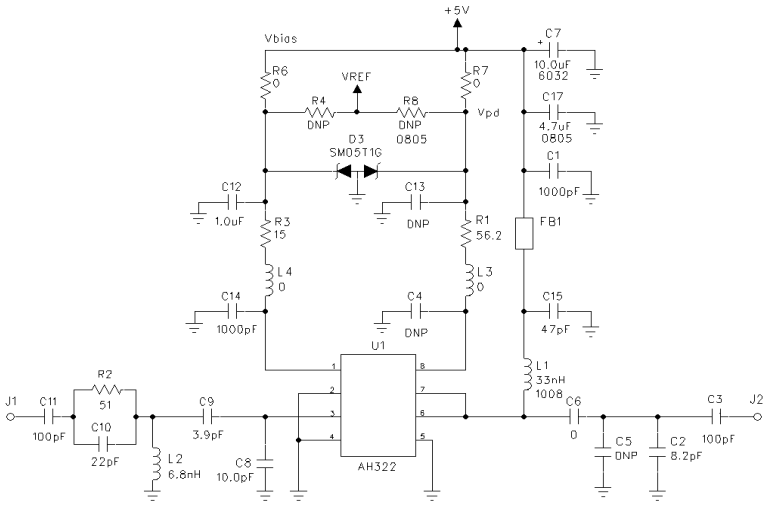
2W High Linearity InGaP HBT Amplifier

824 - 894 MHz Application Circuit

Typical RF Performance at 25 °C

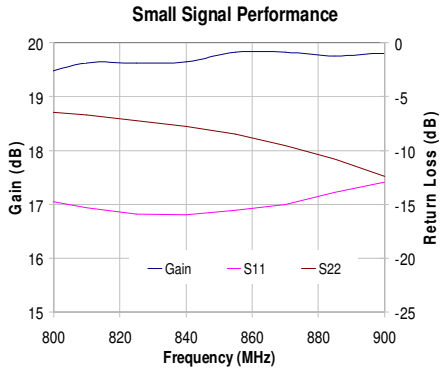
Frequency (MHz)	units	824	848	894
Gain	dB	19.7	19.7	19.7
Input Return Loss	dB	16	16	13
Output Return Loss	dB	7	8	12
Output P1dB	dBm	+33.0	+33	+32.6
Channel Power [1] (@-55 dBc IS-95 CDMA ACPR)	dBm	+24.4	+24.4	+23.8
Channel Power [2] (@ -50 dBc WCDMA ACLR)	dBm	+23.7	+23.7	+23
Output IP3 [3] (21 dBm / tone, 1MHz spacing)	dBm	+46.2	+46.3	+45.1
Quiescent Current, Icq	mA	600		
Vpd [4]	V	+5		
Vcc	V	+5		

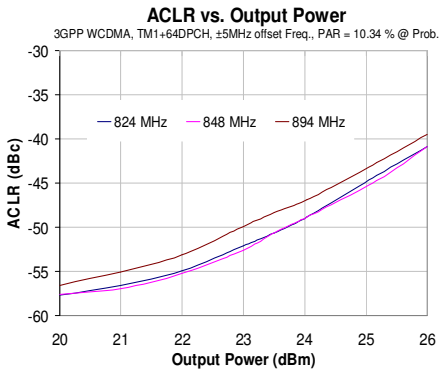


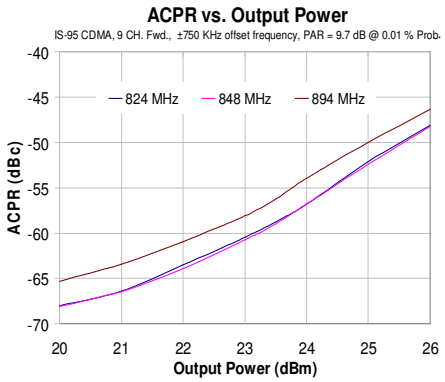


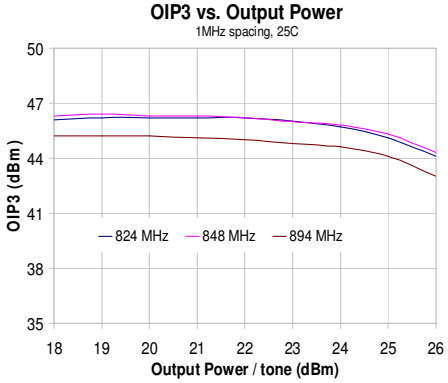
Notes:

1. ACPR test set-up: IS-95 CDMA, 9 channels fwd, ±750 KHz offset, 30 KHz, Meas BW, PAR = 9.7 dB @ 0.01% Prob.
2. ACLR test set-up: 3GPP WCDMA, TM1±64 DPCH, ±5MHz offset no clipping, PAR = 10.34 dB @ 0.01% Probability.
3. OIP3 is measured at 21 dBm / tone output power with 1 MHz spacing.
4. Vpd is used as device power down voltage (low = RF off).
5. The edge of L2 is placed at 265 mils from edge of AH322 RFout pin (12 ° @ 850 MHz).
6. The edge of C2 is placed at 250 mils from edge of AH322 RFout pin (11 ° @ 850 MHz).
7. The edge of C8 is placed at 25 mils from edge of AH322 RFout pin (1 ° @ 850 MHz).
8. Do not exceed +5.5V supply or TVS diode D3 will be damaged.
9. Zero ohm jumpers may be replaced with copper traces in the target application layout.
10. DNP implies Do Not Place.









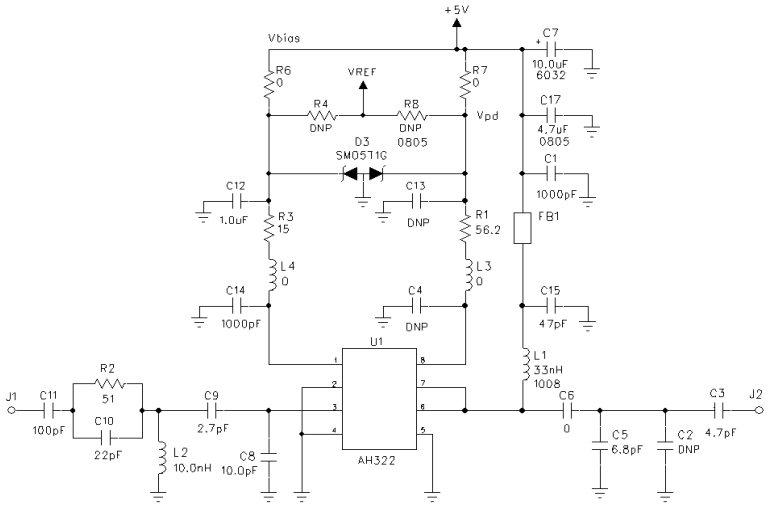
AH322

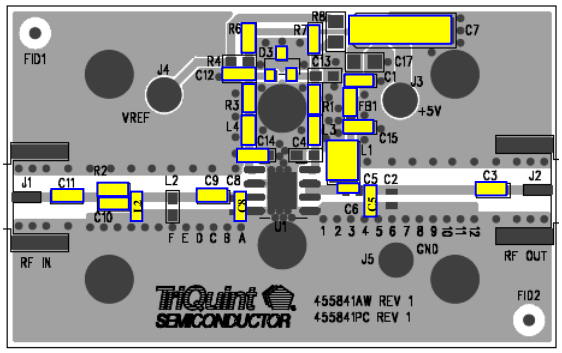
2W High Linearity InGaP HBT Amplifier

920 - 960 MHz Application Circuit (AH322-S8PCB900)

Typical RF Performance at 25 °C

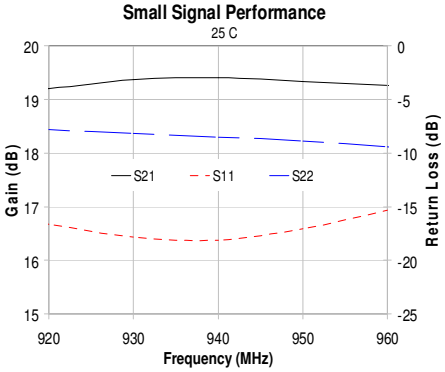
Frequency (MHz)	units	920	940	960
Gain	dB	19.2	19.4	19.2
Input Return Loss	dB	16.6	18	15.3
Output Return Loss	dB	7.8	8.5	9.4
Output P1dB	dBm	+33	+33	+33
Channel Power [1] (@-55 dBc IS-95 CDMA ACPR)	dBm	+24.3	+24.4	+24.3
Channel Power [2] (@ -50 dBc WCDMA ACLR)	dBm	+23.5	+23.6	+23.5
Output IP3 [3] (21 dBm / tone, 1MHz spacing)	dBm	+47.3	+47.6	+47.2
Noise Figure	dB	8.2	8.5	9
Quiescent Current, Icq	mA	600		
Vpd [4]	V	+5		
Vcc	V	+5		

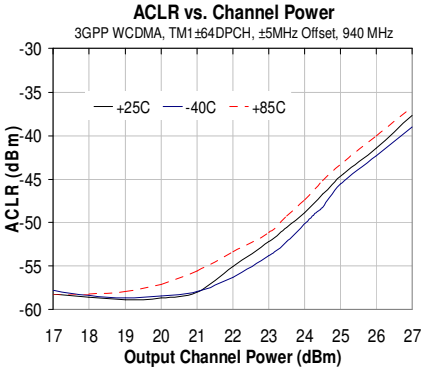


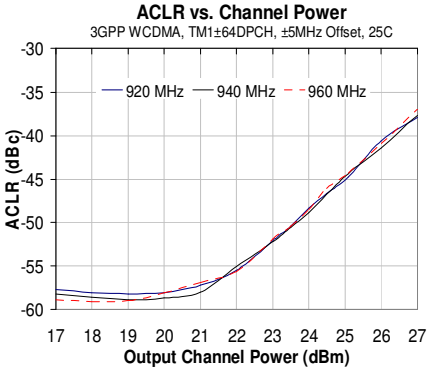


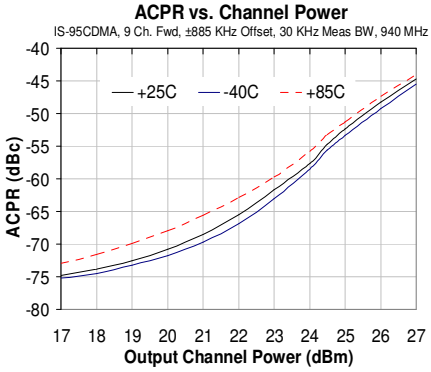
Notes:

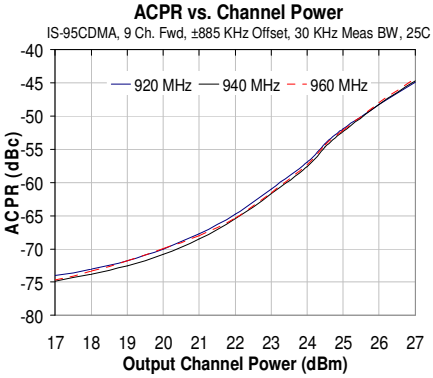
1. ACPR test set-up: IS-95 CDMA, 9 channels fwd, ±885 KHz offset, 30 KHz, Meas BW, PAR = 9.7 dB @ 0.01% Prob.
2. ACLR test set-up: 3GPP WCDMA, TM1±64 DPCH, ±5MHz offset no clipping, PAR = 10.34 dB @ 0.01% Probability.
3. OIP3 is measured at 21 dBm / tone output power with 1 MHz spacing.
4. Vpd is used as device power down voltage (low = RF off).
5. The edge of L2 is placed at 380 mils from the edge of AH322 RFout pin (19 ° @ 940 MHz)
6. The edge of C2 is placed at 190 mils from the edge of AH322 RFout pin (9.5 ° @ 940 MHz).
7. Do not exceed +5.5V supply or TVS diode D3 will be damaged.
8. 0 Ω jumpers may be replaced with copper traces in the target application layout.
9. DNP implies Do Not Place.

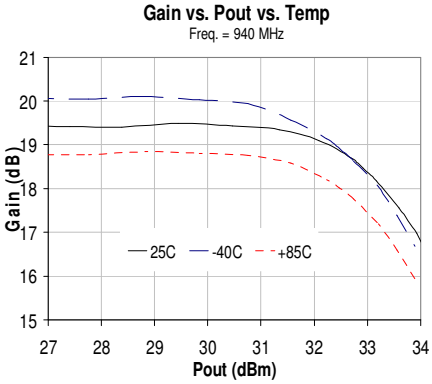




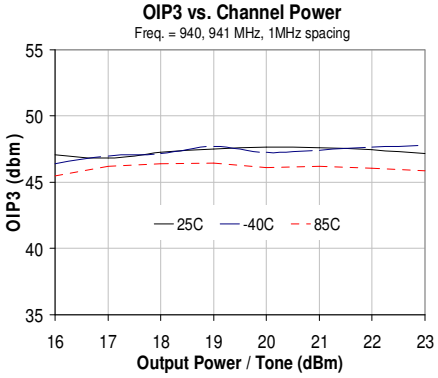


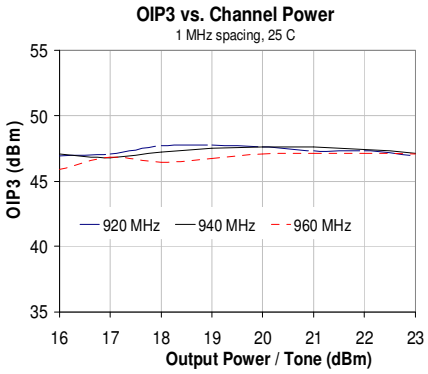


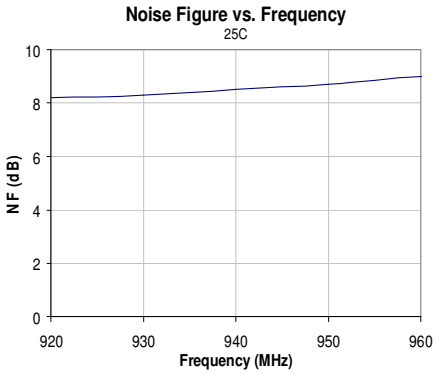




Performance Plots for AH322-S8PCB900 contd.







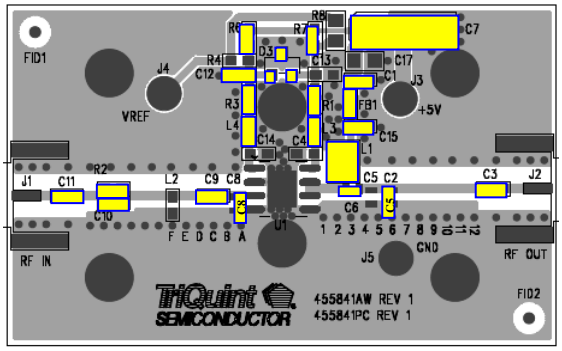
AH322

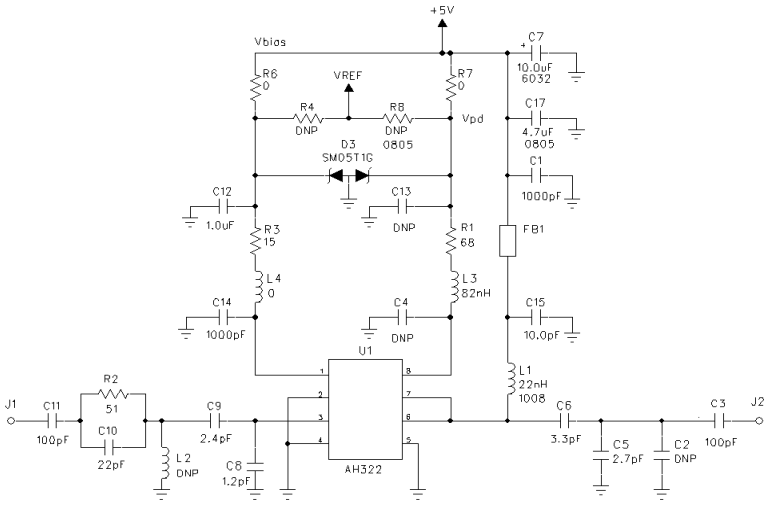
2W High Linearity InGaP HBT Amplifier

1930 - 1990 MHz Application Circuit (AH322-S8PCB1960)

Typical RF Performance at 25 °C

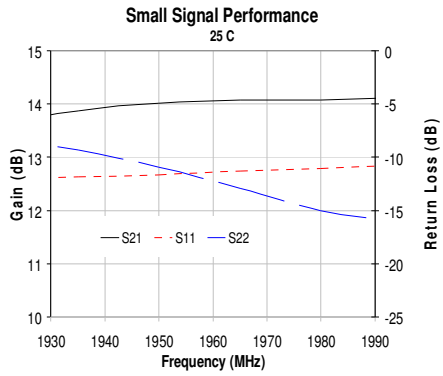
Frequency (MHz)	units	1930	1960	1990
Gain	dB	13.8	14.1	14.2
Input Return Loss	dB	11.8	11.3	10.8
Output Return Loss	dB	9	11.8	15.4
Output P1dB	dBm	+33.2	+33.3	+33.1
Channel Power [1] (@ -50 dBc WCDMA ACLR)	dBm	+23.9	+24.4	+23.7
Output IP3 [2] (24 dBm / tone, 1MHz spacing)	dBm	+47.2	+50.2	+46.7
Noise Figure	dB		4.5	
Quiescent Current, Icq	mA	500		
Vpd [4]	V	+5		
Vcc	V	+5		

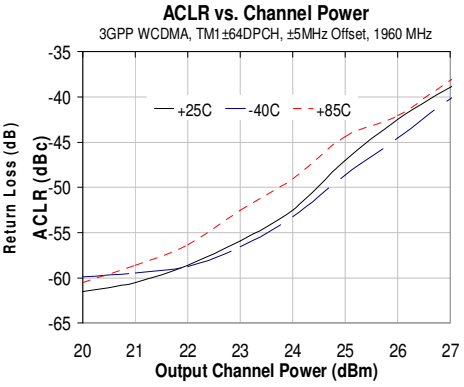


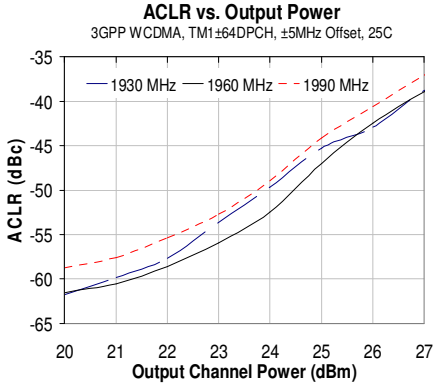


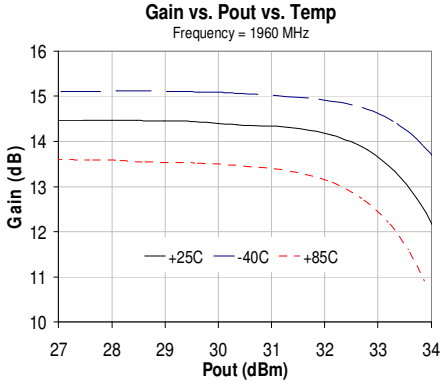
Notes:

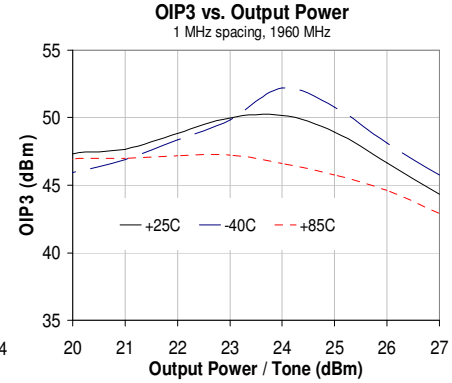
1. ACLR test set-up: 3GPP WCDMA, TM1±64 DPCH, ±5MHz offset no clipping, PAR = 10.34 dB @ 0.01% Probability.
2. OIP3 is measured at 24 dBm / tone output power with 1 MHz spacing.
3. The multilayer inductor L3 (82nH) is critical for linearity performance.
4. Vpd is used as device power down voltage (low = RF off).
5. The edge of C5 is placed at 247 mils from the edge of AH322 RFout pin (11 ° @ 1960 MHz).
6. Do not exceed +5.5V supply or TVS diode D3 will be damaged.
7. 0 Ω jumpers may be replaced with copper traces in the target application layout.
8. DNP implies Do Not Place.

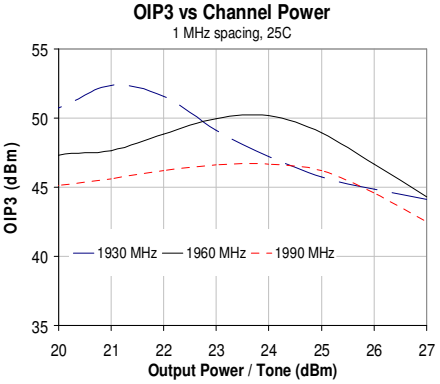












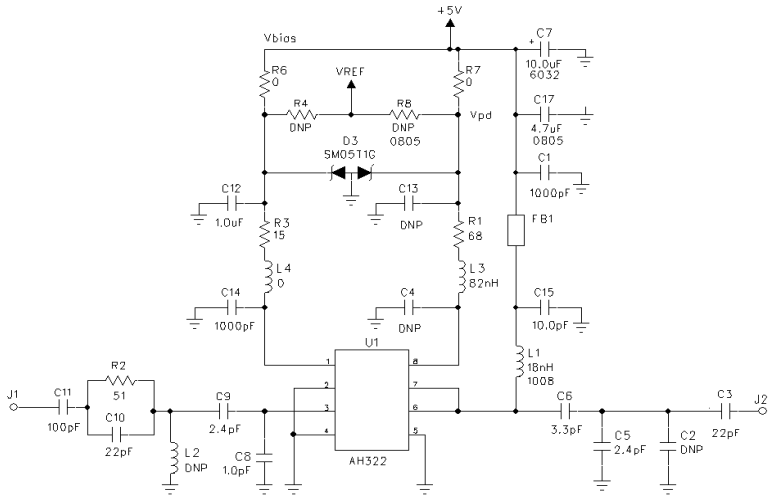
AH322

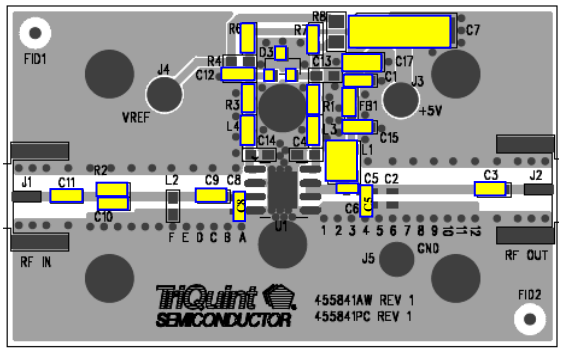
2W High Linearity InGaP HBT Amplifier

2110 - 2170 MHz Application Circuit (AH322-S8PCB2140)

Typical RF Performance at 25 °C

Frequency (MHz)	units	2110	2140	2170
Gain	dB	13.1	13.4	13.6
Input Return Loss	dB	15	14.7	14.2
Output Return Loss	dB	6.3	7.8	10
Output P1dB	dBm		+33	
Channel Power [1] (@ -50 dBc WCDMA ACLR)	dBm	+24.1	+24.1	+23.8
Output IP3 [2] (24 dBm / tone, 1MHz spacing)	dBm	+50.1	+50	+48.4
Noise Figure	dB	4.7	4.8	4.7
Quiescent Current, Icq	mA	500		
Vpd [4]	V	+5		
Vcc	V	+5		

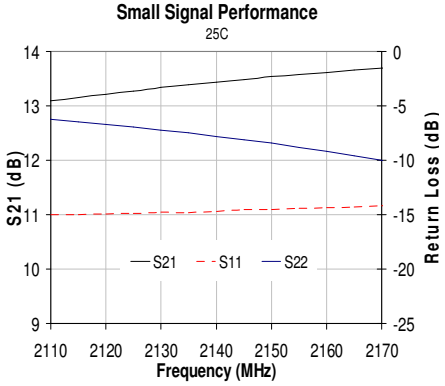




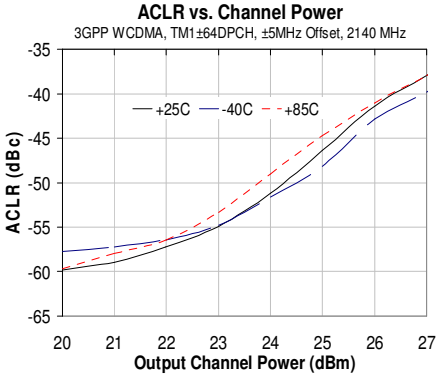
Notes:

1. ACLR test set-up: 3GPP WCDMA, TM1±64 DPCH, ±5MHz offset no clipping, PAR = 10.34 dB @ 0.01% Probability.
2. OIP3 is measured at 24 dBm / tone output power with 1 MHz spacing.
3. The multilayer inductor L3 (82 nH) is critical for linearity performance..
4. Vpd is used as device power down voltage (low = RF off).
5. The edge of C5 is placed at 195 mils from the edge of AH322 RFout pin (22 ° @ 2140 MHz).
6. The edge of C8 is placed at 0.5 mils from the edge of AH322 RFout pin (0 ° @ 2140 MHz).
7. Zero ohm jumpers may be replaced with copper traces in the target application layout.
8. DNP means Do Not Place.

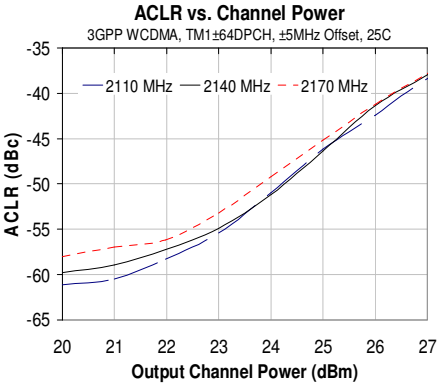
Small Signal Performance



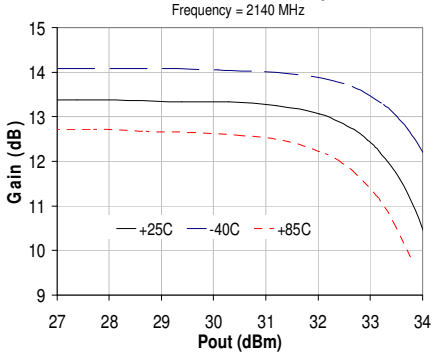
ACLR vs. Channel Power



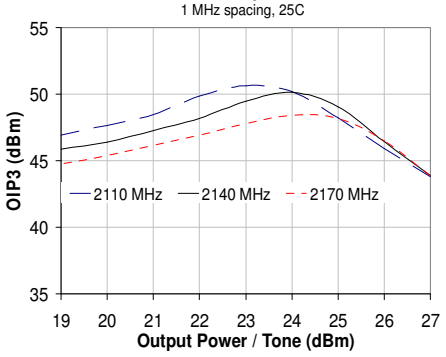
ACLR vs. Channel Power



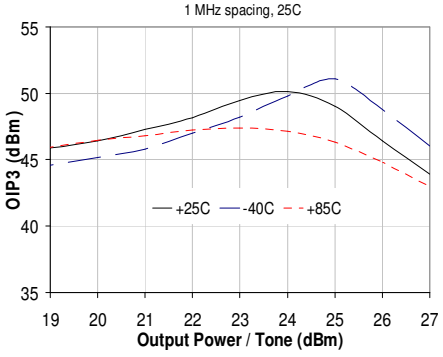
Gain vs. Pout vs. Temp



OIP3 vs. Output Power



OIP3 vs Channel Power



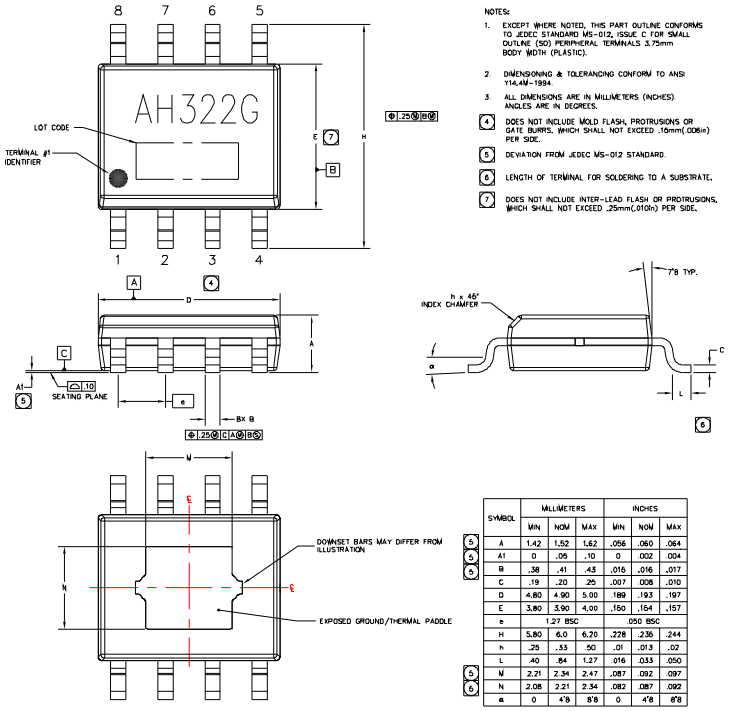
AH322

2W High Linearity InGaP HBT Amplifier

Mechanical Information

This package is lead-free/green/RoHS-compliant. The plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

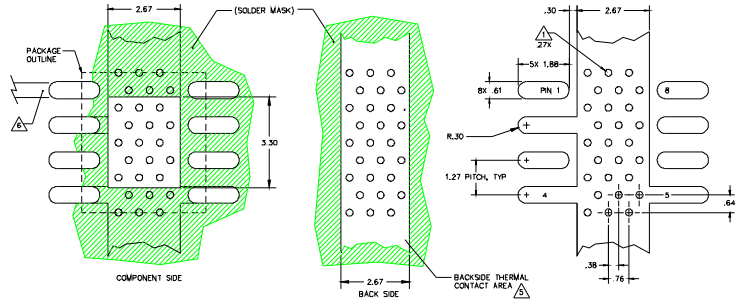
Outline Drawing



NOTES:
1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MS-012, ISSUE C FOR SMALL OUTLINE (SO) PERIPHERAL TERMINALS 3.75mm BODY WIDTH (PLASTIC).
2. DIMENSIONING & TOLERANCING CONFORM TO ANSI Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES). ANGLES ARE IN DEGREES.
4. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS, WHICH SHALL NOT EXCEED .15mm(.006in) PER SIDE.
5. DEVIATION FROM JEDEC MS-012 STANDARD.
6. LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS, WHICH SHALL NOT EXCEED .25mm(.010in) PER SIDE.

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.42	1.52	1.62	.056	.060	.064
A1	0	.05	.10	0	.002	.004
B	.38	.41	.43	.015	.016	.017
C	.19	.20	.25	.007	.008	.010
D	4.80	4.90	5.00	.189	.193	.197
E	3.80	3.90	4.00	.150	.154	.157
e	1.27 BSC			.050 BSC		
H	5.80	6.0	6.20	.228	.236	.244
h	.25	.33	.50	.01	.013	.02
L	.40	.84	1.27	.016	.033	.050
M	2.21	2.34	2.47	.087	.092	.097
N	2.08	2.21	2.34	.082	.087	.092
α	0	4°8	8°8	0	4°8	8°8

Mounting Configuration / Land Pattern



Mounting Config. Notes

1. A heatsink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contact the heatsink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8. All dimensions are in millimeters (inches). Angles are in degrees.

Product Marking

The component will be marked with an "AH322G" designator with an alphanumeric lot code on the top surface of the package.

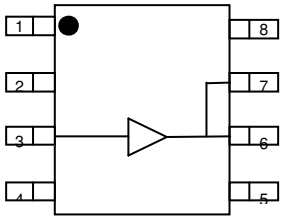
Tape and reel specifications for this part are located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Rating:	Class 1A
Value:	Passes ≥ 250V to < 500V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
ESD Rating:	Class III
Value:	Passes ≥ 1000V min.
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101
MSL Rating:	Level 3 at +260 °C convection reflow
Standard:	JEDEC Standard J-STD-020

Functional Diagram



Function	Pin No.
Iref	8
Input	3
Output / Vcc	6, 7
Vbias	1
GND	Backside Paddle
GND	2, 4, 5