16-bit 30 Ω terminated bus transceiver with direction pin; 3-state

74ALVC16245-1

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no.8-1A
- CMOS low power consumption
- Multibyte™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold
- Output drive capability 50 Ω transmission lines @ 85 °C

DESCRIPTION

The ALVC16245-1 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The ALVC16245-1 is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The '16245-1' features two output enable ($n\overline{OE}$) inputs for easy cascading and two send/receive (nDIR) inputs for direction control. $n\overline{OE}$ controls the outputs so that the buses are effectively isolated.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$n\overline{OE}$	nDIR	nA_n	nB_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	2.2	ns
C_I	input capacitance		3.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16245-1DL	48	SSOP48	plastic	SSOP48/SOT370
74ALVC16245-1DGG	48	TSSOP48	plastic	TSSOP48/SOT362

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	1DIR	'1' direction control
2, 3, 5, 6, 8, 9, 11, 12	$1B_0$ to $1B_7$	'1B' data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
7, 18, 31, 42	V_{CC}	positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	$2B_0$ to $2B_7$	'2B' data inputs/outputs
24	2DIR	'2' direction control
25	$2\overline{OE}$	'2' output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	$2A_0$ to $2A_7$	'2A' data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	$1A_0$ to $1A_7$	'1A' data inputs/outputs
48	$1\overline{OE}$	'1' output enable input (active LOW)

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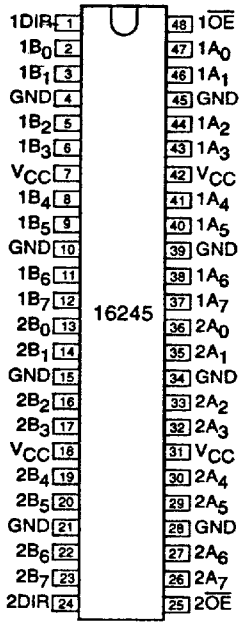


Fig.1 Pin configuration.

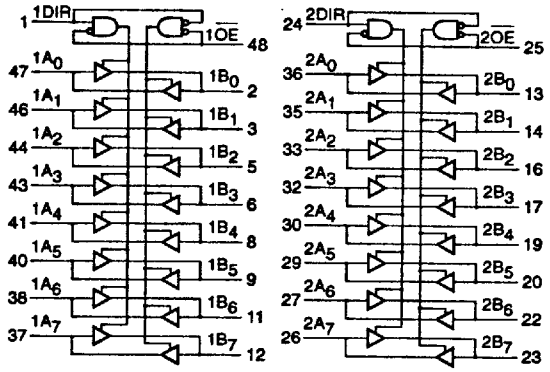


Fig.2 Logic symbol.

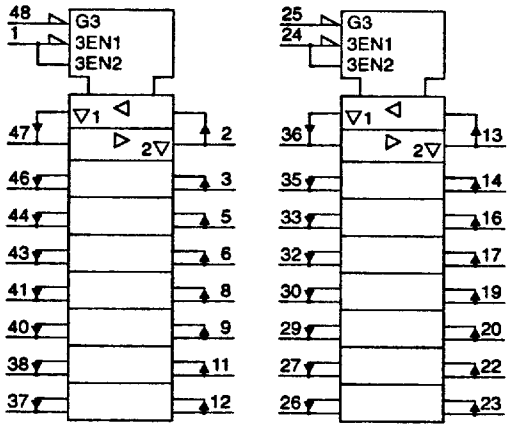


Fig.3 IEC logic symbol.

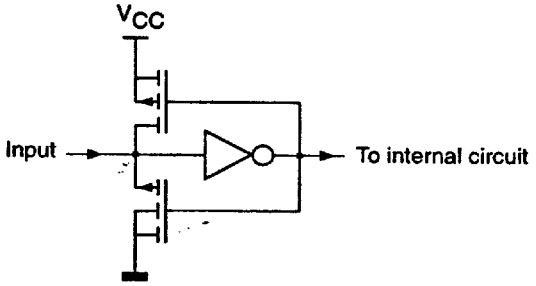


Fig.4 Bushold circuit.

DC CHARACTERISTICS FOR ALVC16245-1

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR ALVC16245-1

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) −40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay	–	16.0	–	ns	1.2	Fig.5
	nA_n to nB_n;	–	–	4.0		2.7	
	nB_n to nA_n	–	2.3*	3.6		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time	–	–	–	ns	1.2	Fig. 6
	$n\overline{OE}$ to nA_n;	–	–	5.0		2.7	
	$n\overline{OE}$ to nB_n	–	–	4.7		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	–	–	ns	1.2	Fig. 6
	$n\overline{OE}$ to nA_n;	–	–	5.2		2.7	
	$n\overline{OE}$ to nB_n	–	–	5.0		3.0 to 3.6	

Noths: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

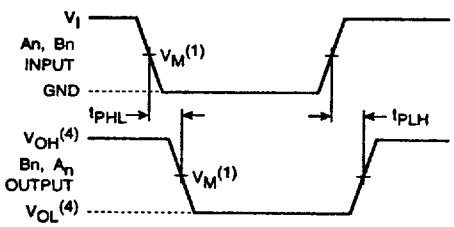


Fig. 5 Waveforms showing the input (nA_n, nB_n) to output (nB_n, nA_n) propagation delay times.

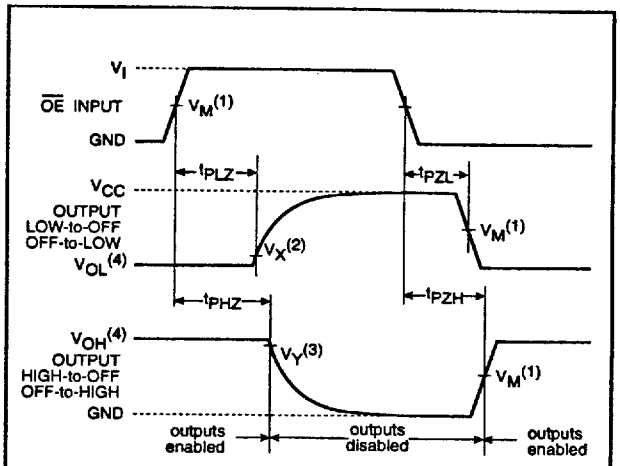
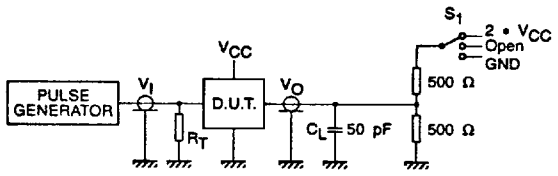


Fig.6 Waveforms showing the 3-state enable and disable times.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig. 7 Load circuitry for switching times.

Notes:

(1) $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V

(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.