GigaBit Logic

10G004

T-68-21-51

Quad 2:1 Multiplexer
1.8 GHz/3.6 Gbit/s NRZ Data Rate
10G PicoLogic™ Family

FEATURES

- 3.6 Gbit/sec output NRZ data rate
- 150 ps output rise and fall times
- Independent or common multiplexing controls
- ECL and 10G PicoLogic™ compatible I/O
- Temperature and voltage compensated design
- On-chip VBBS threshold reference voltage supply
- Wire-OR output capability
- Available in 40 pin C-leaded or leadless chip carrier or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

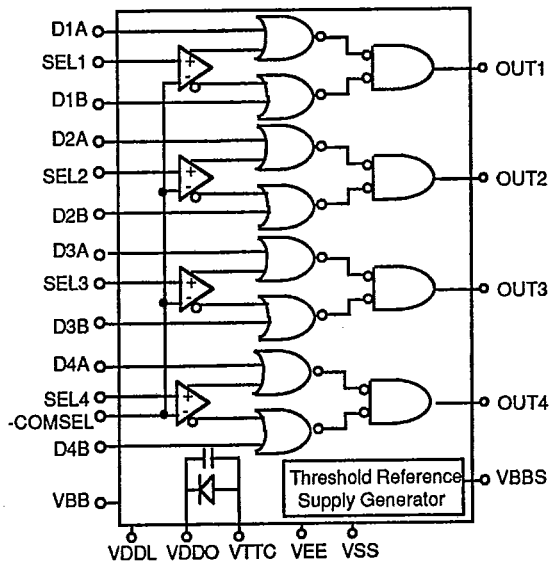
- High Speed Logic
- High Speed Fiber Optic Multiplexing

FUNCTIONAL DESCRIPTION

The 10G004 is an ECL and 10G PicoLogic™ I/O compatible ultra-fast quad 2:1 multiplexer with both independent and common multiplexing controls.
Minimum 25°C multiplexing frequency is 1.8 GHz, making the 10G004 capable of generating a 3.6 Gbit/sec output NRZ data rate while dissipating just 700mW. Typical propagation delay is 450ps for the data inputs and 550ps for SEL and -COMSEL inputs. For compatibility with other high speed logic families, the 10G004 features the PicoLogic™ family standard VBB input which allows the input logic threshold to be controlled by the driving logic family. This way, mismatches in threshold level due to temperature and power supply variation can be compensated, providing high system noise immunity. An on-chip threshold reference voltage output (pin VBBS) is also provided. VBBS must be strapped to the VBB input when PicoLogic™ is used to drive the 10G004.

The 10G004 is a member of GigaBit's PicoLogic™ family of GaAs digital integrated circuits, and is fabricated using GigaBit's high volume GaAs MESFET process technology.

BLOCK DIAGRAM



10G004 ORDERING INFORMATION

PACKAGE TYPE	SPEED (Min. 0°C to 85°C)	
	1.6 GHz	1.3 GHz
C-Leaded CC Leadless CC Die	10G004-2C 10G004-2L	10G004-3C 10G004-3L 10G004-3X

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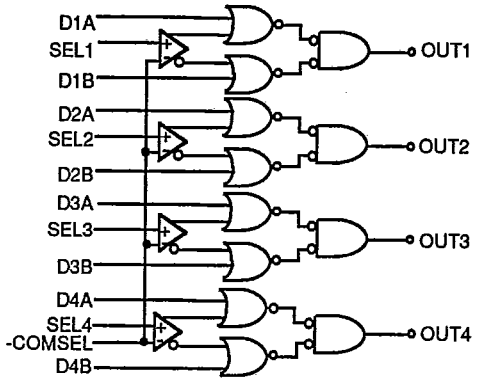
10G004 Operation



TRUTH TABLE				
-COMSEL	SELn	DA	DB	OUT
VBBS	1	X	1	1
VBBS	1	X	0	0
VBBS	0	1	X	1
VBBS	0	0	X	0
1	VBBS	1	X	1
1	VBBS	0	X	0
0	VBBS	X	1	1
0	VBBS	X	0	0

The operation of the 10G004 is illustrated by referring to the logic diagram and truth table above. Each of the four multiplexers will select either the DA or DB input and direct it to the output in response to the individual SELn controls or the common select (-COMSEL) control. Each of the four SELn inputs (SEL1 ... SEL4) forms a differential input with the -COMSEL input. For this reason, the -COMSEL input must be tied to the threshold reference voltage VBBS when individual multiplex control is required. Similarly, when all four multiplexers are to be switched in common using -COMSEL, SEL1 through SEL4, must all be tied to the VBBS output. When the SELn inputs are high (low), the DB (DA) inputs are selected and directed to the output. If the -COMSEL control is used instead, the function is reversed with a high on -COMSEL selecting the DA inputs and a low selecting the DB inputs.

Again, the select control inputs not being driven must be tied to the VBBS threshold output pin for proper operation.

Pin Descriptions

D1A - D4A	A data inputs
D1B - D4B	B data inputs
SEL1 - SEL4	Individual multiplexer input selection controls (differential input)
-COMSEL	Common select control for all four multiplexers (differential input)
OUT1- OUT4	Multiplexer outputs
VDDO	Output driver ground pin
VDDL	Internal logic ground connection
VSS	-3.4V power supply
VEE	-5.2V power supply
VTTC	The AC return pin for the package internal VDDO decoupling capacitor. VTTC is not brought onto the 10G004 circuit, and is typically tied to VTT (nominally -2.0V)
VDCH	Output driver high level clamp voltage. When not used, VDCH should be connected to VDDO. When driving ECL, VDCH may be used to limit VOH. Consult Application Note 4 for detail.
VBB	Reference input to the 10G004's input threshold tracking circuit. Connect to the VBB supplied from ECL when driving the 10G004 from ECL. Connect to the VBBS pin when the 10G004 is driven from PicoLogic. This pin may not be left unconnected.
VBBS	PicoLogic threshold reference output voltage. Connect to VBB when driving from PicoLogic.

DC CHARACTERISTICS

Tc = 0°C to 85°C, VSS = -3.5 V to -3.3 V, VEE = -5.5 to -5.1 V, VDDL = VDDO = 0 V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
IINCS	COMSEL Input Current	-1000	350	1000	µA	Vin: -1.0 to -1.6 V
ISS	Power Supply Current		115	170	mA	
IEE	Power Supply Current		55	85	mA	
PD	Power Dissipation		700	1020	mW	

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

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SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
F	Multiplexing frequency	1.8		1.8	2.0		1.6		GHz	
T1	SELn, -COMSEL to output delay	350	700	350	550	700	400	825	ps	
T2	Data inputs to output delay	300	600	300	450	600	300	650	ps	
T3	Output rise and fall times		175		125	175		200	ps	2

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SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
F	Multiplexing frequency	1.5		1.5	1.8		1.3		GHz	
T1	SELn, -COMSEL to output delay	350	750	350	600	750	400	875	ps	
T2	Data inputs to output delay	300	650	300	500	650	300	700	ps	
T3	Output rise and fall times		210		150	210		225	ps	2

NOTES:
1. Test conditions (unless otherwise noted): VBB = -1.2V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VDCH = VDDO, VIH = -0.7V, VIL = -1.7V, VOH ≥ -0.7V, VOL ≤ -1.7V. Input signal rise and fall times <150ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

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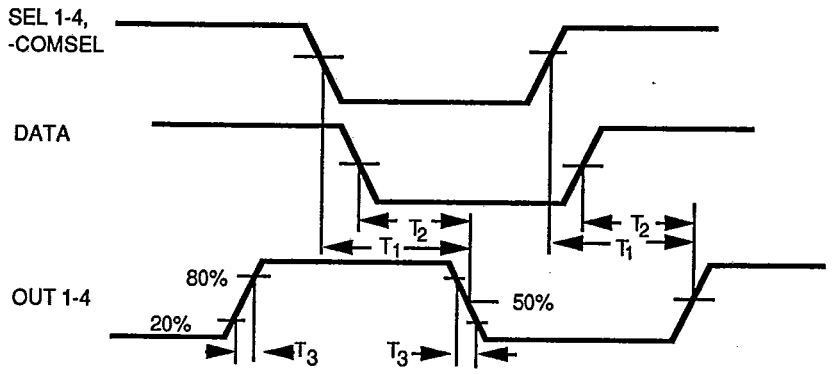
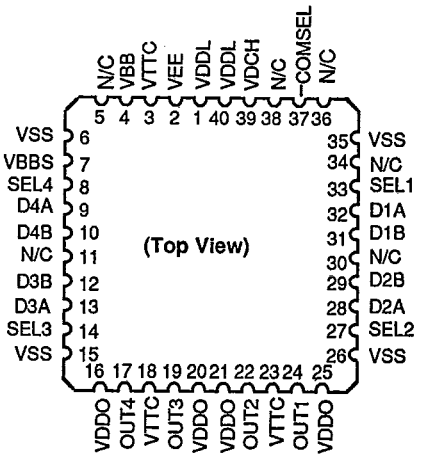
SWITCHING WAVEFORMS



PIN FUNCTIONS - PACKAGE TYPES "L" AND "C"



NOTES:
Pin 1 is marked for orientation. N/C = no connection.

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24 PIN HYBRID 18 PIN PACKAGE

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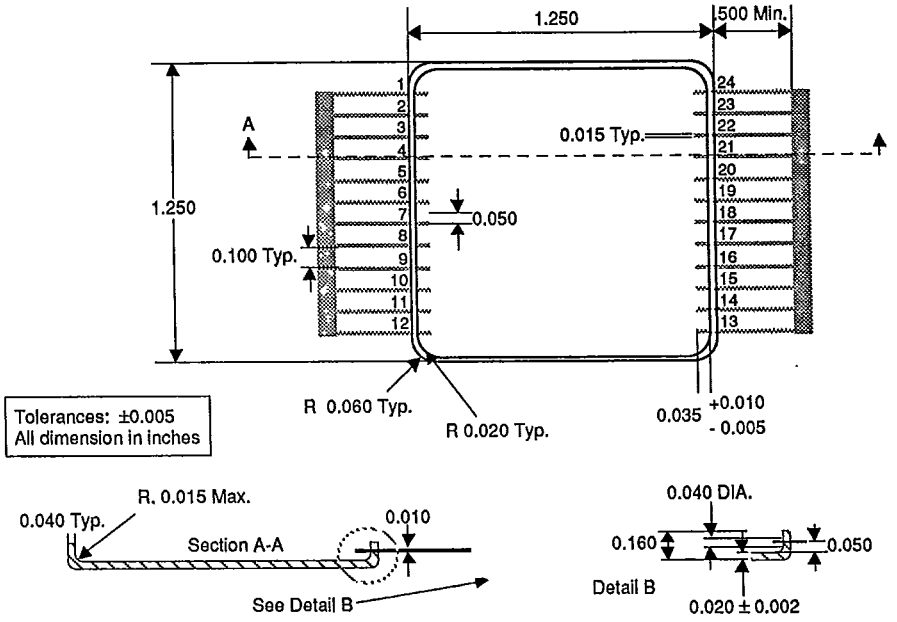
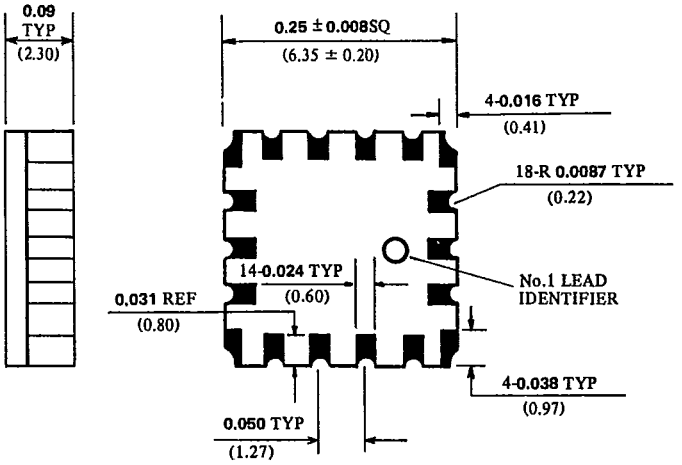
24 PIN HYBRID PACKAGE

Type H



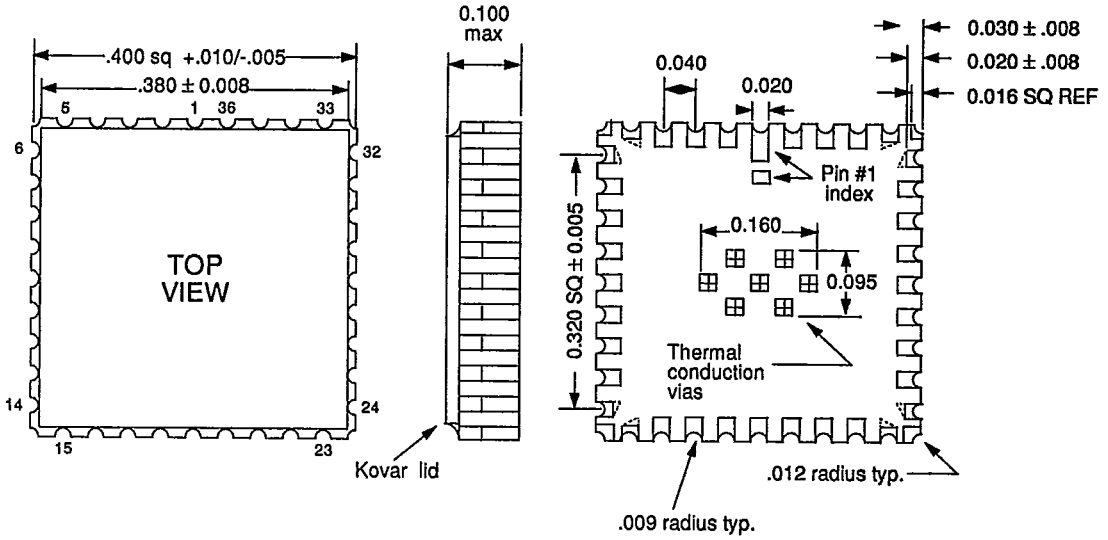
18 PIN LEADLESS CHIP CARRIER

TYPE L1



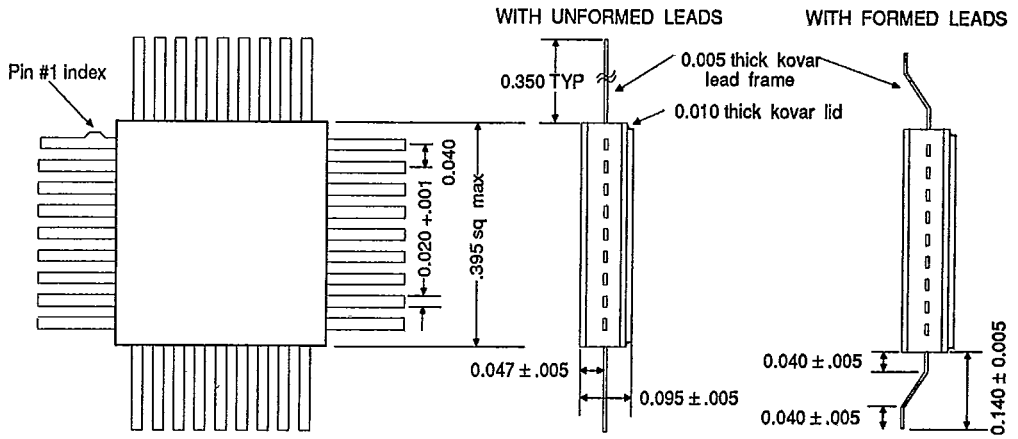
All dimensions shown in **inches** and (millimeters)

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Pin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



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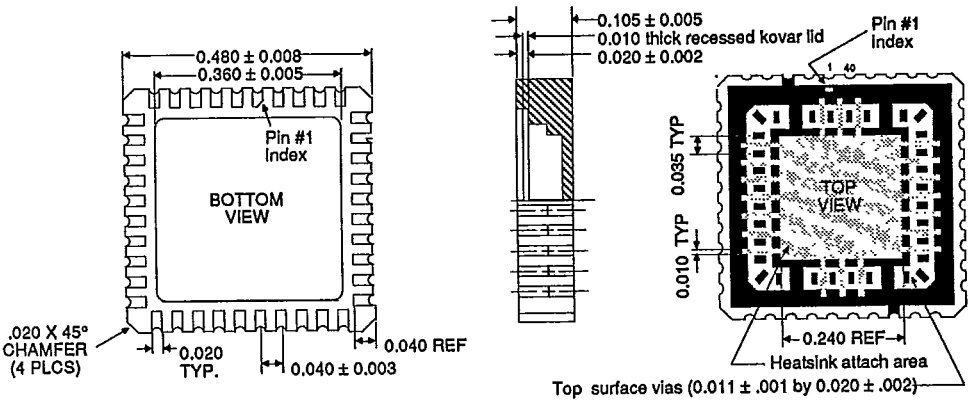
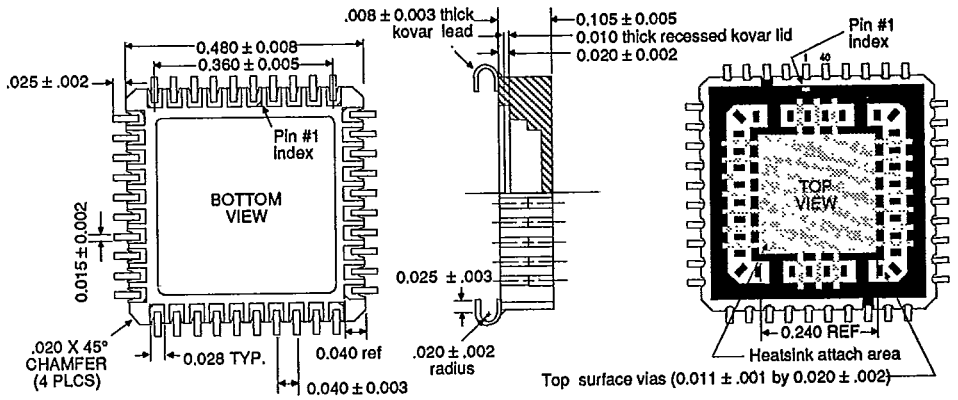
40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L



40 PIN LEADED CHIP CARRIER
TYPE C

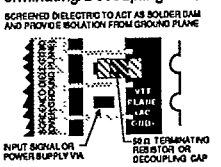


NOTES:

(1) Footprint is JEDEC standard outline.
(2) Top surface vias (for terminating resistors and decoupling capacitors) are not available on pins 3,4,17, 18, 23,24,37 and 38.
(3) Top surface metal (not including vias) and pins 3 and 23 are fixed at VTT potential.
(4) Recommended top surface chip resistors are0.040 long by 0.020 wide by 0.010 thick typ, 100 mw min. nominal power rating (Mini-Systems MSR-21 or equivalent.)
(5) Recommended top surface chip capacitors are 0.040 long by 0.030 wide by 0.020 thick typ, 25V VDCW, 1000 pf, min. (Johanson R09 case or equivalent).
(6) Recommended heatsinks are GBL P/Ns 90GHS-40-A and 90GHS-40-B.
(7) Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789-4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width.

TOP SURFACE LEGEND:
Metalized Ceramic.....
Screened Dielectric.....
Bare Ceramic.....

Top Surface Terminating/Decoupling Detail



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68 & 132 PIN PACKAGES

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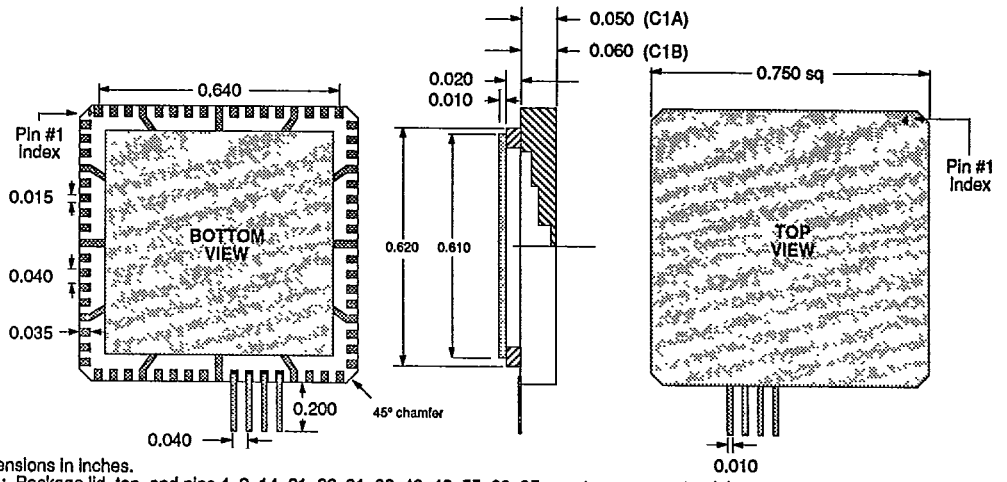
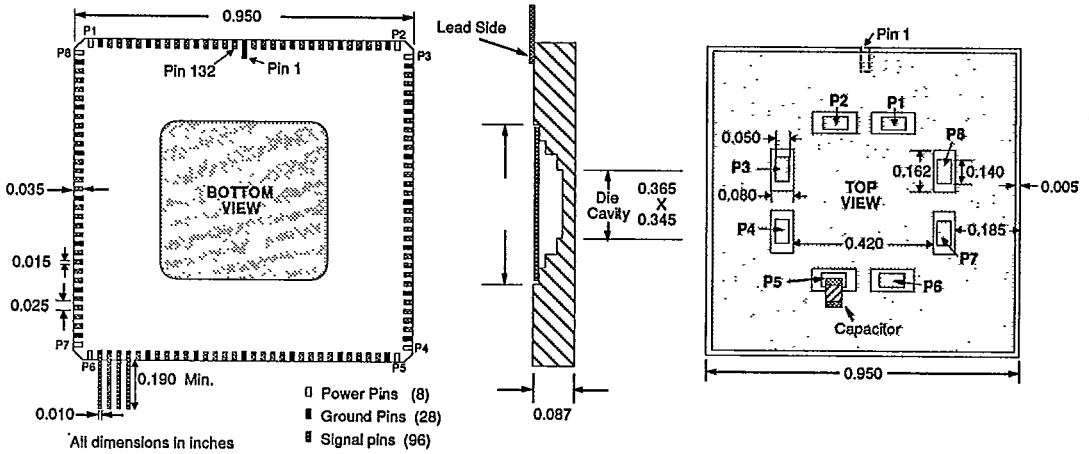
68 PIN LEADED CHIP CARRIER
TYPE C1



(1) All dimensions in inches.
(2) a. C1A: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
b. C1B: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).

132 PIN LEADED CHIP CARRIER
TYPE C3



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