APPLICATION NOTE

A V A I L A B L E

AN56

16K X20C17 2K x 8 Bit

High Speed AUTOSTORE™ NOVRAM

FEATURES

- **24-Pin Standard SRAM DIP Pinout**
- **Fast Access Time: 35ns, 45ns, 55ns**
- **High Reliability**
  - **—Endurance: 1,000,000 Nonvolatile Store Operations**
  - **—Retention: 100 Years Minimum**
- **AUTOSTORE™ NOVRAM**
  - **—Automatically Stores SRAM Data Into the E^2PROM Array When V_{CC} Low Threshold is Detected**
  - **—E^2PROM Data Automatically Recalled Into RAM Upon Power-up**
- **Low Power CMOS**
  - **—Standby: 250μA**
- **Infinite E^2PROM Array Recall, and RAM Read and Write Cycles**

DESCRIPTION

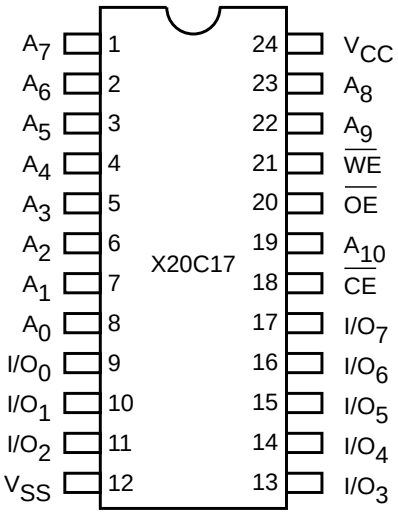
The Xicor X20C17 is a 2K x 8 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E^2PROM) and the AUTOSTORE feature which automatically saves the RAM contents to E^2PROM at power-down. The X20C17 is fabricated with advanced CMOS floating gate technology to achieve high speed with low power and wide power-supply margin. The X20C17 features a compatible JEDEC approved byte-wide memory pinout for industry standard SRAMs.

The NOVRAM design allows data to be easily transferred from RAM to E^2PROM (store) and E^2PROM to RAM (recall). The store operation is completed in 2.5ms or less. An automatic array recall operation reloads the contents of the E^2PROM into RAM upon power-up.

Xicor NOVRAMS are designed for unlimited write operations to RAM, either from the host or recalls from E^2PROM, and a minimum 1,000,000 store operations to the E^2PROM. Data retention is specified to be greater than 100 years.

PIN CONFIGURATION

PLASTIC



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AUTOSTORE™ NOVRAM is a trademark of Xicor, Inc.

PIN DESCRIPTIONS

Addresses (A_0–A_{10})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of $\overline{CE}$, $\overline{WE}$.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X20C17 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH.

Write Enable ($\overline{WE}$)

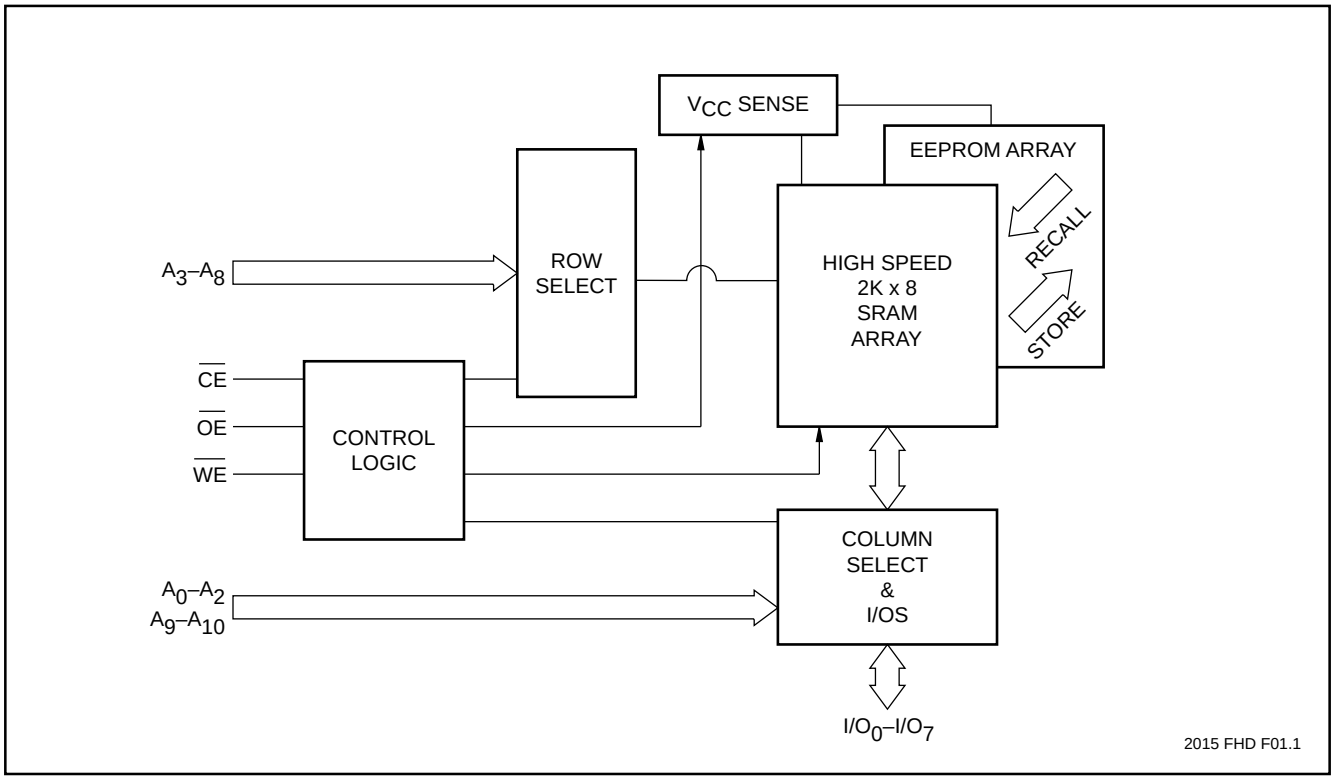
The Write Enable input controls the writing of data to the static RAM.

PIN NAMES

Symbol	Description
A_0–A_{10}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground

2015 PGM T01

FUNCTIONAL DIAGRAM



2015 FHD F01.1

DEVICE OPERATION

The $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ inputs control the X20C17 operation. The X20C17 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

RAM Operations

RAM read and write operations are performed as they would be with any static RAM. A read operation requires $\overline{CE}$ and $\overline{OE}$ to be LOW. A write operation requires $\overline{CE}$ and $\overline{WE}$ to be LOW. There is no limit to the number of read or write operations performed to the RAM portion of the X20C17.

Memory Transfer Operations

There are two memory transfer operations: a recall operation whereby the data stored in the E^2PROM array is transferred to the RAM array; and a store operation which causes the entire contents of the RAM array to be stored in the E^2PROM array.

Recall operations are performed automatically upon power-up.

Store operations are performed automatically upon power-down. The store operation take a maximum of 2.5ms.

Write Protection

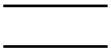
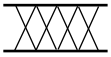
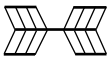
The X20C17 supports two methods of protecting the nonvolatile data.

—If after power-up no RAM write operations have occured, no AUTOSTORE operation can be initiated.

—V_{CC} Sense – All functions are inhibited when V_{CC} is ≤ 3V typical.

SYMBOL TABLE

The following symbol table provides a key to understanding the conventions used in the device timing diagrams. The diagrams should be used in conjunction with the device timing specifications to determine actual device operation and performance, as well as device suitability for user's application.

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 10mA
Lead Temperature (Soldering, 10 seconds)..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any conditions other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

2015 PGM T02.1

Supply Voltage	Limits
X20C17	4.5V to 5.25V

2015 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I_{CC1}	V_{CC} Current (Active)		100	mA	$\overline{WE}$ = V_{IH}, $\overline{CE}$ = $\overline{OE}$ = V_{IL} Address Inputs = 0.4V/2.4V Levels @ f = 20MHz, All I/Os = Open
I_{CC2}(2)	V_{CC} Current During AUTOSTORE		2.5	mA	All I/Os = Open
I_{SB1}	V_{CC} Standby Current (TTL Input)		10	mA	All Inputs = V_{IH}, All I/Os = Open
I_{SB2}	V_{CC} Standby Current (CMOS Input)		250	µA	All Inputs = V_{CC} – 0.3V All I/Os = Open
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(1)	Input LOW Voltage	–1	0.8	V	
V_{IH}(1)	Input HIGH Voltage	2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 4mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –4mA

2015 PGM T04.3

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-Up to RAM Operation	100	µs
t_{PUW}(2)	Power-Up to Nonvolatile Operation	5	ms

2015 PGM T05

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

2015 PGM T06.2

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

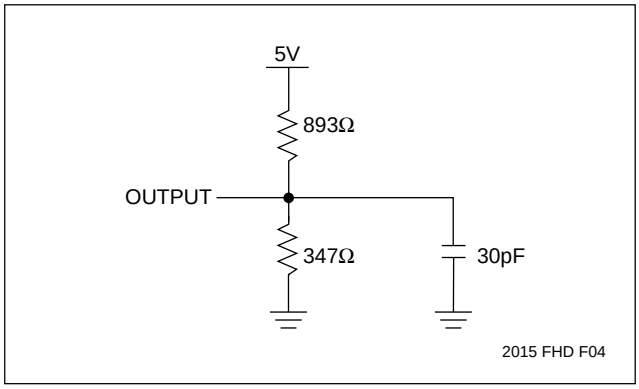
2015 PGM T07.1

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	Not Selected	Output High Z	Standby
L	H	L	Read RAM	Output Data	Active
L	L	H	Write “1” RAM	Input Data High	Active
L	L	H	Write “0” RAM	Input Data Low	Active
L	L	L	Not Allowed	Output High Z	Active
L	H	H	No Operation	Output High Z	Active

2015 PGM T09

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

2015 PGM T08.1

A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	X20C17-35		X20C17-45		X20C17-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35		45		55		ns
t_{CE}	Chip Enable Access Time		35		45		55	ns
t_{AA}	Address Access Time		35		45		55	ns
t_{OE}	Output Enable Access Time		20		25		30	ns
t_{LZ}(3)	Chip Enable to Output in Low Z	0		0		0		ns
t_{OLZ}(3)	Output Enable to Output in Low Z	0		0		0		ns
t_{HZ}(3)	Chip Disable to Output in High Z	0	15	0	20	0	25	ns
t_{OHZ}(3)	Output Disable to Output in High Z	0	15	0	20	0	25	ns
t_{OH}	Output Hold From Address Change	0		0		0		ns

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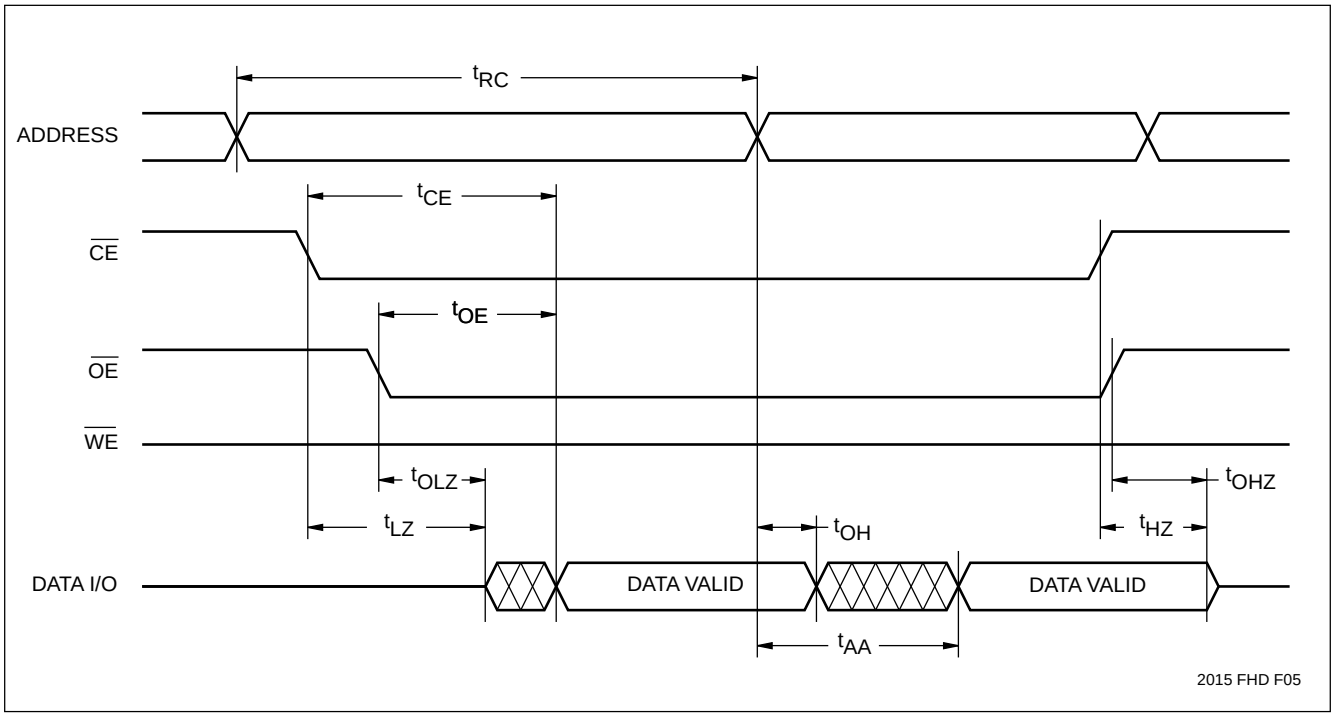
Read Cycle



2015 FHD F05

Note: (3) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the Outputs are no longer driven.

Write Cycle Limits

Symbol	Parameter	X20C17-35		X20C17-45		X20C17-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	35		45		55		ns
t_{CW}	Chip Enable to End of Write Input	30		35		40		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	30		35		40		ns
t_{WR}	Write Recovery Time	0		0		0		ns
t_{DW}	Data Setup to End of Write	15		20		25		ns
t_{DH}	Data Hold Time	3		3		3		ns
t_{OEH}	$\overline{OE}$ High Hold Time	0		0		0		ns
t_{OES}	$\overline{OE}$ High Setup Time	0		0		0		ns
t_{OZ}(4)	Output Enable to Output in High Z		15		20		25	ns

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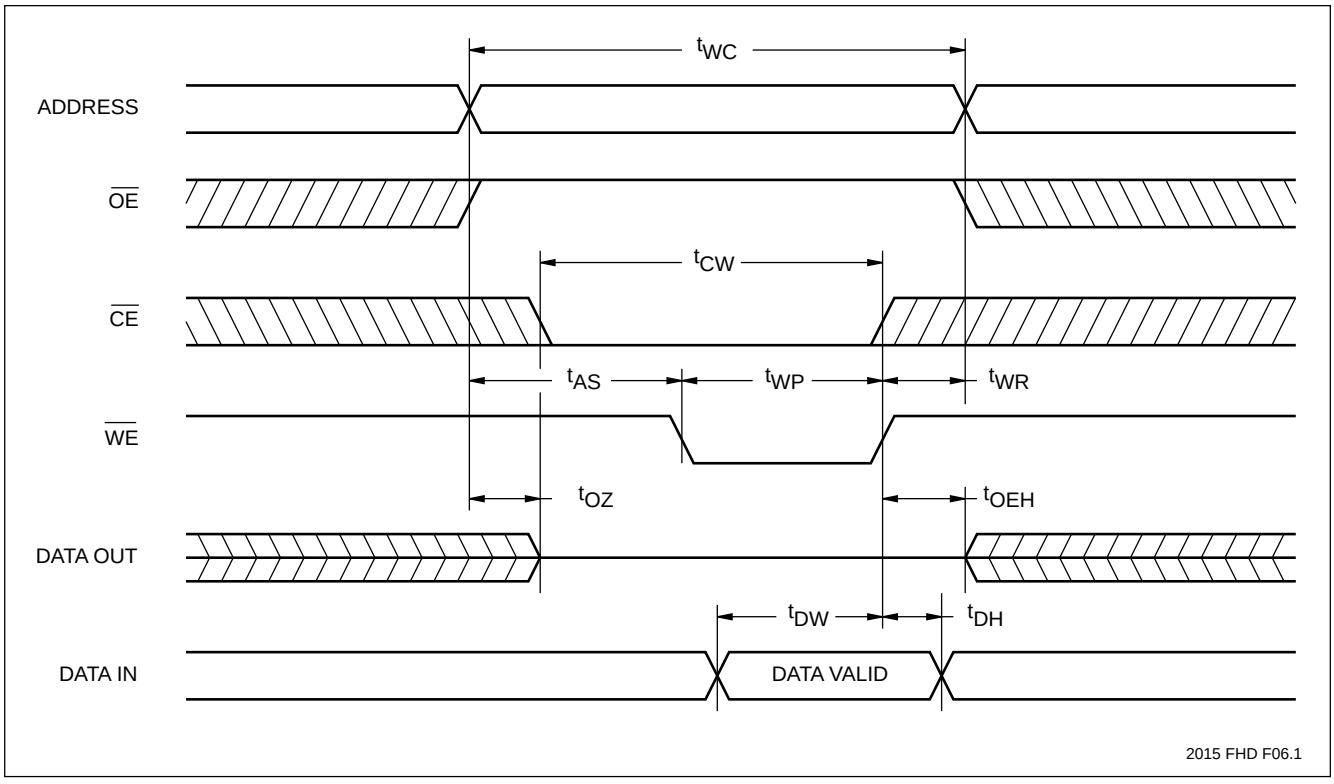
Write Cycle



2015 FHD F06.1

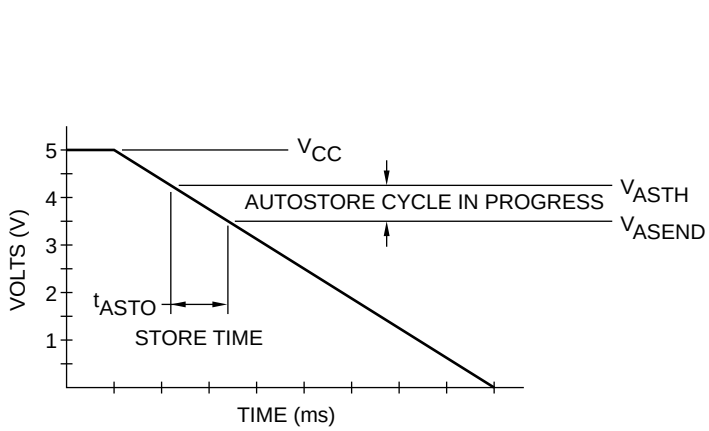
Note: (4) t_{OW}, t_{OZ} are periodically sampled and not 100% tested.

AUTOSTORE Feature

The AUTOSTORE feature automatically saves the contents of the X20C17's static RAM to the on-board bit-for-bit shadow E²PROM at power-down. This circuitry insures that no data is lost during accidental power-downs or general system crashes, and is ideal for microprocessor caching systems, embedded software systems, and general system back-up memory.

The X20C17 automatically initiates a nonvolatile store cycle whenever Vcc falls below the AUTOSTORE threshold voltage (V_{ASTH}). V_{CC} must remain above the AUTOSTORE Cycle End Voltage (V_{ASEND}) for the duration of the store cycle (t_{ASTO}). The detailed timing for this feature is illustrated in the AUTOSTORE timing diagram, below. Once the AUTOSTORE cycle is initiated, all other device functions are inhibited.

AUTOSTORE CYCLE Timing Diagram and Suggested AUTOSTORE Implementation Circuit



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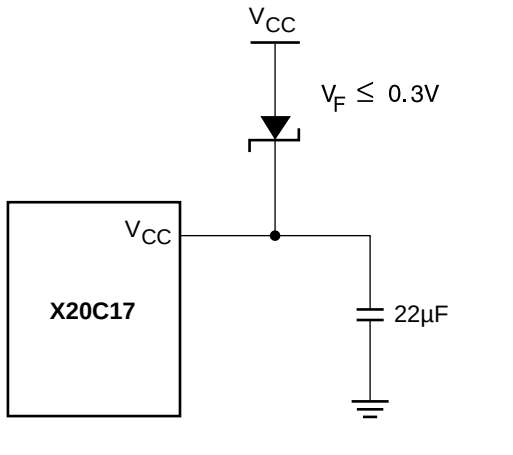


2015 ILL F30.4

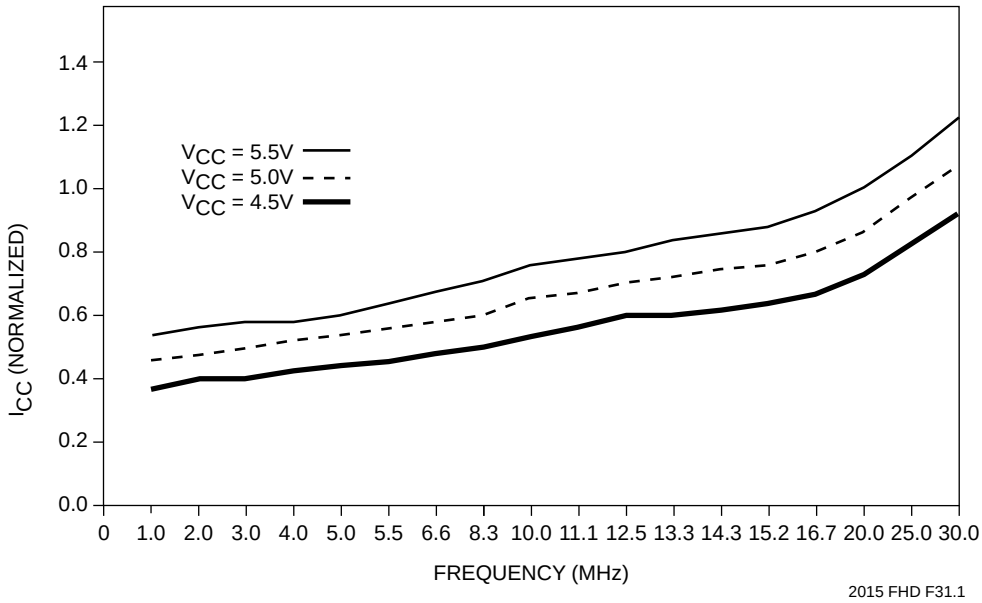
AUTOSTORE CYCLE LIMITS

Symbol	Parameter	X20C17		Units
		Min.	Max.	
t_{ASTO} (5)	AUTOSTORE Cycle Time		2.5	ms
V_{ASTH}	AUTOSTORE Threshold Voltage	4.0	4.3	V
V_{ASEND} (5)	AUTOSTORE Cycle End Voltage	3.5		V

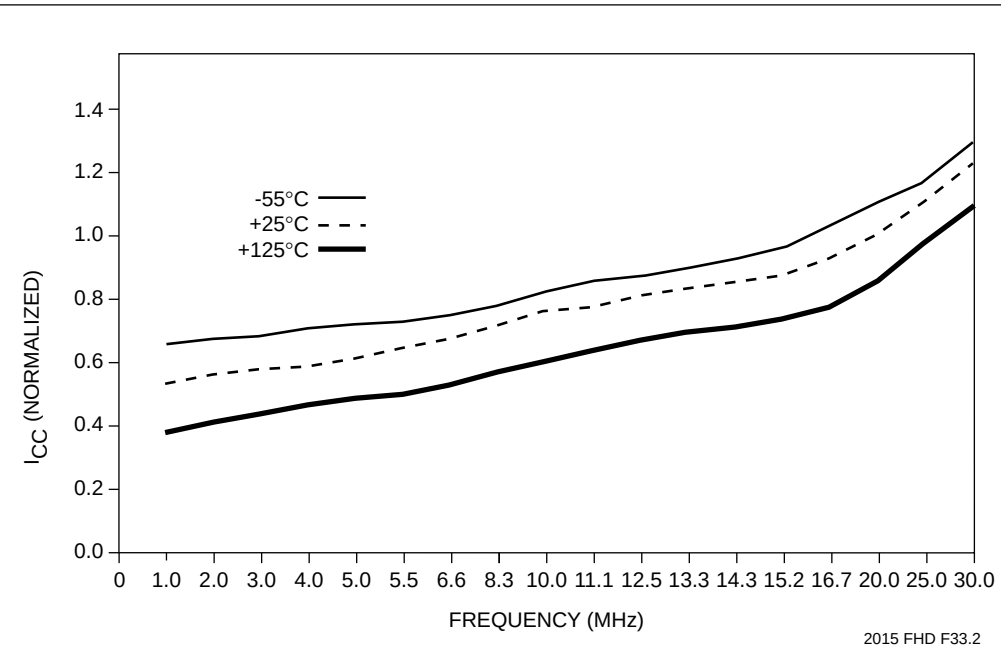
2015 PGM T15

Note: (5) t_{ASTO} and V_{ASEND} are periodically sampled and not 100% tested.

Normalized I_{CC} by Temperature over the V_{CC} Range and Frequency

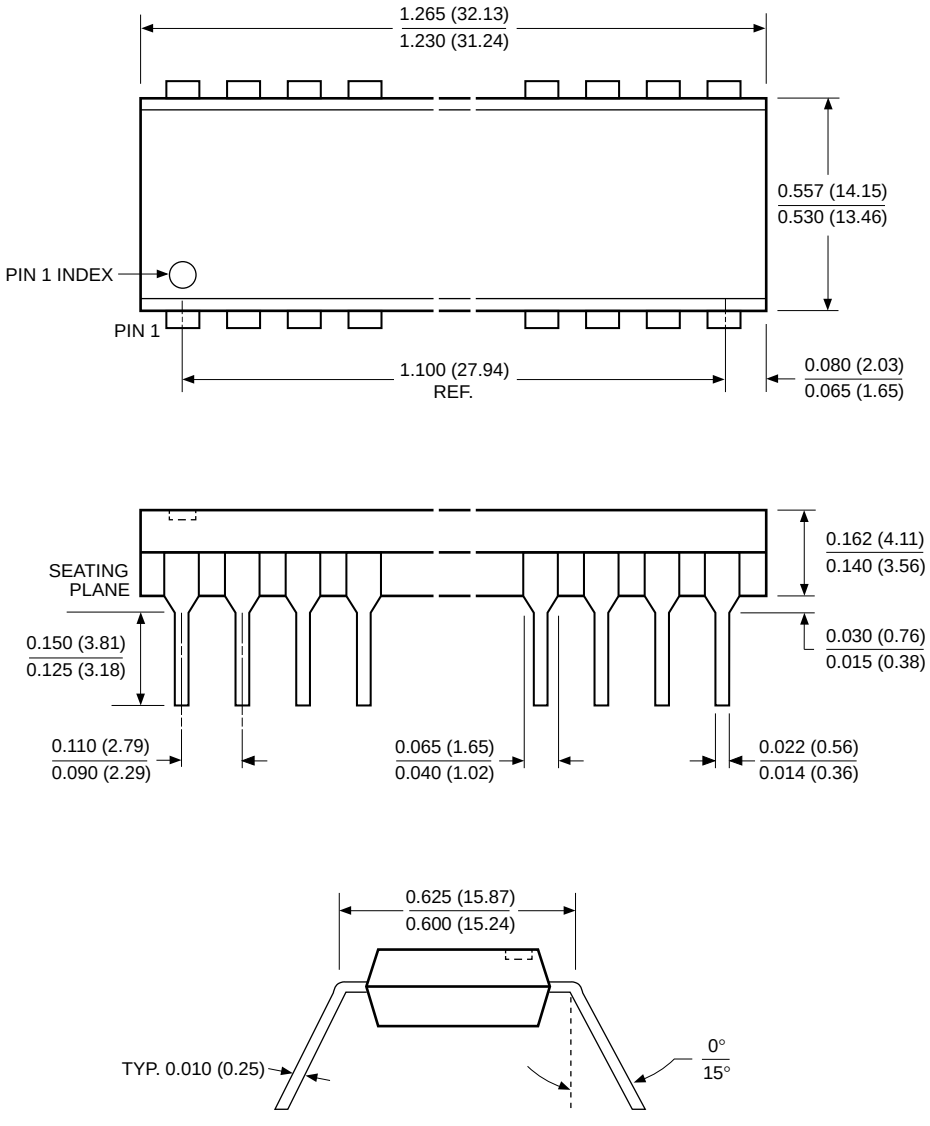


Normalized I_{CC} by Temperature over Frequency



PACKAGING INFORMATION

24-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

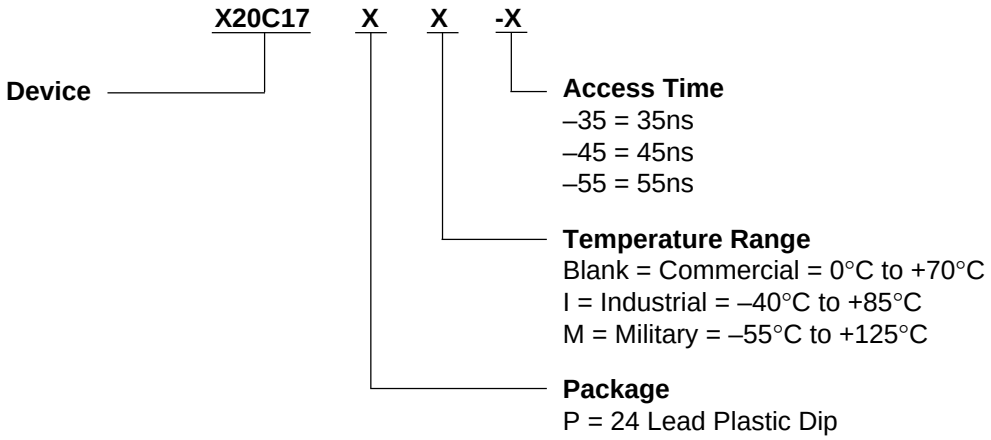


NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F03

ORDERING INFORMATION



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