# SONET/SDH/ATM CLOCK RECOVERY UNIT S3025

## FEATURES

- Complies with ANSI, Bellcore, and ITU-T specifications for jitter tolerance, jitter transfer and jitter generation
- On-chip high frequency PLL with internal loop filter for clock recovery
- Supports clock recovery for OC-12/STM-4 (622.08 Mbit/s) NRZ data
- 12.96 MHz reference frequency
- Lock detect—monitors run length and frequency
- 350mW typical power dissipation
- Low-jitter PECL interface
- On-chip crystal oscillator allows use of low cost reference crystal
- Micro-power Bipolar technology
- 5V supply
- Available in die form or 20 TSSOP package

## GENERAL DESCRIPTION

The function of the S3025 clock recovery unit is to derive high speed timing signals for SONET/SDH-based equipment. The S3025 is implemented using AMCC's proven Phase Locked Loop (PLL) technology.

The S3025 receives an OC-12/STM-4 scrambled NRZ signal and recovers the clock from the data. The chip outputs a differential PECL bit clock and retimed data.

The S3025 utilizes an on-chip PLL which consists of a phase detector, a loop filter, and a voltage controlled oscillator (VCO). The phase detector compares the phase relationship between the VCO output and the serial data input. A loop filter converts the phase detector output into a smooth DC voltage, and the DC voltage is input to the VCO whose frequency is varied by this voltage. A block diagram is shown in Figure 2.

***Figure 1. System Block Diagram***

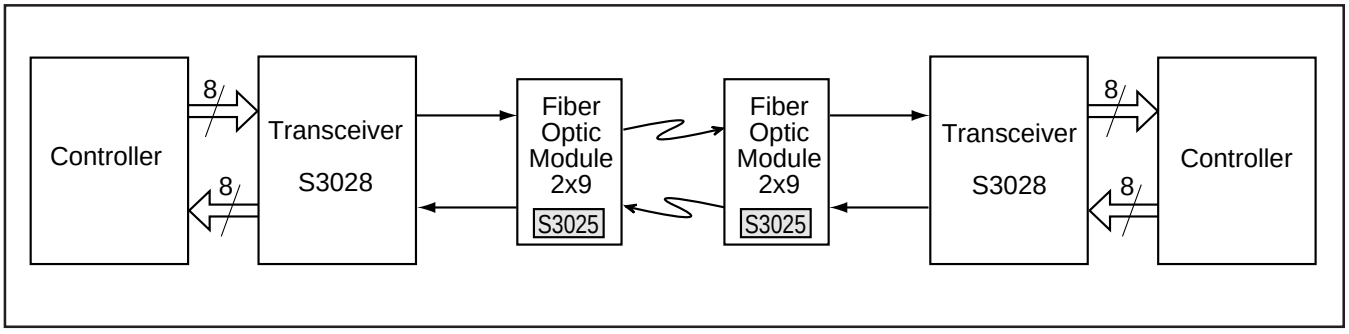
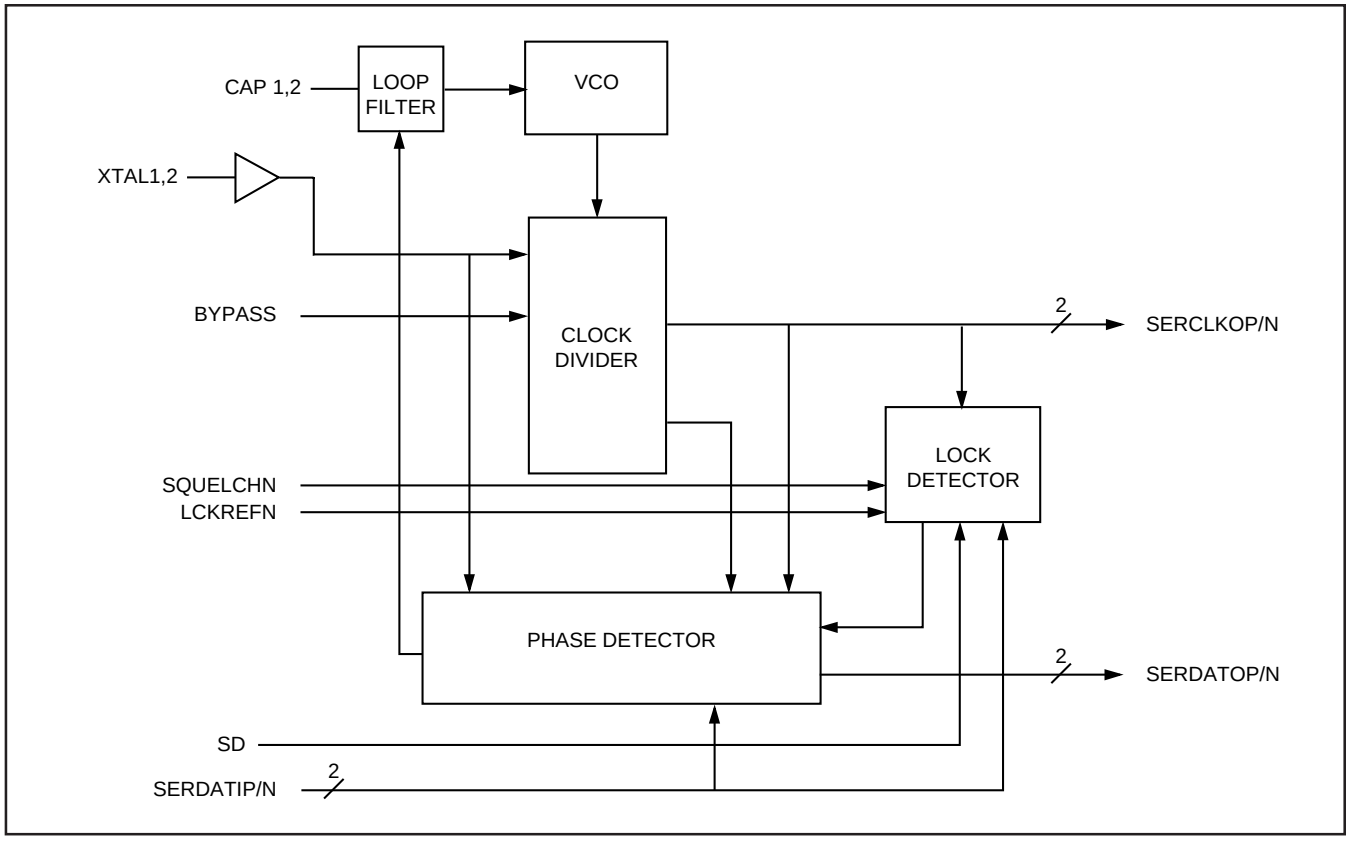


***Figure 2. Functional Block Diagram***



## OVERVIEW

The S3025 supports clock recovery for the OC-12/ STM-4 data rate. Differential serial data is input to the chip at the specified rate and clock recovery is performed on the incoming data stream. An external crystal is required to minimize the PLL lock time and provide a stable output clock source in the absence of serial input data. Retimed data and clock are output from the S3025.

## CHARACTERISTICS

### Performance

The S3025 PLL complies with the jitter specifications proposed for SONET/SDH equipment defined by the T1X1.6/91-022 document, when used with differential inputs and outputs as shown in Figure 3.

### Jitter Transfer

Jitter transfer functions is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. Jitter transfer requirements are shown in Figure 5. The measurement condition is that input sinusoidal jitter up to the mask level in Figure 4 be applied for each of the OC-N/STS-N rates.

### Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. SONET input jitter tolerance requirements are shown in Figure 4. The measurement condition is the input jitter amplitude which causes an equivalent of 1 dB power penalty.

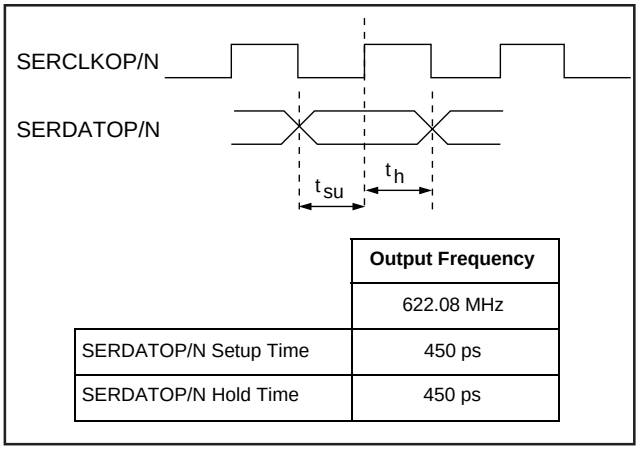
### Serial Data Output Set-up and Hold Time

The output set-up and hold times are represented by the waveforms shown in Figure 3.

### Jitter Generation

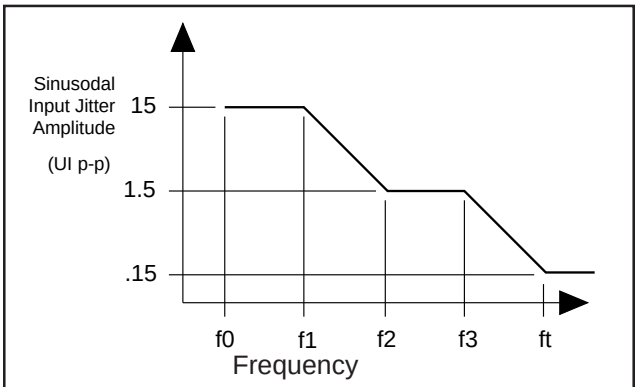
The jitter of the serial clock and serial data outputs shall not exceed .01 U.I. when a serial data input with less than 14ps rms jitter is presented to the serial data inputs.

***Figure 3. Clock Output to Data Transition Delay***



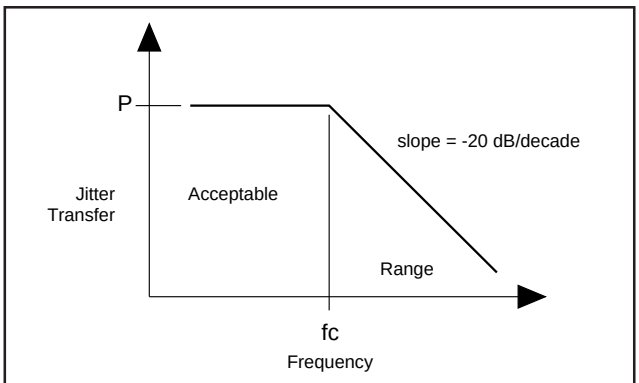

| | Output Frequency |
|---|---|
| | 622.08 MHz |
| SERDATOP/N Setup Time | 450 ps |
| SERDATOP/N Hold Time | 450 ps |

***Figure 4. Input Jitter Tolerance Specification***




| OC/STS Level | f0 (Hz) | f1 (Hz) | f2 (Hz) | f3 (kHz) | ft (kHz) |
|---|---|---|---|---|---|
| 12 | 10 | 30 | 300 | 25 | 250 |

***Figure 5. Jitter Transfer Specification***



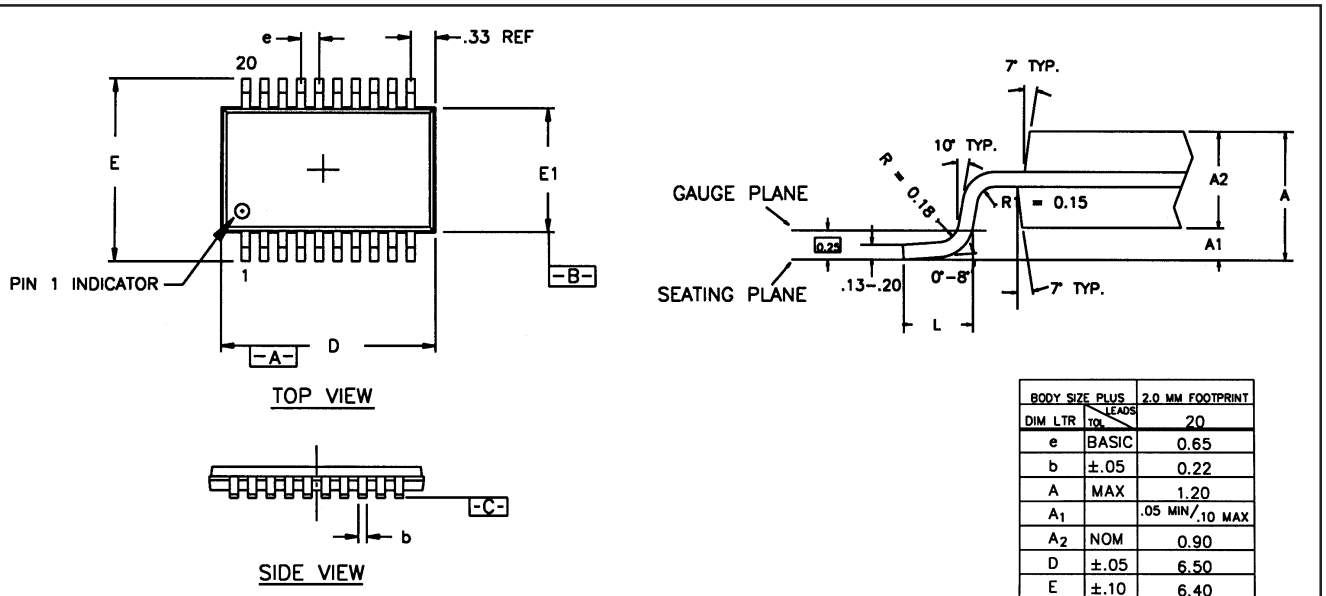

| OC/STS Level | fc (kHz) | P (dB) |
|---|---|---|
| 12[1,2] | 500 | 0.1 |

1. Bellcore Specifications: TR-NWT-000253, Issue 2, December 1991.
2. CCITT Recommendations: G.958.

***S3025 Pin Assignment and Descriptions***

| Pin Name | Level | I/O | Pin # | Description |
|---|---|---|---|---|
| SERDATIP<br>SERDATIN | Diff.<br>PECL | I | 2<br>3 | Serial data in. A clock is recovered from transitions on these inputs. |
| BYPASS | TTL | I | 16 | Bypass enable, active high. Used during production test to bypass the VCO in the PLL. Tie to ground for normal operation. |
| SD | PECL | I | 15 | Signal detect, active high. A single-ended 10K PECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SD is inactive, the PLL will be forced to lock to the XTAL1, 2 inputs and the SERDATOP/N output will be held in the logic low state. See Table 1. When SD is active, data on the SERDATIP/N pins will be processed normally. |
| XTAL1<br>XTAL2 | Analog | I | 6<br>7 | External crystal. A series resonant crystal is connected to these pins. The crystal is used to establish the initial operating frequency of the clock recovery PLL and also is used as a standby clock in the absence of data or during reset. |
| CAP1<br>CAP2 | – | I | 18<br>17 | The loop filter capacitor is connected to these pins. The capacitor value should be 1.0µf ±10% tolerance, X7R dielectric. |
| SQUELCHN | TTL | I | 5 | Clock squelch, active low. When active, the serial clock output will be forced to lock to the local reference clock input [XTAL1,2] and the SERDATOP/N output will be held in the logic low state. See Table 1. |
| LCKREFN | TTL | I | 8 | Lock to reference, active low. When active, the serial clock output will be forced to lock to the local reference clock input [XTAL1,2]. |
| SERDATOP<br>SERDATON | Diff.<br>PECL | O | 14<br>13 | Serial data out signal that is the delayed version of the incoming data stream (SERDATI) updated on the falling edge of Serial Clock Out (SERCLKOP). |
| SERCLKOP<br>SERCLKON | Diff.<br>PECL | O | 12<br>11 | Serial clock out signal that is phase aligned with Serial Data Out (SERDATOP/N). (See Figure 3.) |
| DGND | GND | | 9 | Digital Ground (0V) |
| DVCC | +5V | | 10 | Digital Power Supply (+5V) |
| AGND | GND | | 4, 19 | Analog Ground (0V) |
| AVCC | +5V | | 1, 20 | Analog Power Supply (+5V) |

***Figure 6. S3025A TSSOP Package***




| BODY SIZE PLUS LEADS / DIM LTR / TOL. | | 2.0 MM FOOTPRINT 20 |
|---|---|---|
| e | BASIC | 0.65 |
| b | ±.05 | 0.22 |
| A | MAX | 1.20 |
| $A_1$ | | .05 MIN/.10 MAX |
| $A_2$ | NOM | 0.90 |
| D | ±.05 | 6.50 |
| E | ±.10 | 6.40 |
| $E_1$ | ±.10 | 4.40 |
| L | ±.15 | 0.60 |

All dimensions are in mm.

***Table 1. Clock Squelch Enable Function***

| | | | SQUELCHN ACTIVE | | SQUELCHN INACTIVE | |
|---|---|---|---|---|---|---|
| **SD** | **LCKREFN** | ***LOCK DETECT** | **SERCLKOP/N** | **SERDATP/N** | **SERCLKOP/N** | **SERDATP/N** |
| X | X | 0 | 0 | — | Active | 0 |
| X | 0 | X | 0 | 0 | Active | 0 |
| 0 | X | X | 0 | 0 | Active | 0 |
| 1 | 1 | 1 | Active | Active | Active | Active |

1. LOCKDET is not a pin. This column indicates the state of the internal Lock Detect state machine. (See Lock Detect description.)

***Performance Specifications***

| Parameter | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|
| Nominal VCO Center Frequency | | 622.08 | | MHz | |
| Reference Clock Frequency Tolerance Clock Recovery[1] | -250 | | +250 | ppm | |
| OC-12/STS-12 Capture Range | | ±500ppm | | | With respect to fixed reference frequency |
| Clock Output Duty Cycle | 45 | | 55 | % of UI | Minimum transition density of 20% |
| Acquisition Lock Time[1] OC-12/STS-12 | | | 16 | µsec | With device already powered up and valid REFCLK. |
| PECL Output Rise & Fall Times | | | 600 | ps | 10% to 90%, 50 to -2V equivalent load, 5 pf cap |
| SERCLKOP/N Jitter Generation | | .005 | .01 | U.I. | With less than 14ps rms jitter on SERDATIP/N data inputs |
| OC-12/STS-12 Jitter Tolerance[1] | 0.5 | | | U.I. | Sinusoidal input jitter. Amplitude on SERDATIP/N data inputs from 250KHz to 5MHz. |

1. Guaranteed but not tested.

***Absolute Maximum Ratings***

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Case Temperature under Bias | -55 | | +125 | ° C |
| Junction Temperature under Bias | -55 | | +150 | ° C |
| Storage Temperature | -65 | | +150 | ° C |
| Voltage on VCC with Respect to GND | -0.5 | | +7.0 | V |
| Voltage on any TTL Input Pin | -0.5 | | +5.5 | V |
| Voltage on any PECL Input Pin | VCC -2.0 | | VCC | V |
| TTL Output Sink Current | | | 20 | mA |
| TTL Output Source Current | | | 10 | mA |
| High Speed PECL Output Source Current | | | 50 | mA |
| Static Discharge Voltage | | 500 | | V |

***Recommended Operating Conditions***

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Ambient Temperature under Bias (industrial) | -40 | | +85 | ° C |
| Ambient Temperature under Bias (commercial) | 0 | | +70 | ° C |
| Junction Temperature under Bias | -10 | | +130 | ° C |
| Voltage on VCC with Respect to GND | 4.75 | 5.0 | 5.25 | V |
| Voltage on Any TTL Input Pin | 0.0 | | VCC | V |
| Voltage on Any PECL Input Pin | VCC -2 | | VCC | V |
| PECL Output Source Current (50 to Vcc-2V) | | 14 | 25 | mA |
| ICC Supply Current | | 70 | 100 | mA |

### *TTL Input/Output DC Characteristics*[2]

($T_A$ = -40°C to +85°C, $V_{CC}$ = 5 V ±5%)

| Symbol | Parameter | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IL}$[1] | Input LOW Voltage | Guaranteed Input LOW Voltage for all inputs | | 0.8 | Volts |
| $V_{IH}$[1] | Input HIGH Voltage | Guaranteed Input HIGH Voltage for all inputs | 2.0 | | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.5V | -400.0 | | uA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V | | 50.0 | uA |
| $I_I$ | Input HIGH Current at Max VCC | $V_{CC}$ = MAX, $V_{IN}$ = 5.25V | | 1.0 | mA |
| $I_{OS}$ | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.5V | -100.0 | -25.0 | mA |
| $V_{IK}$ | Input Clamp Diode Voltage | $V_{CC}$ = MIN, $I_{IN}$ = -18.0mA | -1.2 | | Volts |
| $V_{OL}$ | TTL Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 8mA | | 0.5 | Volts |
| $V_{OH}$ | TTL Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = -1.0mA | 2.4 | | Volts |

1. These input levels provide a zero–noise immunity and should only be tested in a static, noise-free environment.

### *PECL Input/Output DC Characteristics*

($T_A$ = -40°C to +85°C, $V_{CC}$ = 5 V ±5%)

| Symbol | Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ -2.000 | | $V_{CC}$ -1.441 | Volts | Guaranteed Input LOW Voltage for single-ended inputs |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ -1.225 | | $V_{CC}$ -0.570 | Volts | Guaranteed Input HIGH Voltage for single-ended inputs |
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ -2.000 | | $V_{CC}$ -0.700 | Volts | Guaranteed Input LOW Voltage for differential inputs |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ -1.750 | | $V_{CC}$ -0.450 | Volts | Guaranteed Input HIGH Voltage for differential inputs |
| $V_{ID}$ | Input Diff. Voltage | 0.250 | 0.500 | 1.400 | Volts | Differential Input Voltage |
| $I_{IH}$ | Input High Current | -0.500 | | 20.000 | µA | $V_{ID}$ = 500mV |
| $I_{IL}$ | Input Low Current | -0.500 | | 20.000 | µA | $V_{ID}$ = 500mV |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ -2.000 | | $V_{CC}$ -1.500 | Volts | 50 ohm termination to $V_{CC}$ -2V |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ -1.110 | | $V_{CC}$ -0.670 | Volts | 50 ohm termination to $V_{CC}$ -2V |
| $V_{OD}$ | Output Diff. Voltage | 0.390 | | 1.330 | Volts | Differential Output Voltage |

### *External Series Resonant Crystal Specifications*

| Parameter | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|
| Frequency | | 12.96 | | MHz | |
| Accuracy | -500 | | +500 | ppm | |

***Ordering Information***

| GRADE | PART | PACKAGE |
|---|---|---|
| S-commercial/ Industrial | 3025 | A – 20 TSSOP |

**X** Grade **XXXX** Part number – **X** Package

ISO 9001 CERTIFIED

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