SONY

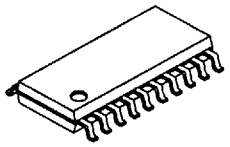
CXA1380M/N

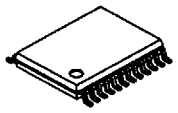
ADIP Demodulator for MiniDisc

Description

The CXA1380M/N can be used to read the ADIP (Address In Pre-groove) signal stamped in MiniDiscs.

20 pin SOP (Plastic) 24 pin SSOP (Plastic)





Features

- ADIP FM demodulator
- ADIP defect protection circuit
- ADIP data clock regeneration circuit
- Generate of FG (Frequency Generator) signal used to CLV (Constant Linea Velocity) servo control, rough mode and standard mode.
  When used in conjunction with the CXA1381, CXD2525, and others, the CXA1380 can decode address data from wobbled pre-groove on recordable discs.

Applications

Reproduceing the binary data from the ADIP signal in Mini Discs. The binary data is used for controling motor and include address information.

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	7	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation			
CXA1380M	P_D	700	mW
CXA1380N	P_D	620	mW

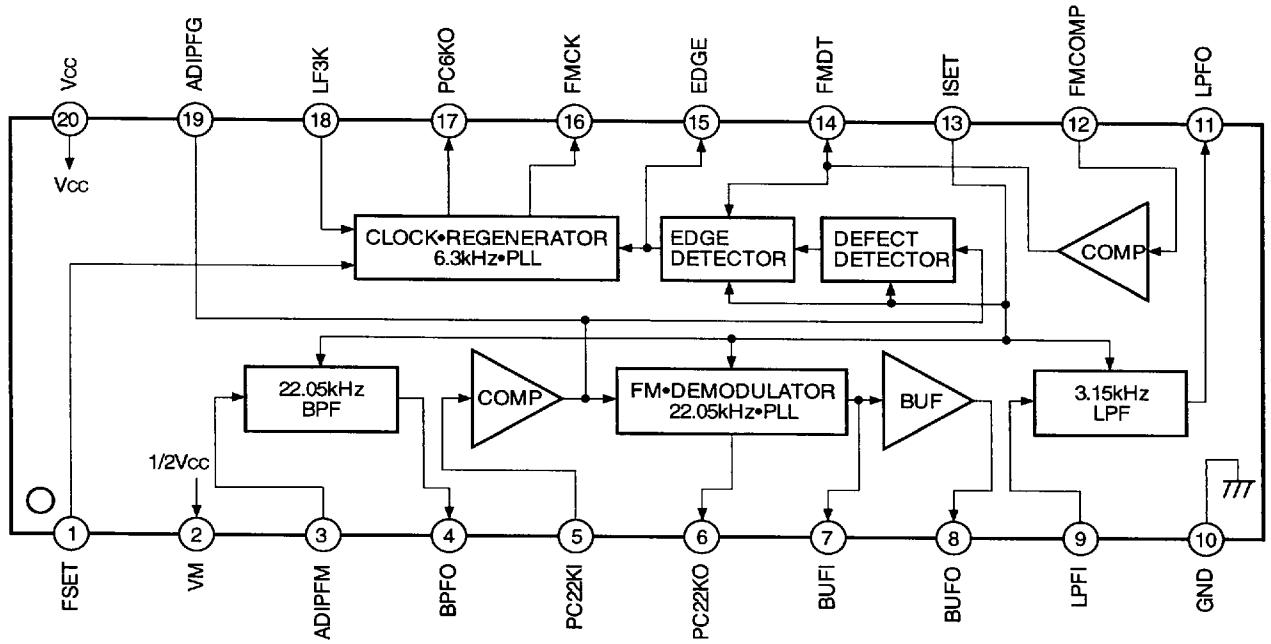
Operating Conditions

• Supply voltage	V_{CC}	3.6 to 5	V

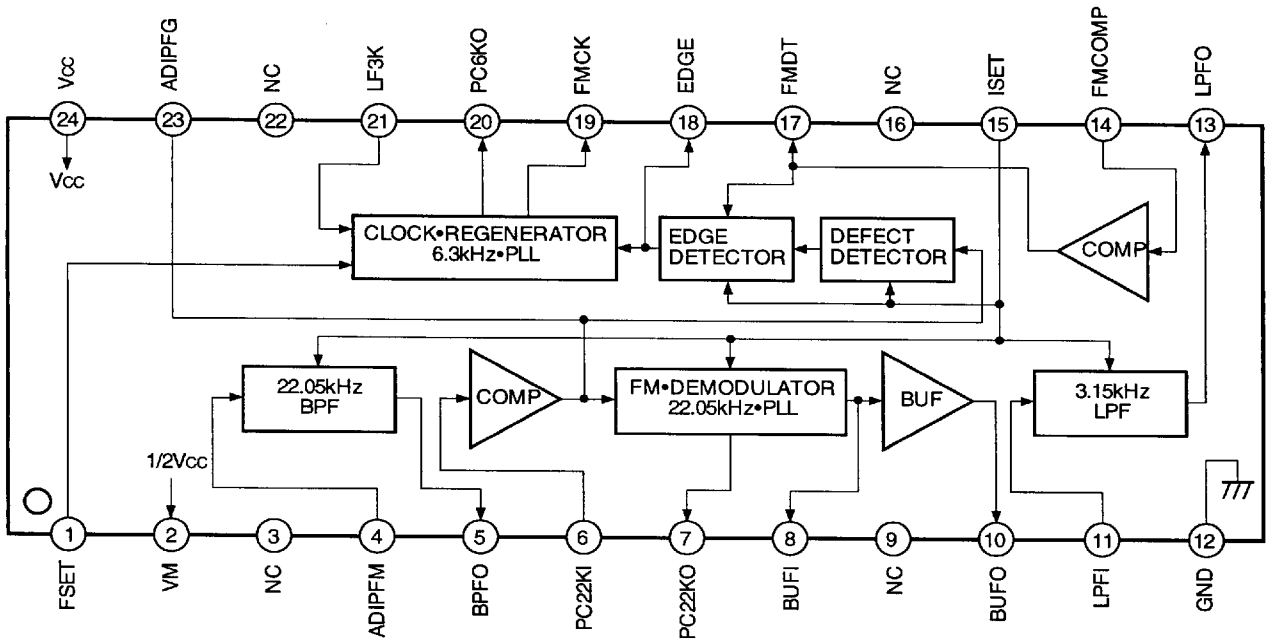
E92008A58-PP

Block Diagram and Pin Configuration

CXA1380M

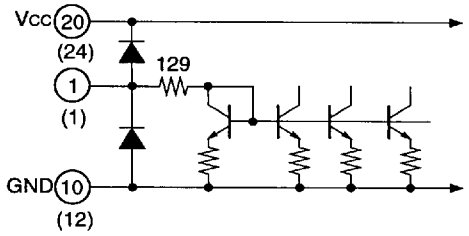
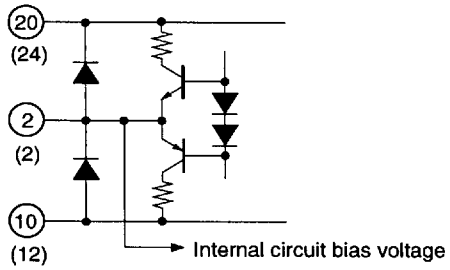
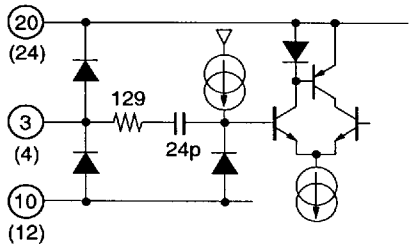
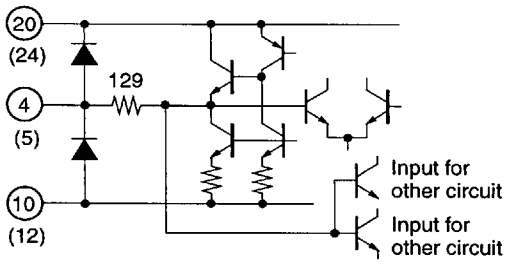
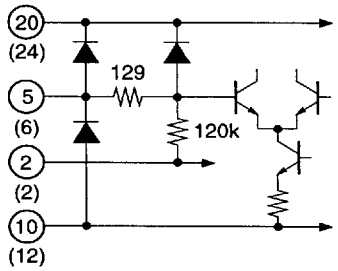


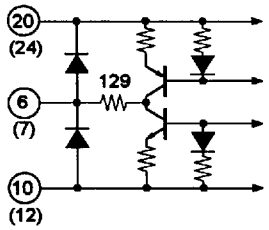
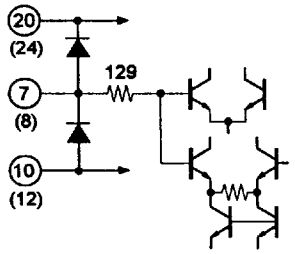
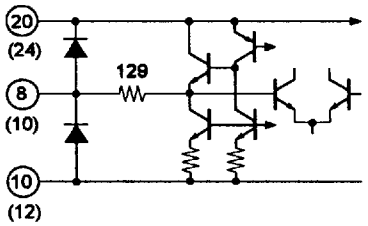
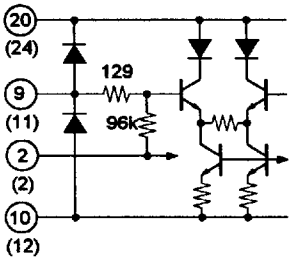
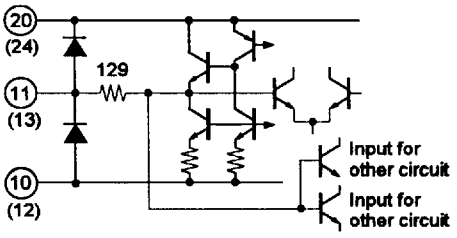
CXA1380N

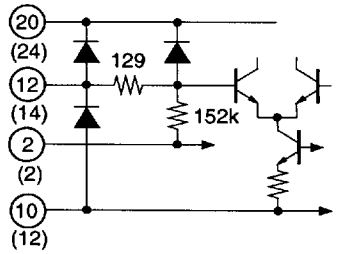
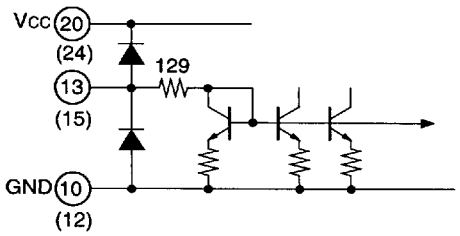
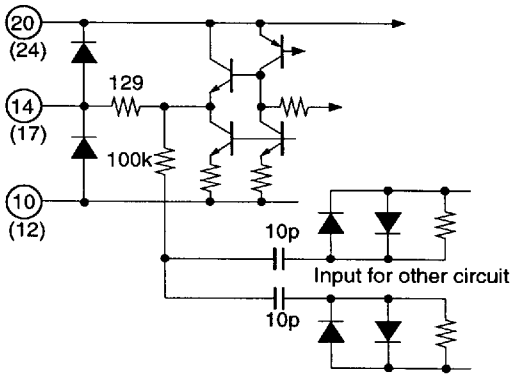
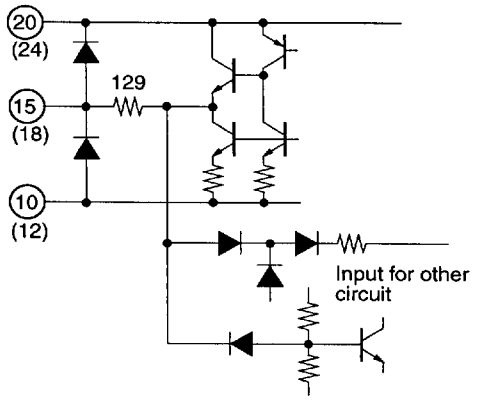


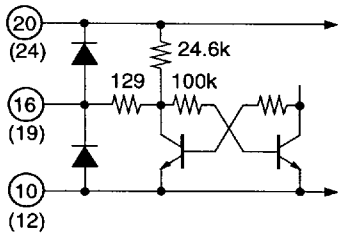
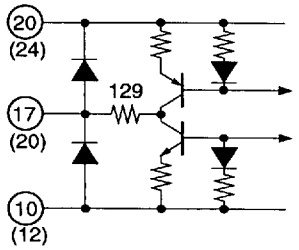
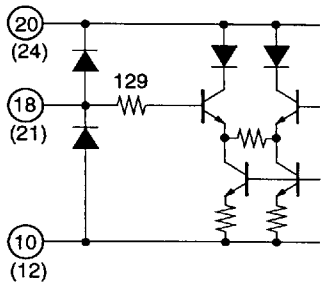
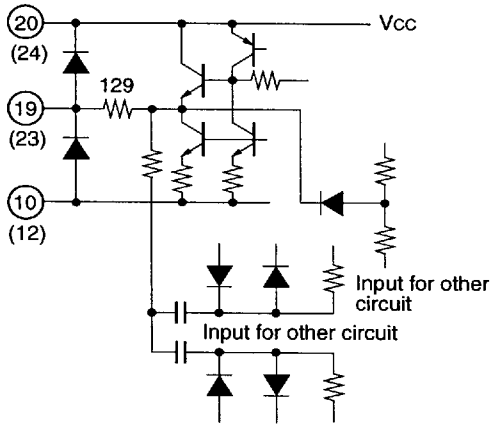
Pin Description

The pin numbers are for the CXA1380M. The pin numbers given in parentheses are for the CXA1380N.

Pin No.	Symbol	Typical voltage	Equivalent Circuit	Description
1 (1)	FSET	720mV		Setting a free running frequency of VCO used for ADIP bit clock regenerator.
2 (2)	VM	2.5V		1/2 Vcc voltage output. Internal circuit bias voltage.
(3)	NC	OPEN		No connected.
3 (4)	ADIP FM	450mVp-p		ADIP FM signal input.
4 (5)	BPFO	1Vp-p +2.5V		Band-pass filter output.
5 (6)	PC22KI	1Vp-p +2.5V		Phase comparator input for FM demodulation. Connecting to BPFO (Pin 4 (5)) through the capacitor.

Pin No.	Symbol	Typical voltage	Equivalent Circuit	Description
6 (7)	PC22KO	Digital output		Phase comparator output for FM demodulation.
7 (8)	BUFI	0.8Vp-p +2.5V		PLL feedback for FM demodulation. Signal comes from PC22KO (Pin 6 (7)) through PLL's loop filter.
(9)	NC	OPEN		No connected.
8 (10)	BUFO	0.8Vp-p +2.5V		FM demodulation signal output.
9 (11)	LPFI	0.8Vp-p +2.5V		Low-pass filter input. Connecting to BUFO (Pin 8 (10)) through the capacitor.
10 (12)	GND	0V		GND.
11 (13)	LPFO	0.15Vp-p +2.5V		Low-pass filter output.

Pin No.	Symbol	Typical voltage	Equivalent Circuit	Description
12 (14)	FM COMP	0.15Vp-p +2.5V		ADIP data comparator input. Connecting to LPFO (Pin 11 (13)) through the capacitor.
13 (15)	ISET	720mV		Setting the constants below. • Band-pass filter fo • Low-pass filter fc • Free running frequency of VCO used for FM demodulation. • Edge pulse width • Defect pulse width
(16)	NC	OPEN		No connected.
14 (17)	FM DT	Digital output		ADIP data output.
15 (18)	EDGE	Digital output		Output for Gather edge used for ADIP data signal.

Pin No.	Symbol	Typical voltage	Equivalent Circuit	Description
16 (19)	FMCK	Digital output		ADIP bit clock output.
17 (20)	PC6KO	Digital output		Phase comparator output for ADIP bit clock regenerator.
18 (21)	LF3K	0.2Vp-p +2.5V		PLL feedback for ADIP bit clock regenerator. Signal comes from PC6KO (Pin 17 (20)) through PLL's loop filter).
(22)	NC	OPEN		No connected.
19 (23)	ADIPFG	Digital output		ADIP FM binary data output.
20 (24)	Vcc	5V		Power supply.

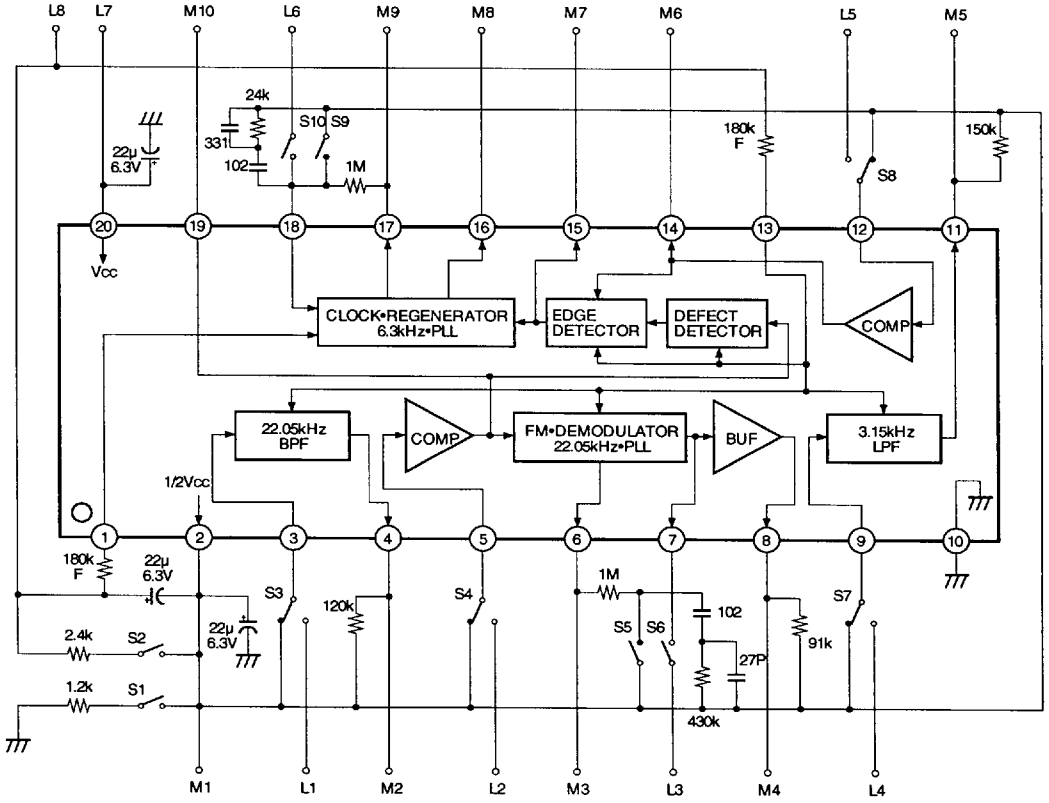
Electrical Characteristics (V_{CC} = 5V, Ta = 25°C)

No.		Item	Symbol	Switch conditions O: ON										Input						Output		Limit			
				S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	Supply		Input A		Input B				Min.	Typ.	Max.	Unit
1		Current consumption	I_{CC}											L7 5V	L8 5V					L7	No input	3.5	6	9	mA
2	Center Voltage	Output voltage	V_{MO}											↓	↓					M1	No load	2.45	2.5	2.55	V
3	Center Voltage	Output current 1	V_{M1}	O										↓	↓					M1	SORCE Down 50mV for V_{MO}	2	4.5		mA
4	Center Voltage	output current 2	I_{M2}		O									↓	↓					M1	SINK Up 50mV for V_{MO}	1	3		mA
5	BPF	Voltage gain	G_{BPF}			O								↓	↓	L1	f = 22.05kHz, SINE 0.7Vp-p+2.5V			M2	I/O gain	6	8.5	11	dB
6	BPF	Frequency response 1	F_{BPF1}			O								↓	↓	L1	f = 16kHz, SINE 0.7Vp-p+2.5V			M2	I/O gain – G_{BPF}	–10	–6.3	–2.5	dB
7	BPF	Frequency response 2	F_{BPF2}			O								↓	↓	L1	f = 30kHz, SINE 0.7Vp-p+2.5V			M2	I/O gain – G_{BPF}	–11	–6.7	–3	dB
8	BPF	Output swing	V_{BPF0}			O								↓	↓	L1	f = 22.05kHz, SINE offset = V_{MO}			M2	THD 5%	3.2	3.4		Vp-p
9	22K • COMP	Operating input voltage	V_{FGIN}				O							↓	↓	L2	f = 22.05kHz, SINE offset = V_{MO}			M10	Operating input voltage range 	50			mVp-p
10	22K • COMP	Output voltage 1	V_{FGOH}				O							↓	↓	L2	2.3V			M10		4	4.25		V
11	22K • COMP	Output voltage 2	V_{FGOL}				O							↓	↓	L2	2.7V			M10			300	600	mV
12	FM • DEMOD	Free-running frequency	F_{DMD0}				O	O	O					↓	↓	L2	2.7V	L3	V_{MO}	M3		18	22	25	kHz
13	FM • DEMOD	Frequency alteration 1	F_{DMD1}				O	O	O					↓	↓	L2	2.7V	L3	V_{MO} +0.5V	M3	Variation for F_{DMD0}	25	30	35	%
14	FM • DEMOD	Frequency alteration 2	F_{DMD2}				O	O	O					↓	↓	L2	2.7V	L3	V_{MO} –0.5V	M3	Variation for F_{DMD0}	–36	–32	–26	%
15	BUFFER	Voltage gain	G_{BUF}					O	O					↓	↓	L3	f = 3.15kHz, SINE 0.5Vp-p+2.5V			M4	Output/Input	0.944	1	1.059	
16	BUFFER	Output swing	V_{BUF0}					O	O					↓	↓	L3	f = 3.15kHz, SINE offset = V_{MO}			M4	THD 1%	3.4	3.6		Vp-p

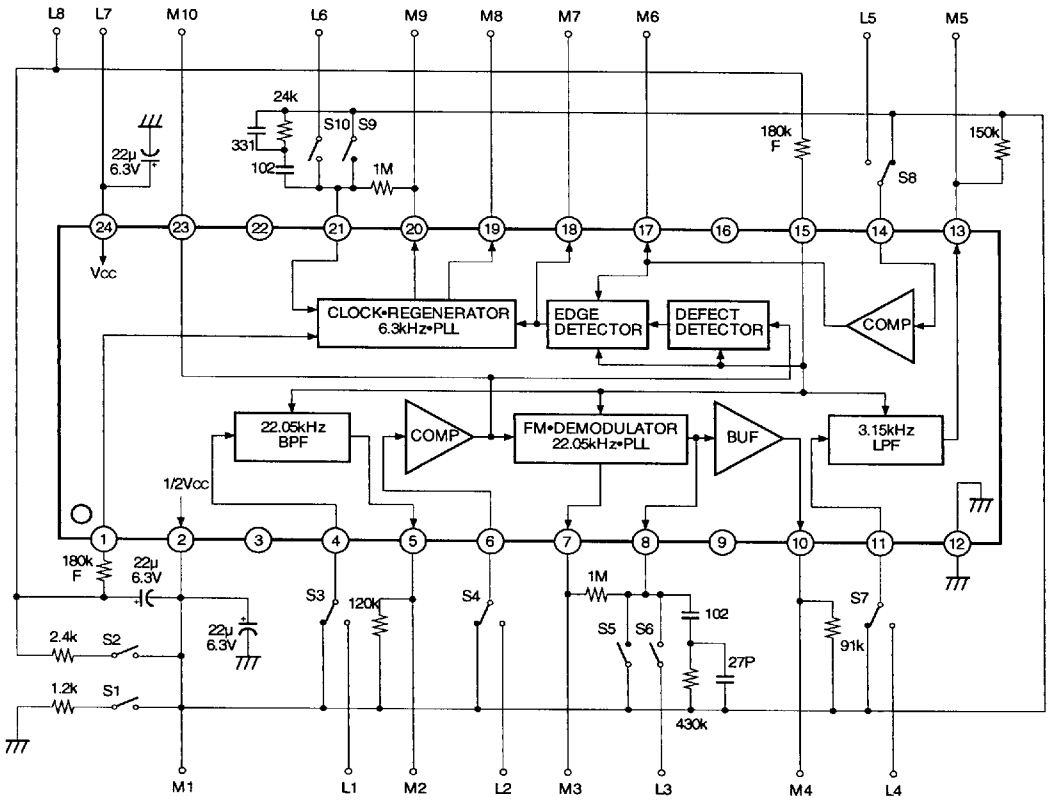
No.	Item		Symbol	Switch conditions O: ON										Input						Output		Limit			
				S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	Supply		Input A		Input B				Min.	Typ.	Max.	Item
17	LPF	Voltage gain	GLPF							O				L7 5V	L8 5V	L4	f = 500Hz, SINE 0.5Vp-p+2.5V			M5	I/O gain	–2.5	–0.4	1.0	dB
18		Frequency response	FLPF							O				↓	↓	L4	f = 3.8kHz, SINE 0.5Vp-p+2.5V			M5	I/O gain – GLPF	–6	–2.5	0	dB
19		Output swing	VLPFO							O				↓	↓	L4	f = 3.15kHz, SINE offset = VMO			M5	THD 5%	2.7	2.9		Vp-p
20	3K • COMP	Operating input voltage	VDTIN								O			↓	↓	L5	f = 3.15kHz, SINE offset = VMO			M6	Operating input voltage range	40			mVp-p
21		Output voltage 1	VDTOH								O			↓	↓	L5	2.3V			M6		4	4.25		V
22		Output voltage 2	VDTOL								O			↓	↓	L5	2.7V			M6			10	200	mV
23	EDGE	Edge width-1	TEDGE1				O				O			↓	↓	L2	f = 22kHz, SINE 0.7Vp-p+2.5V	L5	VMO, 0.5Vp-p, 65µs	M7	L5 negative VMO crossing M7 negative going	60	81	110	µs
24		Edge width-2	TEDGE2				O				O			↓	↓	L2	f = 22kHz, SINE 0.7Vp-p+2.5V	L5	65µs, VMO, 0.5Vp-p	M7	L5 positive VMO crossing M7 negative going	60	81	110	µs
25		Carrier frequency	FCAR				O				O			↓	↓	L2	f • Sweep SINE 0.7Vp-p+2.5V	L5	f = 3.15kHz, SINE 0.5Vp-p+2.5V	M7	Operating frequency range	15	22.05		kHz
26	CLOCK REGEN	Free-running frequency	FCLKO								O	O	O	↓	↓	L5	2.7V	L6	VMO	M8		5.7	6.3	6.8	kHz
27		Frequency alteration 1	FCLK1								O	O	O	↓	↓	L5	2.7V	L6	VMO+0.5V	M8	Variation for FCLKO	28	34	38	%
28		Frequency alteration 2	FCLK2								O	O	O	↓	↓	L5	2.7V	L6	VMO–0.5V	M8	Variation for FCLKO	–38	–34	–28	%

Measurement Circuit

CXA1380M

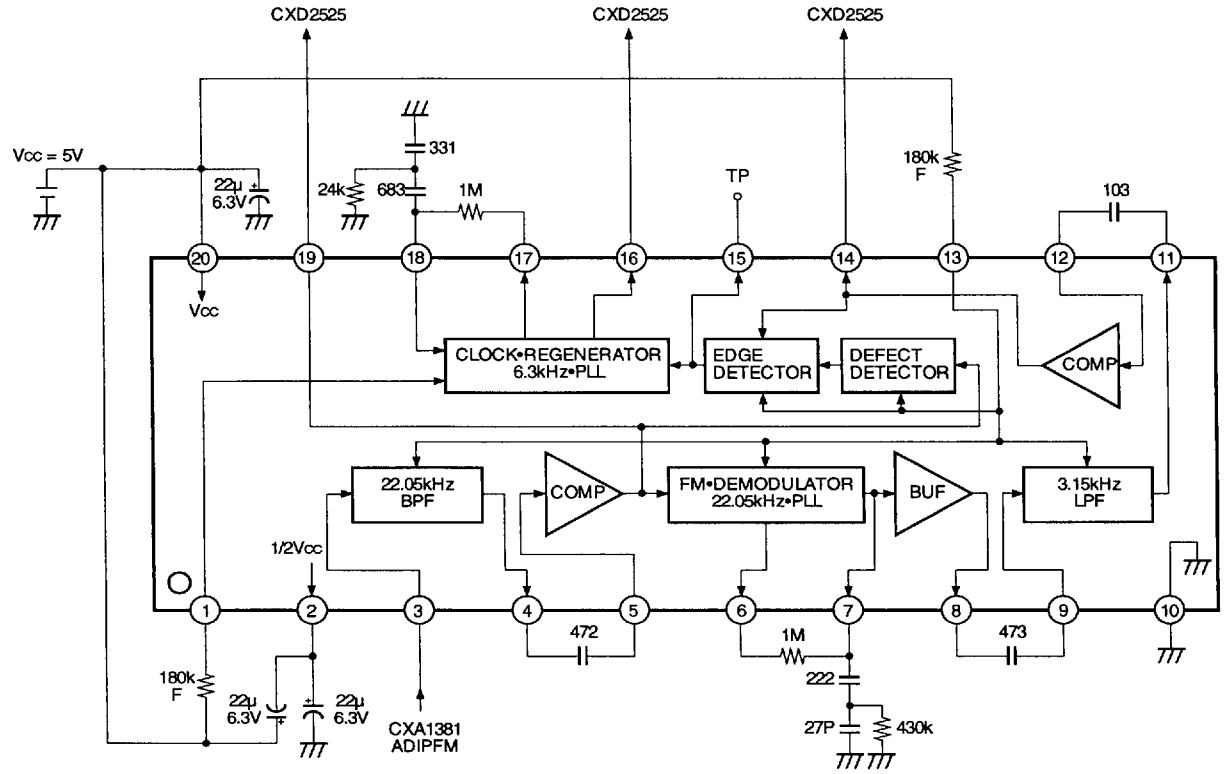


CXA1380N

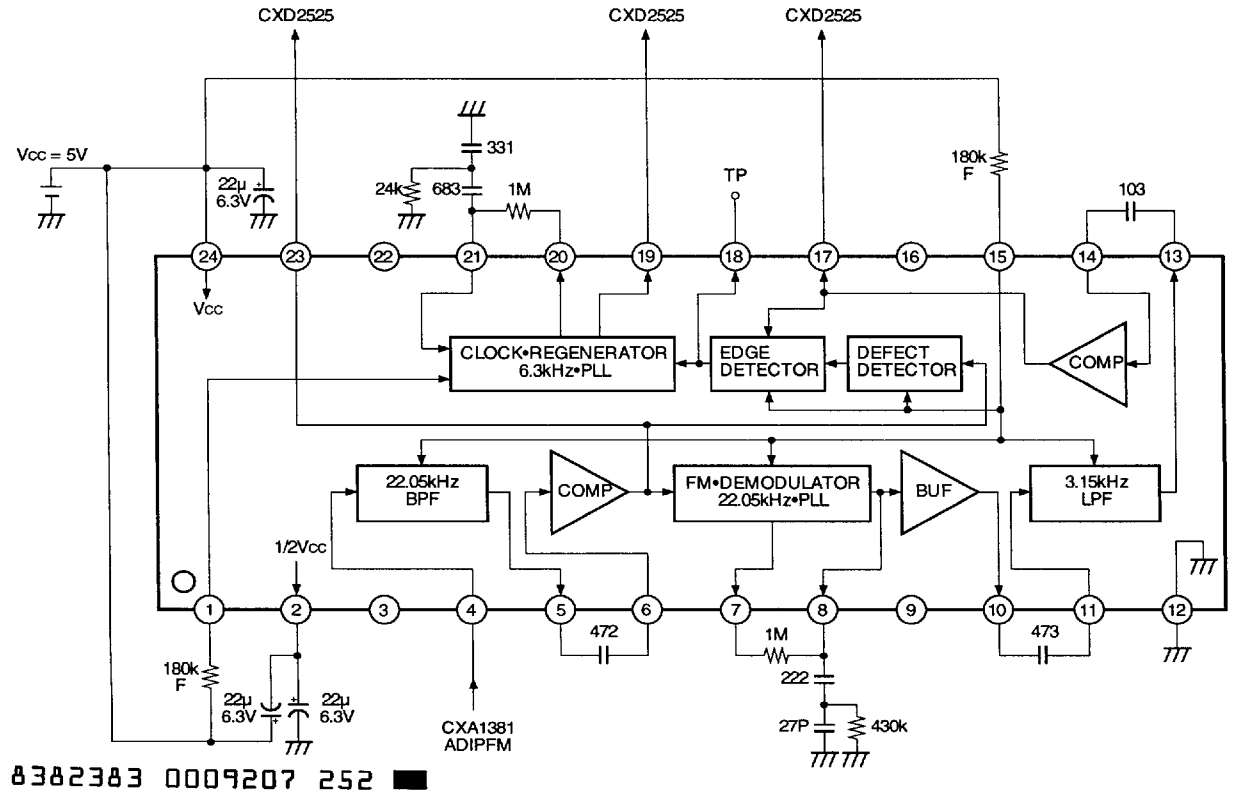


Application Circuit

CXA1380M



CXA1380N

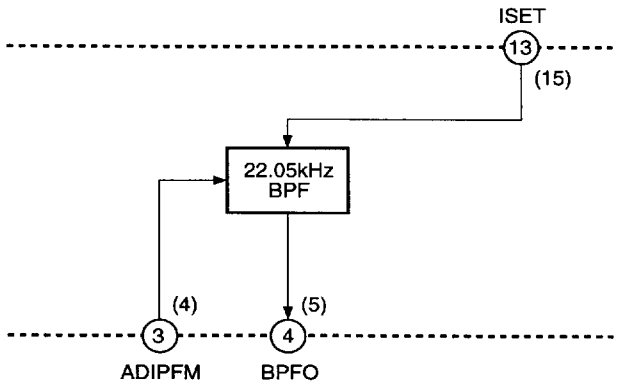


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Functions

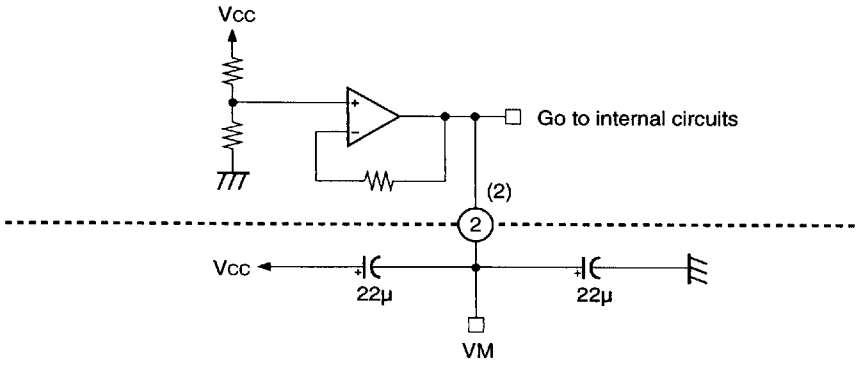
The following explanations are for the CXA1380M as representation. The only difference with the CXA1380N concerns the pin numbers; the operation of the internal circuits for each is identical.

1. Band-pass filter



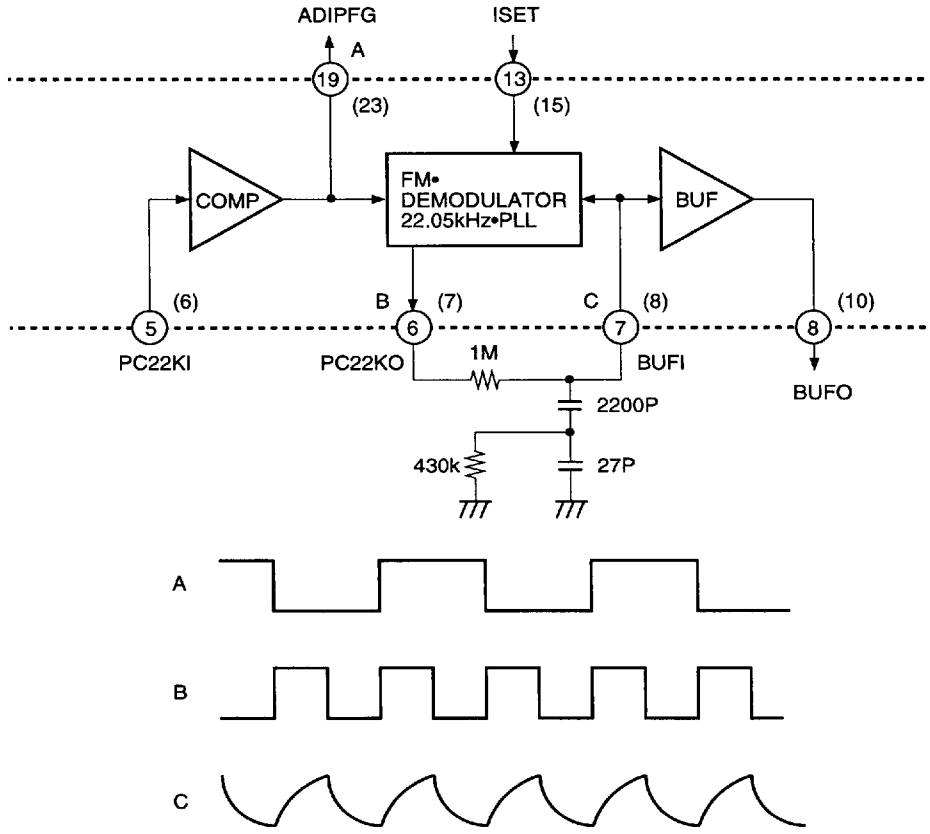
Band-pass filter (BPF) is eliminating the noises from ADIP signal. Signal comes from CXA1381-RF matrix amplifier with a 22.05±1kHz FM signal.

2. Center voltage generation circuit



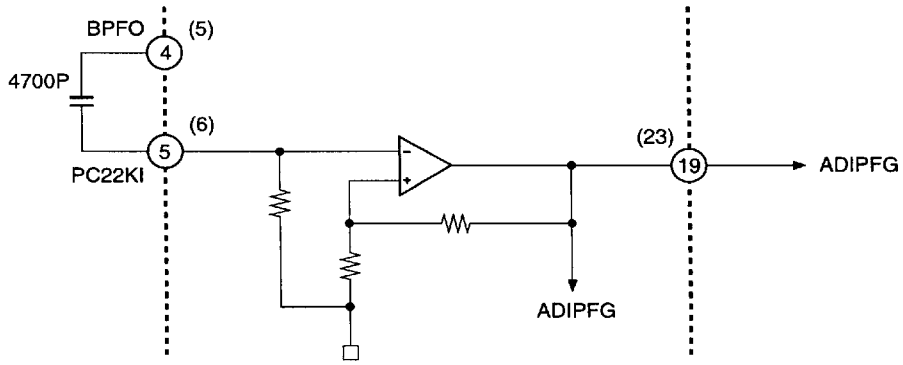
This circuit is generating a half voltage of supply voltage, and take of operating reference to internal circuits. Motors or actuators can not be connected because the maximum output currents are +2mA and −1mA. Note that an electrolytic capacitor should be connected as shown in the diagram to reduce the noises and maintainning a normally operation.

3. FM demodulator



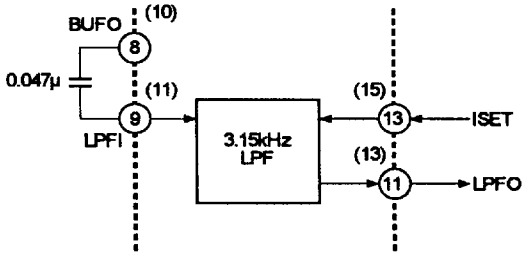
The circuit is extracting the bi-phase data from 22.05±1kHz FM modulated signal (ADIPFM) in applied to PLL, that is an explanation next. PC22KI is input of ADIPFM signal. It's an analog signal, can't matching the digital circuits, because passing through the BPF. ADIPFM signal is transformed to binary value by the COMP, and bring to ADIPFG output. PC22KO is output of the compared signal of ADIPFG signal and internal VCO signal. BUFI is input of the PC22KO signal through the loop filter (LPF), and then complete the PLL circuit is controlling the oscillation frequency of internal VCO. In addtion, the buffer is reducing the impedance of loop filter and outputing to BUFO.

4. CLV rough servo FG



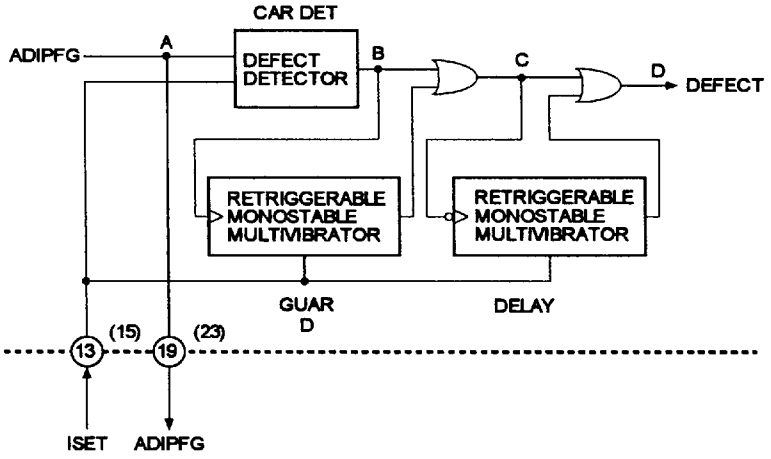
The spindle motor is controlled by servo control of two states. This one is a rough servo which pull the revolutions in the captor range of motor's PLL circuit with ADIPFG signal. Another one is a standard (Phase lock loop) servo which adjust the revolutions in data clocks with FMCK signal.
This circuit is producing the digital signal in use the CLV rough servo. The digital siganal is a FG signal and made by 22.05±1kHz ADIPFM. The FG signal is made by comparator with hysteresis, and outputing to ADIPFG.

5. Low-pass filter



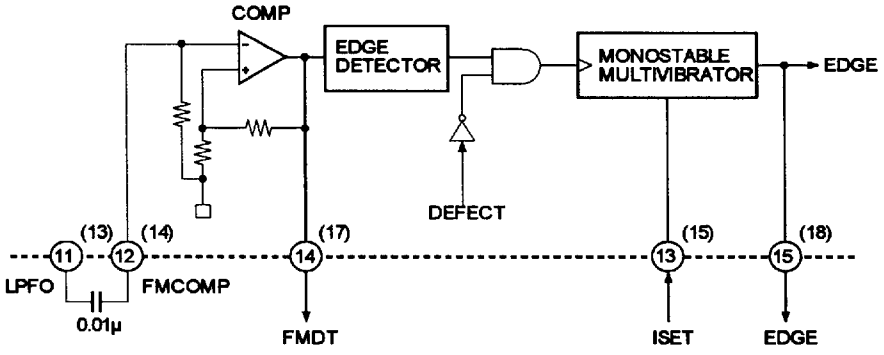
This circuit eliminates the carrier component (22.05kHz) from the BPFO output signal (It has components of carrier and bi-phase data), and produce the bi-phase data.
The filter is set to cut off frequency of 5kHz.
The input signal of LPFI needs the capacitor.

6. Defect detection



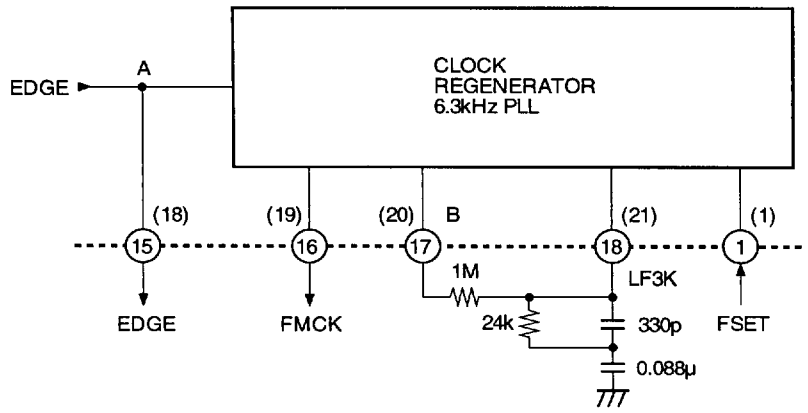
This circuit detects defects in ADIP.

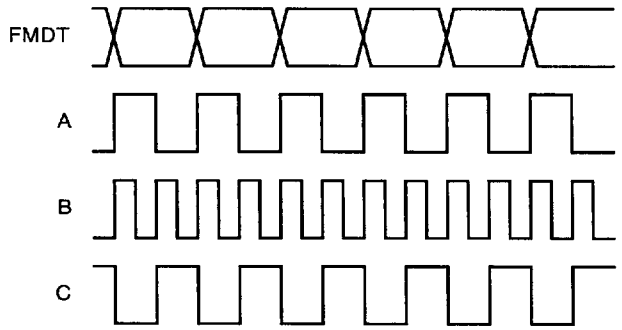
7. Edge detection



If you want to extract the bit clock included the bi-phase data. You must get the edge timing from the bi-phase data with EDGE DETECTOR. After that, MONOSTABLE MULTIVIBRATOR is triggerd by edge signal and marking a 78µs pulse.
However, when DEFECT is high, the pulse is stopped.
FMDT output signal is a bi-phase data processed binary value.

8. Clock regenerator





This circuit regenerates the bit clock from edges included bi-phase data. 6.3kHz PLL is locked to the edges timing, and create the double frequency, and the signal is outputed to the FMCK.

Notes on Operation

CXA1380M

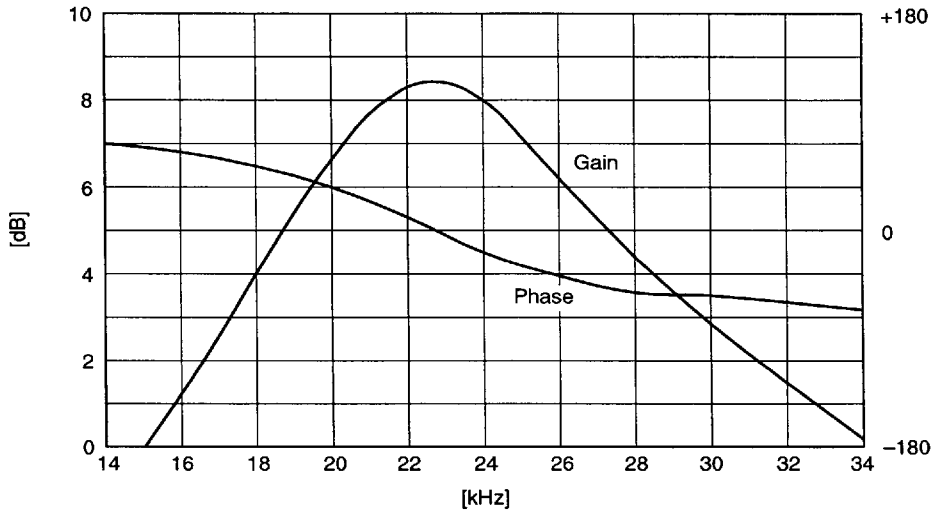
- When using FMDT (Pin 14), EDGE (Pin 15), FMCK (Pin 16), and ADIPFG (Pin 19), they should be received using Schmitt triggers. However buffers are not needed because the CXD2525 has built-in Schmitt triggers.
- Do not use shielded wire or coaxial cable to carry the signals because each output pin has little drive capability. Connect the output pins to other ICs on the PCB by the shortest route possible.

CXA1380M

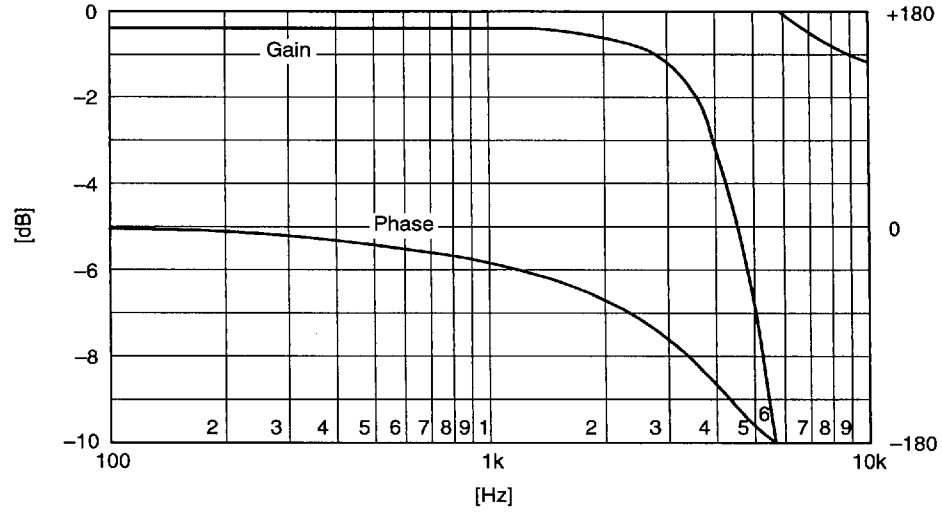
- When using FMDT (Pin 17), EDGE (Pin 18), FMCK (Pin 19), and ADIPFG (Pin 23), they should be received using Schmitt triggers. However buffers are not needed because the CXD2525 has built-in Schmitt triggers.
- Do not use shielded wire or coaxial cable to carry the signals because each output pin has little drive capability. Connect the output pins to other ICs on the PCB by the shortest route possible.
- Pins 3, 9, 16, and 22 are not connected internally. The anti-noise performance of the IC are improved when these pins are connected to GND.

Example of Representative Characteristics

BPF characteristics



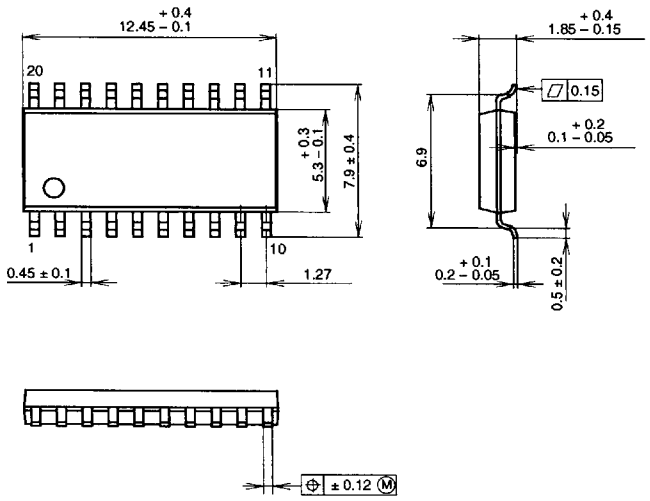
LPF characteristics



Package Outline Unit: mm

CXA1380M

20PIN SOP (PLASTIC) 300mil



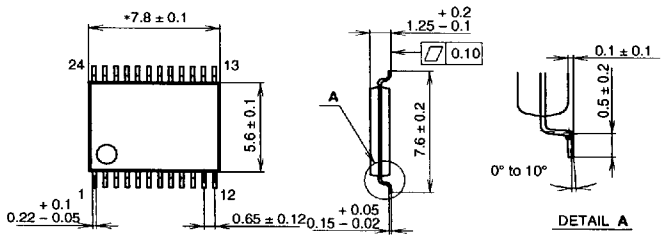
PACKAGE STRUCTURE

SONY CODE	SOP-20P-L01
EIAJ CODE	*SOP020-P-0300-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.3g

CXA1380N

24PIN SSOP (PLASTIC) 275mil



NOTE : *NOT INCLUDE MOLD FINS.

PACKAGE STRUCTURE

SONY CODE	SSOP-24P-L01
EIAJ CODE	A SIMILAR TO SSOP024-P-0300
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	————