A Cirrus Logic Company

CS5032

12-Bit, 400kSPS, Sampling A/D Converter

Features

- Monolithic CMOS A/D Converter
  - 0.5 µs Track/Hold Amplifier
  - 2.0 µs A/D Conversion
  - 2.5 V Voltage Reference
  - Parallel, Serial and Byte Interface.
- 12-Bit ADC Linearity Error: 0.5 LSB
- Low Distortion
  - Signal-to-Noise Ratio: 72.8 dB
  - Total Harmonic Distortion: 0.01 %
  - Spurious-Free-Dynamic-Range: -80dBc
- Low Power: 120 mW
- 60 ppm/°C Reference Drift

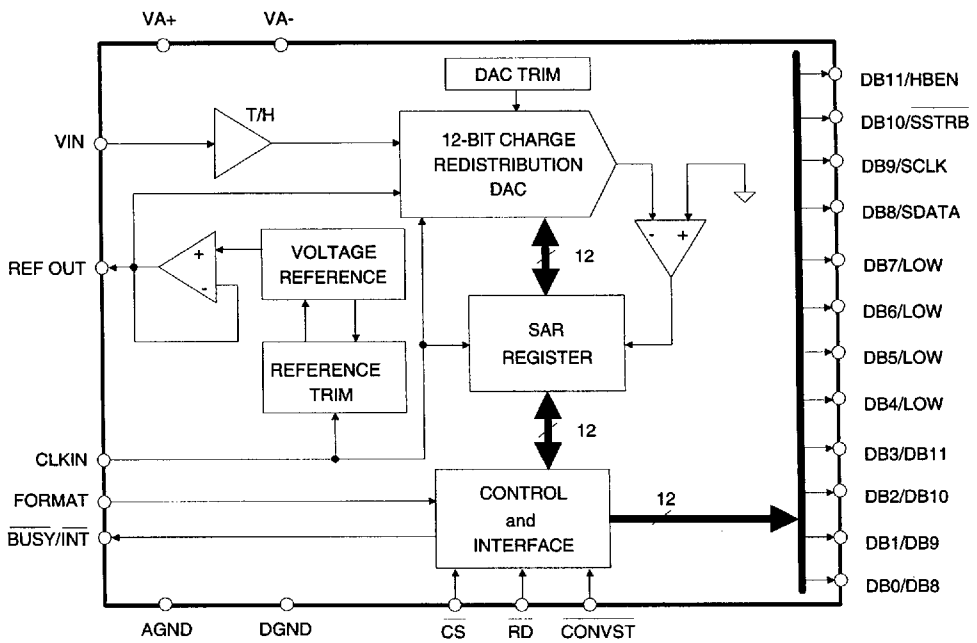
General Description

The CS5032 is a complete monolithic CMOS analog-to-digital converter providing 400kSPS throughput. The part has an internal sample-and-hold, voltage reference, and can operate with an internal or external clock.

The CS5032 has a high-speed digital interface with three-state data outputs and standard control inputs allowing easy interfacing to common microprocessors and digital signal processors. Digital output data is available in either 12-bit parallel, two 8-bit bytes, or serial formats.

The CS5032 is available in a 24-pin, 0.3" plastic dual-in-line package (PDIP), and small outline (SOIC) package.

ORDERING INFORMATION: See Page 21



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ANALOG CHARACTERISTICS (VA+ = +5V±5%; VA- = -5V±5%; AGND = DGND = 0V; CLKIN = 8MHz, unless otherwise specified. $T_A = T_{MIN}$ to T_{MAX})

Parameter	(Note 1)	Symbol	Min	B Typ	Max	Units
Specified Temperature Range				-40 to +85		°C
Accuracy						
Integral Non-Linearity		INL	-	0.5	1.0	LSB
Differential Non-Linearity		DNL	-	0.8	1.0	LSB
No Missing Codes		NMC		Guaranteed		
Bipolar Zero Error		V_{BP}	-	1	5	LSB
Positive Full Scale Error	(Note 2)	FSE_P	-	2	5	LSB
Bipolar Negative Full Scale Error	(Note 2)	FSE_N	-	2	5	LSB
Dynamic Performance	(Note 3)					
Signal-to-Noise-and-Distortion	(Note 4)	SINAD	70	72	-	dB
Signal-to-Noise Ratio		SNR	70	72.8	-	dB
Total Harmonic Distortion		THD	-80	-85	-	dB
			-	-	0.01	%
Spurious-Free-Dynamic-Range	(Note 5)	SFDR	-	-	0.01	%
			-80	-87	-	dBc
Intermodulation Distortion	(Note 6)	IMD				
Second Order			-80	-88	-	dBc
Third Order			-80	-88	-	dBc
Analog Input						
Input Voltage Range		AIN	-2.5	-	+2.5	V
Aperture Delay		t_{apd}	-	-	25	ns
Aperture Jitter		t_{apj}	-	-	100	ps
Input Capacitance		A_{cin}	-	-	10	pF

Notes:
1. All parameters are guaranteed by design, test, and/or characterization.
2. Measured with respect to internal reference and includes bipolar offset error.
3. $A_{IN} = \pm 2.5V_{pp}$
4. A_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 400kSPS. Typically 71.5dB for 10kHz<A_{IN}<250kHz.
5. A_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 400kSPS. Typically -80dB for 0<A_{IN}<250kHz.
6. fa = 9kHz, fb = 9.8kHz, f_{SAMPLE} = 400kSPS.

* Parameter definitions are given at the end of this data sheet prior to the package outline information.

ANALOG CHARACTERISTICS (Continued)

Parameter		Symbol	B Min	Typ	Max	Units
Specified Temperature Range			-40 to +85			°C
Reference Output						
Output Voltage		V_R	2.49	-	2.51	V
REF OUT Tempco			-	60	-	ppm/°C
Load Regulation	(Note 7)	$\Delta VR/\Delta I$	-	0.6	1	mV/mA
Output Noise Voltage		e_N	-	100	-	μV_{rms}
Output Current Drive						
Source Current		I_{SOURCE}	-	500	-	µA
Sink Current		I_{SINK}	-	100	-	µA
Conversion & Throughput						
Conversion Time		tconv		16	17	MMC*
External Clock (CLKIN = 8MHz)			-	-	2.2	µs
Internal Clock			1.8	-	2.4	µs
Acquisition Time		t_{acq}	-	-	0.5	µs
Throughput		ftp	400	-	-	kSPS
Power Supplies						
Positive Supply Current @ +5.0V		I_{A+}	-	13	18	mA
Negative Supply Current @ -5.0V		I_{A-}	-	9	12	mA
Power Dissipation		P_D	-	110	150	mW

Note: 7. Reference Load Current Change (0-500 µA). Reference Load should not be changed during conversion

LSB	%FS	ppm FS	mV
0.25	.0061	61	0.31
0.50	.0122	122	0.61
1.00	.0244	244	1.22
2.00	.0488	488	2.44
4.00	.0976	976	4.88

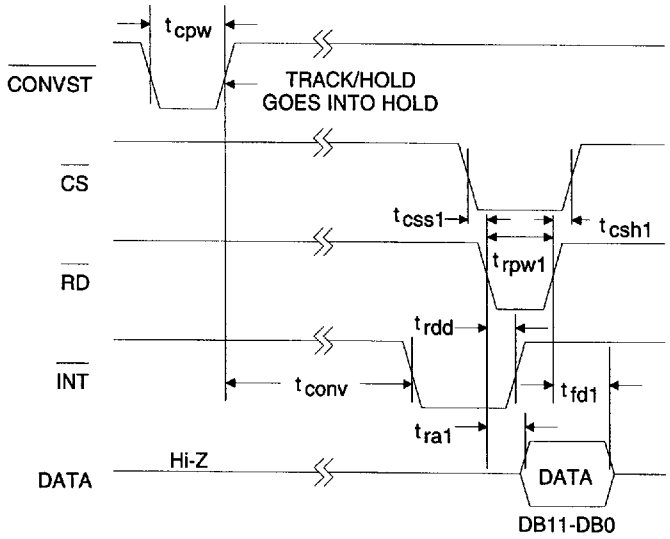
Unit Conversion Factors: $V_{IN} = \pm 2.5V$

SWITCHING CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+ = +5V±5%, VA- = -5V±5%; AGND = DGND = 0V, (Note 8)

Parameter		Symbol	Min	B Typ	Max	Units
Specified Temperature Range				-40 to +85		°C
CLKIN	Period	t_{clk}	125	-	400	ns
CLKIN	Low Time	t_{clkl}	0.4	-	0.6	MCC*
CLKIN	High Time	t_{clkh}	0.4	-	0.6	MCC*
Rise Times	Any Digital Input	t_{rise}	-	-	20	ns
	Any Digital Output	t_{rise}	-	20	-	
Fall Times	Any Digital Input	t_{fall}	-	-	20	ns
	Any Digital Output	t_{fall}	-	20	-	ns
Mode 1 Timing						
Conversion Time		tconv	-	-	17	ns
CONVST Pulse Width		t_{cpw}	95	-	-	ns
$\overline{CS}$ Active to $\overline{RD}$ Active		t_{css1}	0	-	-	ns
$\overline{RD}$ Pulse Width		t_{rpw1}	60	-	-	ns
$\overline{RD}$ Inactive to $\overline{CS}$ Inactive		t_{csh1}	0	-	-	ns
$\overline{RD}$ Active to $\overline{INT}$ Inactive		t_{rdd}	-	-	70	ns
Data Access Time after $\overline{RD}$	(Note 9)	t_{ra1}	-	-	57	ns
Output Float Delay: $\overline{RD}$ Rising to Hi-Z	(Note 10)	t_{fd1}	5	-	95	ns
HBEN to $\overline{RD}$ Falling		t_{hrs}	95	-	-	ns
$\overline{RD}$ Inactive to HBEN Hold Time		t_{hrh}	0	-	-	ns
Serial Clock Timing						
$\overline{SSTRB}$ to SLCK Falling Time	(Note 11)	t_{sss}	10	-		ns
Serial Clock Pulse Width High		t_{pwh}	0.4	-	0.6	MCC*
Pulse Width Low		t_{pwl}	0.4	-	0.6	MCC*
SCLK rising to Data Valid	(Note 12)	t_{ss}	-	-	35	ns
SCLK rising to $\overline{SSTRB}$ Inactive		t_{ssr}	5	-	35	ns
SCLK rising to SDATA Hold Time		t_{sh}	5	-	35	ns

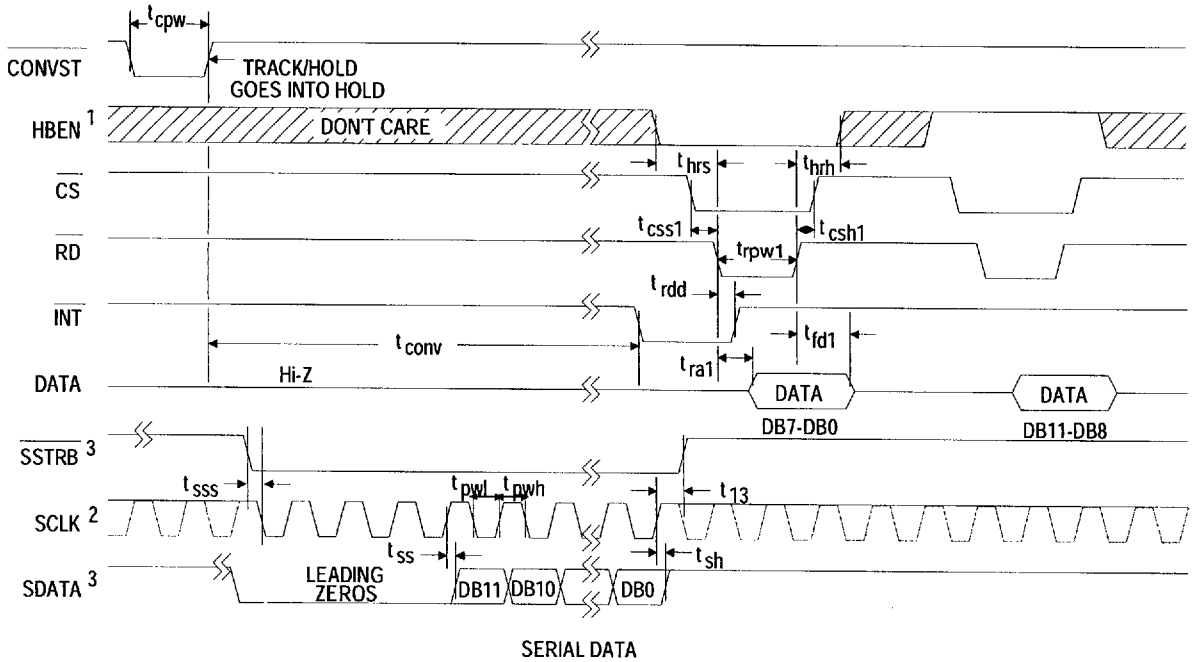
MCC = Master Clock Cycles, 1 MCC = t_{clk}

Notes:
8. All input signals are specified with t_{rise} = t_{fall} = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
9. Measured with the load circuits of Figure 5 and defined as the time required for an output to cross 0.8V or 2.4V.
10. Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 6.
11. t_{sss} = MCC/2 - 25ns. t_{sss} = 25ns for t_{clk} = 125ns.
12. CL = 35pF. SDATA will drive higher capacitive loads but this will add to tss.



NOTE: FORMAT = +5V

Figure 1. Mode 1 Timing Diagram, 12-Bit Parallel Read



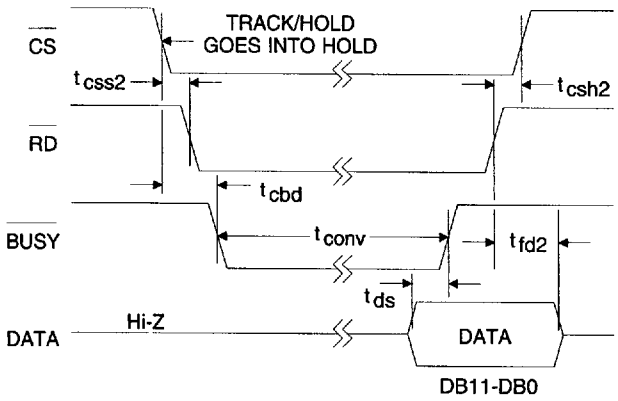
NOTES:
1. Times t_{css1}, t_{rpw1}, t_{csh1}, and t_{hrh} are the same for a high byte read as for a low byte read.
2. Continuous SCLK (Dashed line) when FORMAT = -5V
   Noncontinuous whenFORMAT = 0V

Figure 2. Mode 1 Timing Diagram, Byte or Serial Read

SWITCHING CHARACTERISTICS (Continued)

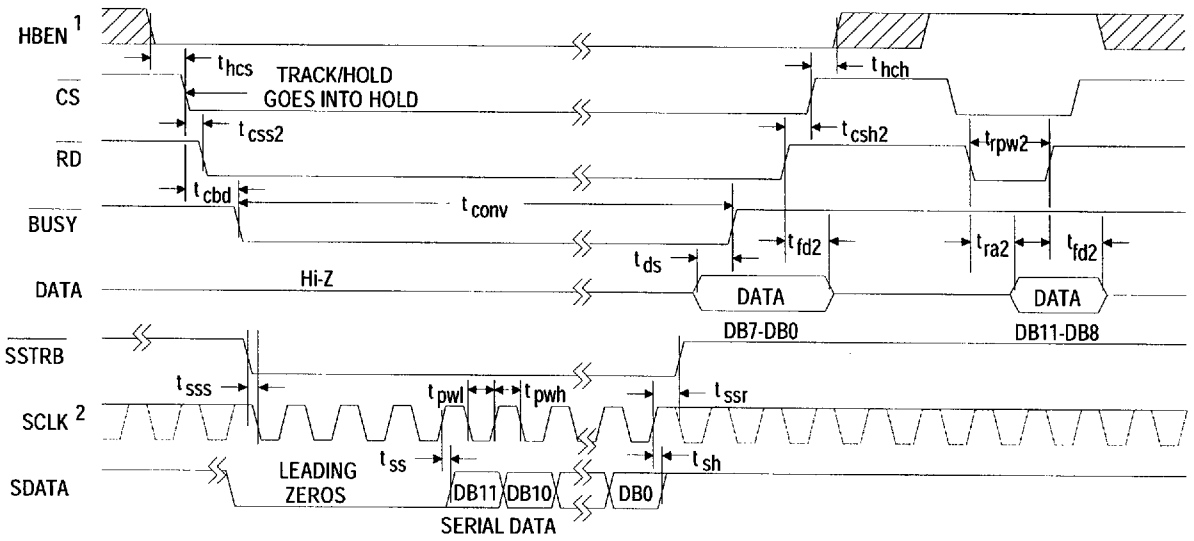
Parameter		Symbol	Min	B Typ	Max	Units
Specified Temperature Range				-40 to +85		°C
Mode 2 Timing						
Conversion Time		t_{conv}	-	-	17	MMC*
$\overline{CS}$ Active to $\overline{RD}$ Active		t_{css2}	30	-	-	ns
$\overline{CS}$ Active to $\overline{BUSY}$ Active		t_{cbd}	-	-	95	ns
Data Setup Time to $\overline{BUSY}$ Inactive		t_{ds}	100	-	-	ns
$\overline{RD}$ Inactive to $\overline{CS}$ Inactive		t_{csh2}	0	-	-	ns
Output Float Delay: $\overline{RD}$ Rising to Hi-Z		t_{fd2}	5	-	95	ns
HBEN Low to $\overline{CS}$ Active Setup Time		t_{hcs}	0	-	-	ns
$\overline{CS}$ Inactive to HBEN Hold Time		t_{hch}	0	-	-	ns
$\overline{RD}$ Pulse Width		t_{rpw2}	60	-	-	ns
Data Access Time After $\overline{RD}$	(Note 10)	t_{ra2}	-	-	57	ns
Serial Clock Timing						
Serial Clock	Pulse Width High	t_{pwh}	0.4	-	0.6	MCC*
	Pulse Width Low	t_{pwl}	0.4	-	0.6	MCC*
$\overline{SSTRB}$ to SCLK Falling Time	(Note 12)	t_{sss}	10	-	-	ns
SCLK rising to Data Valid	(Note 13)	t_{ss}	-	-	35	ns
SCLK rising to $\overline{SSTRB}$ Inactive		t_{ssr}	5	-	35	ns
SCLK rising to SDATA Hold Time		t_{sh}	5	-	35	ns

*MCC = Master Clock Cycles, 1 MCC = t_{clk}



NOTE: FORMAT = +5V.

Figure 3. Mode 2 Timing Diagram, 12-Bit Parallel Read



NOTES: 1. Times t_{hcs}, t_{css2}, t_{csh2}, and t_{hch} are the same for a high byte read as for a low byte read.
2. Continuous SCLK (Dashed line) when FORMAT = -5V
Noncontinuous when FORMAT = 0V

Figure 4. Mode 2 Timing Diagram, Byte or Serial Read

DIGITAL CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}: VA+ = +5V±5%; VA- = -5V±5%)

Parameter		Symbol	Min	Typ	Max	Units
Logic Inputs						
High-level Input Voltage		V_{IH}	3.3			V
Low-level Input Voltage		V_{IL}			0.8	V
Input leakage current		I_{in}			10	µA
Input Capacitance		C_{in}			10	pF
Logic Outputs						
High-level Output Voltage	(Note 13)	V_{OH}	4.0			V
Low-level Output Voltage	(Note 14)	V_{OL}			0.4	V
DB11-DB0 Floating State leakage Current		I_{OZ}			25	µA
DB11-DB0 Output Capacitance		C_{out}			15	pF

Notes: 13. I_{source} = -40µA
14. I_{sink} = 1.6 mA

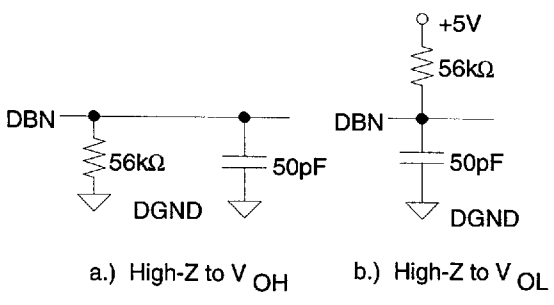


Figure 5. Load Circuits for Access Time

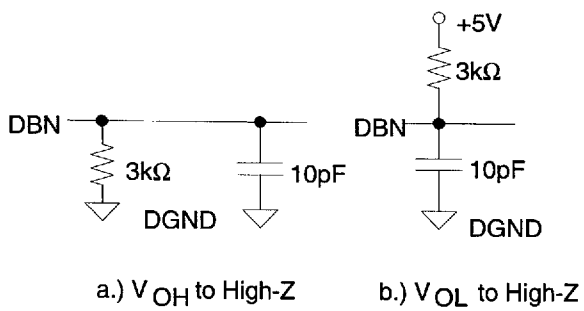


Figure 6. Load Circuits for Output Float Delay

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V. All voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Supply	VA+	4.75	5.0	5.25	V
Negative Analog Supply	VA-	4.75	5.0	5.25	V
Analog Input Voltage	A_{in}	-2.5		+2.5	V
FORMAT Input Voltage Range			VA-, 0V, VA+		V
CLKIN Input Voltage Range		0		VA+	V
Other Digital Input Voltage Ranges		0		VA+	V
External Clock Frequency			10		MHz
External Clock Jitter				65	ps
AGND to DGND Voltage Differential				10	mV

ABSOLUTE MAXIMUM RATINGS (AGND = 0V, All voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
Positive Analog Supply		VA+	-0.3		6.0	V
Negative Analog Supply		VA-	0.3		6.0	V
Analog Input Voltage		A_{in}	(VA-)-0.3		(VA+)+0.3	V
FORMAT Input Voltage Range			(VA-)-0.3		(VA+)+0.3	V
CLKIN Input Voltage Range			(VA-)-0.3		(VA+)+0.3	V
Other Digital Input Voltage Ranges			(VA-)-0.3		(VA+)+0.3	V
REF OUT Current					10	mA
Sustained Digital Output Current					5	mA
AGND to DGND Voltage Differential					100	mV
Operating Temperature Range	CS5032-BP/BS		-40		+85	°C
Storage Temperature Range			-65		+150	°C
Lead Solder Temperature					+300	°C

* WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes

GENERAL DESCRIPTION

The CS5032 is a complete 12-bit 400 kSPS sampling ADC utilizing a successive approximation architecture. Factory calibration ensures 12-bit conversion accuracy over industrial and military temperature ranges. The analog input range is ±2.5 V, with the output data provided in parallel, byte or serial formats. The internal capacitor array DAC acts as an inherent sample-and-hold, and forms the heart of the CS5032. The on-chip +2.5 V reference is available at the REFOUT pin. Additionally, an on-chip 8 MHz clock oscillator can be used to control converter operations.

OPERATIONAL OVERVIEW

Track-and-Hold Operation

Track-and-hold operation within the CS5032 is transparent to the user. The capacitor array DAC acts as the hold capacitor. During tracking mode all elements of the capacitor array DAC are switched to the analog input for charging. The load capacitance of the entire array during tracking mode is typically 5 pF. The input bandwidth of the track-and-hold is typically 2 MHz. The ADC goes into hold mode on the rising edge of $\overline{\text{CONVST}}$.

Capacitor Array DAC Calibration

To achieve 12-bit accuracy from the capacitor array DAC, the CS5032 uses a novel calibration scheme. Each bit capacitor consists of several capacitors that are trimmed to optimize the overall bit weighting with an internal resolution of 14-bits, resulting in nearly ideal differential and integral linearity.

The calibration coefficients for the capacitive bit weights are stored in an on-chip EEPROM during the factory calibration. When the converter is subsequently powered-up these coefficients are applied to the capacitor array DAC. The low temperature coefficient of the capacitor array easily maintains 12-bit accuracy over the full temperature range without recalibration.

Reference Operation

The reference voltage is available at the REF OUT pin and is capable of sourcing 500 µA to peripheral devices. This pin must be decoupled with a parallel combination of a +10 µF tantalum capacitor and a 0.1 µF ceramic capacitor. The reference voltage is calibrated on power-up, with full accuracy achieved after 1.1 sec.

Analog Input

The CS5032 provides a ±2.5 V analog input voltage range. The equivalent analog input circuit is illustrated in Figure 7 (shown in track mode). During hold mode the input impedance to the device is typically 10 MΩ, and the various elements of the capacitor array DAC are connected to either AGND or VREF. In switching back from hold mode to track mode, some elements in the capacitor array must be charged by the analog input. For the CS5032, the worst case charging current occurs when the analog input changes from +2.5 V to -2.5 V.

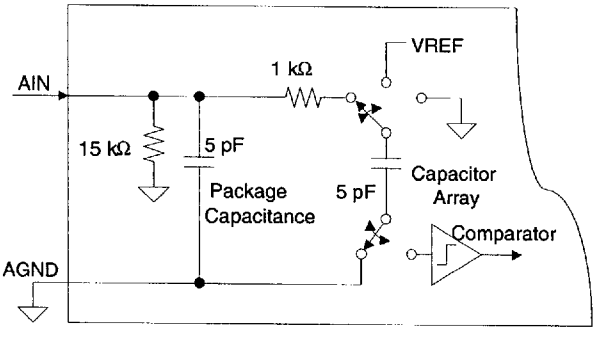


Figure 7. Analog Input Model.

To ensure that the capacitor array DAC has settled to within 0.25 LSB during the allowed acquisition time, the external source resistance should be less than 4 kΩ.

Output Coding

The digital output coding is 2's complement.

Input Level	2's Complement Output
+2.5 V	0111 1111 1111
0 V	0000 0000 0000
-2.5 V	1000 0000 0000

High-Speed System Clock

The CS5032 employs a high-speed clock (typically 10 MHz) to control internal operations. This high-speed clock can be generated internally with the on-chip oscillator, or it can be supplied from an external CMOS source. Connecting a CMOS clock signal to the CLKIN pin allows the converter to operate from an external clock. Alternatively, connecting the CLKIN pin to VA- activates the internal clock oscillator.

External Clock.....CLKIN = External Clock Source
Internal Clock.....CLKIN = VA-

CONVERT Clock Considerations

When digitizing time varying signals, it is possible to create additional noise sources over and above those resulting from quantization noise and thermal noise. This is particularly true when high-speed conversion rates, or high-frequency analog input frequencies are involved. Special care must be taken to see that $\overline{\text{CONVST}}$ clock jitter does not undermine high-speed signal processing applications by introducing noise into the conversion process.

Simple quantization noise is a direct result of the finite LSB size, which is itself related to the number of digital output bits. Quantization noise places a hard limit on SNR for a 12-Bit ADC according to the following equation.

$$SNR_{MAXQuantization} = (6.02dB)(\#\text{ of Bits}) + 1.76dB$$

$$\therefore\ SNR_{MAXQuantization} = 74\ dB$$

Although SNR can never be better than the theoretical limit, it can certainly be worse. Jitter between the $\overline{\text{CONVST}}$ clock and the analog input signal is often one of the largest contributors to decreased SNR, particularly as frequencies increase.

To be considered insignificant, noise related to jitter ($SNR_{MAXjitter}$) should be at least 12 dB below the other dominant noise sources, such as quantization noise ($SNR_{MAXQuantization}$). The 12 dB target is somewhat arbitrary, but yield less than 4 % additional noise. In terms of the CS5032, a 250 kHz analog input signal requires less than 80 ps of jitter between the $\overline{\text{CONVST}}$ clock and the analog input signal to achieve full performance. The use of low-jitter $\overline{\text{CONVST}}$ clock source is the most common means of reducing the effects of jitter. Lower conversion rates and lower analog input frequencies are significantly less sensitive to jitter effects.

Digital Output Formats

The CS5032 provides three digital output formats. These include 12-bit parallel, two 8-bit bytes, and a serial output mode. The output data

$$SNR_{MAX} = \sqrt{SNR_{MAXjitter}^{2} + SNR_{MAXQuantization}^{2}}$$

$$SNR_{MAXjitter}\ (dB) = 20\ \text{Log}\left[\frac{1}{2\pi f_{IN}\ jitter_{RMS}}\right]$$

$$jitter_{RMS} = \sqrt{clock\ jitter_{RMS}^{2} + analog\ jitter_{RMS}^{2}}$$

format is controlled by the level applied to the FORMAT pin. All three of the digital output formats can be used with either of the convert start timing modes ... Mode 1 and Mode 2, which are described in the next two sections.

FORMAT	Digital Outputs
+VA	12-Bit Parallel
GND	Byte; Serial w/Non-Continuous SCLK
-VA	Byte; Serial w/Continuous SCLK

Figure 8 shows the schematic for the CS5032 in 12-bit parallel mode. The twelve bits of data are output simultaneously on DB11/(MSB) through DB0 (LSB).

In byte mode, two 8-bit read operations (four leading zeros with 4 data bits ... plus 8 more data bits) are required to collect the data as shown in Figure 9. In byte mode, the DB11/HBEN pin defers to the HBEN function, selecting the high or low byte of data to be read from the ADC. The lower eight bits of data are placed on the data bus when HBEN is held low. To access the four MSBs of data, HBEN must be held high. The 4 MSBs of the 12-bit data word are right justified with zeros in the upper nibble of the high byte.

In serial mode, DB8/SDATA, DB9/SCLK and DB10/$\overline{\text{SSTRB}}$ defer to their serial functions. The serial strobe pin $\overline{\text{SSTRB}}$ provides a framing signal for serial data. Serial data is available at the

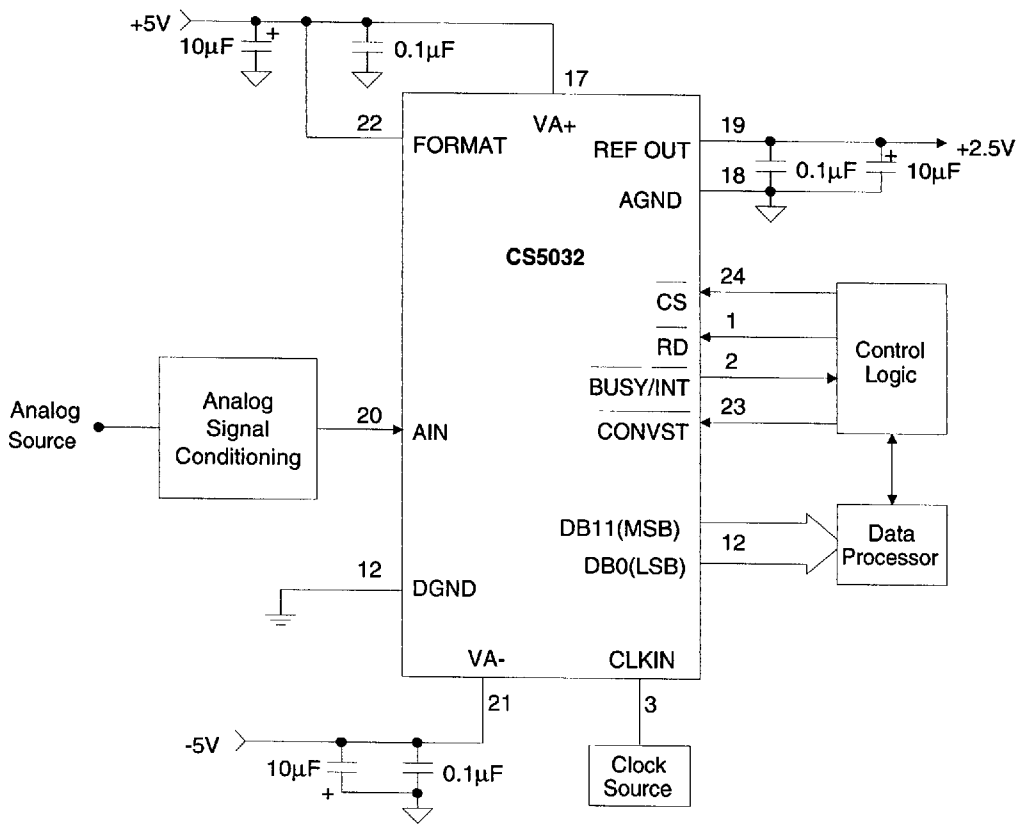


Figure 8. System Connection Diagram: Parallel Data Format

SDATA pin when $\overline{\text{SSTRB}}$ falls low. $\overline{\text{SSTRB}}$ falls low within three clock cycles of $\overline{\text{CONVST}}$. A total of sixteen bits (four leading zeros and twelve data bits starting with the MSB) are clocked out on the SDATA pin on the rising edge of SCLK. The data bits become valid no more than t_{ss} after the rising edge of SCLK. $\overline{\text{SSTRB}}$ goes low during data transmission and automatically returns high when the LSB has been clocked out on the SDATA line. For serial operation, 0V on the FORMAT pin causes the serial clock to run only when data is being clocked out of the device; SCLK goes high after data transmission is completed. If the FORMAT is connected to -VA, the SCLK output will run continuously, independent of data transmission. Serial data operation is identical for MODE 1 and MODE 2 timing control (see next two sections).

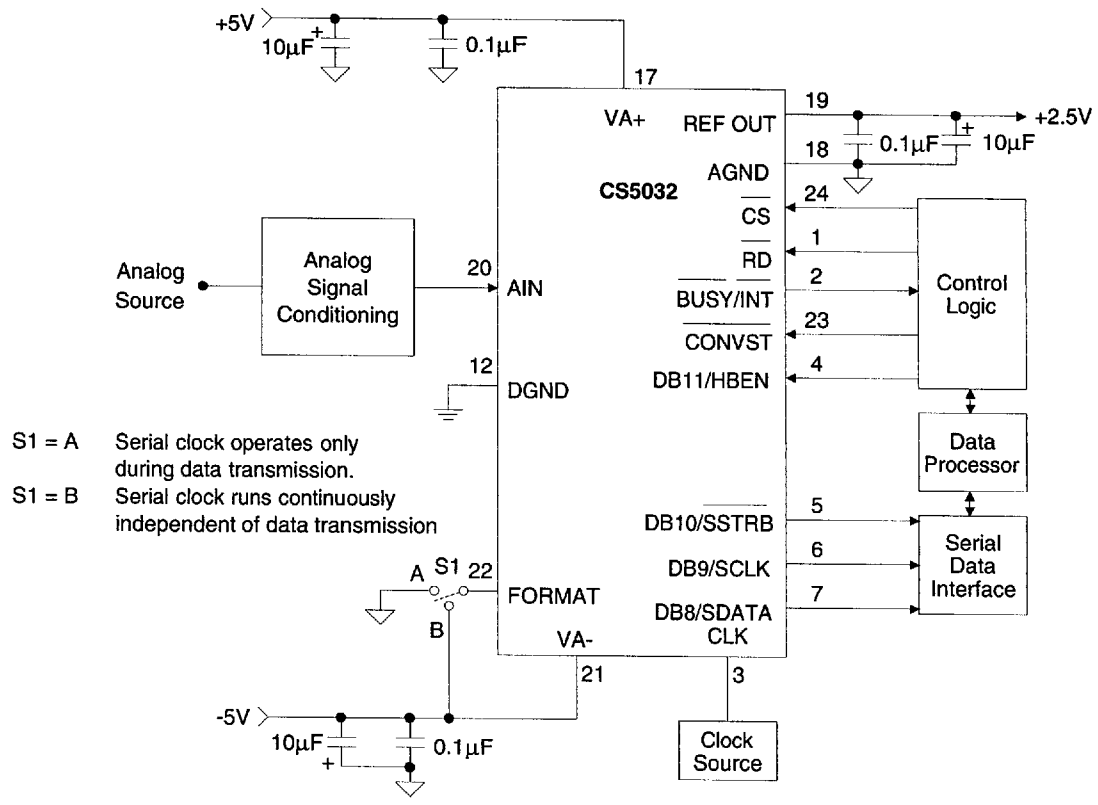


Figure 9. System Connection Diagram: Serial and Byte Data format

MODE 1 Operation

The rising edge of $\overline{\text{CONVST}}$ signal is used to put the device into hold mode and initiate a conversion. At the end of conversion the device returns to it's tracking mode. MODE 1 timing is primarily used in DSP type applications where precise control of $\overline{\text{CONVST}}$ timing is required.

Conversion begins on the rising edge of $\overline{\text{CONVST}}$ provided that $\overline{\text{CS}}$ is high. The $\overline{\text{BUSY}}/\overline{\text{INT}}$ line performs the $\overline{\text{INT}}$ function and can be used to interrupt the microprocessor. $\overline{\text{INT}}$ is normally high and goes low at the end of conversion. The ADC returns to track mode when $\overline{\text{INT}}$ goes low. Bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low allows data to be read from the ADC, and also resets $\overline{\text{INT}}$ high. $\overline{\text{CONVST}}$ must be high when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are brought low for the ADC to operate correctly in this mode. Data cannot be read during a conversion cycle because the output data latches are disabled while a conversion is in progress.

MODE 1 - 12-Bit Parallel Read

Figure 10 shows the MODE 1 timing diagram for 12-bit parallel operation (FORMAT = +VA). A data read operation performed at the end of conversion will read all twelve bits of data at the same time.

MODE 1 - Byte Read

Figure 11 shows the MODE 1 timing diagram for byte operation. At the end of conversion when INT goes low, either the low byte or the high byte of data can be read, depending on the status of HBEN. Bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low allows data to be read from the ADC and also resets $\overline{\text{INT}}$ high.

MODE 1 - Serial Read

The MODE 1 timing diagram for serial operation is shown in Figure 12. Conversion begins on the rising edge of $\overline{\text{CONVST}}$, and data is clocked out on SDATA immediately upon the falling edge of $\overline{\text{SSTRB}}$. The data is output as four leading zeroes followed by the twelve data bits with the MSB first. The first zero should be latched into the external receiving circuitry on the first falling edge of SCLK after $\overline{\text{SSTRB}}$ goes low. A total of sixteen falling SCLK edges will latch all sixteen bits of output data. $\overline{\text{SSTRB}}$ automatically returns high after the last bit of data has been clocked out of the device.

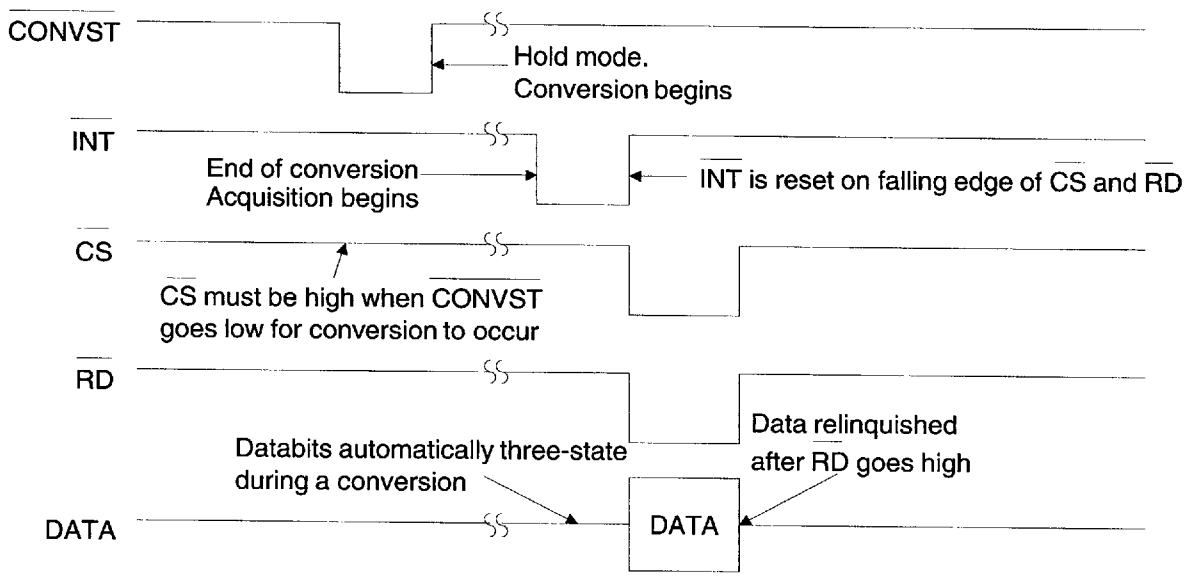
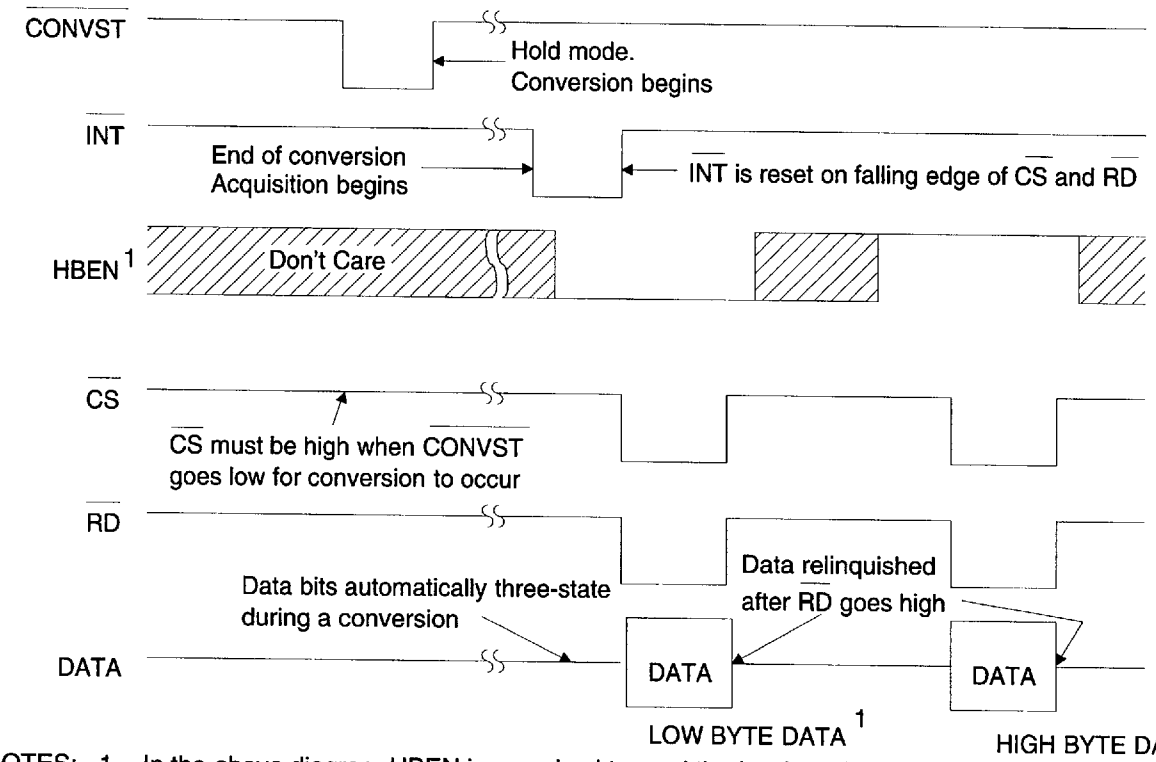


Figure 10. Mode 1 Timing Diagram, 12-bit Parallel Read



NOTES: 1. In the above diagram HBEN is exercised to read the low byte first (DB7-DB0) and then the high byte (DB11-DB8). To change the order in which the bytes are read, simply invert the HBEN signal shown above.

Figure 11. Mode 1 Timing Diagram, Byte Read

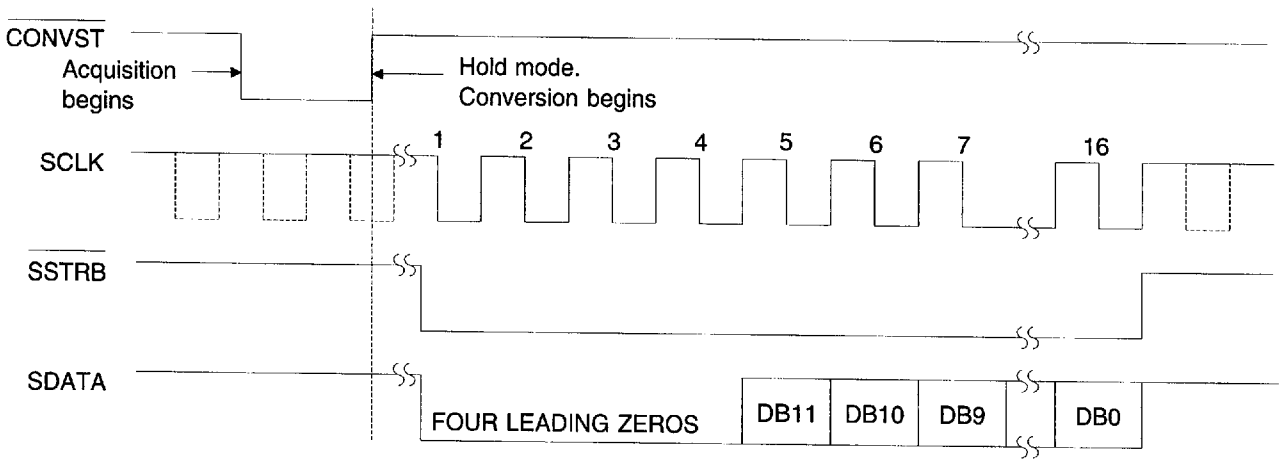


Figure 12. Mode 1 Timing Diagram - Serial Read

MODE 2 Operation

Mode 2 operation allows the ADC conversion to be initiated by a read operation from a µC. The $\overline{BUSY}$ signal can be used in this mode to halt µC operations by placing the µC in a WAIT state until the conversion is complete. This avoids having to handle interrupts and timing delays, assuring that the conversion cycle is complete before any attempted data read.

In this mode, $\overline{CONVST}$ must be held permanently low. Bringing $\overline{CS}$ low (while $\overline{HBEN}$ is low) puts the device into hold mode and initiates a conversion. The $\overline{BUSY}/\overline{INT}$ pin defers to the $\overline{BUSY}$ function such that $\overline{BUSY}$ goes low at the start of conversion and returns high at the end of conversion.

MODE 2 - 12-Bit Parallel Read

The MODE 2 timing diagrams for the parallel data output format are shown in Figure 13. This mode of operation forces the µC into a WAIT state until the conversion has been completed. It removes the risk of inadvertently reading invalid data before the conversion cycle has been completed.

MODE 2 - Byte Read

Figure 14 shows the timing diagram for byte operation in MODE 2. Since $\overline{HBEN}$ must be low to initiate a conversion, the lower byte of data will be accessed first during the two-byte read operation. This is followed by a second byte read operation (with $\overline{HBEN}$ high) to complete the data transfer.

MODE 2 - Serial Read

The timing diagram for MODE 2 serial operation is shown in Figure 15. The device goes into hold mode on the falling edge of $\overline{CS}$ and conversion begins when $\overline{BUSY}$ goes low. The data is clocked out similarly as for MODE 1 serial operation. Upon clocking of the final data bit $\overline{BUSY}$ returns high indicating end of conversion.

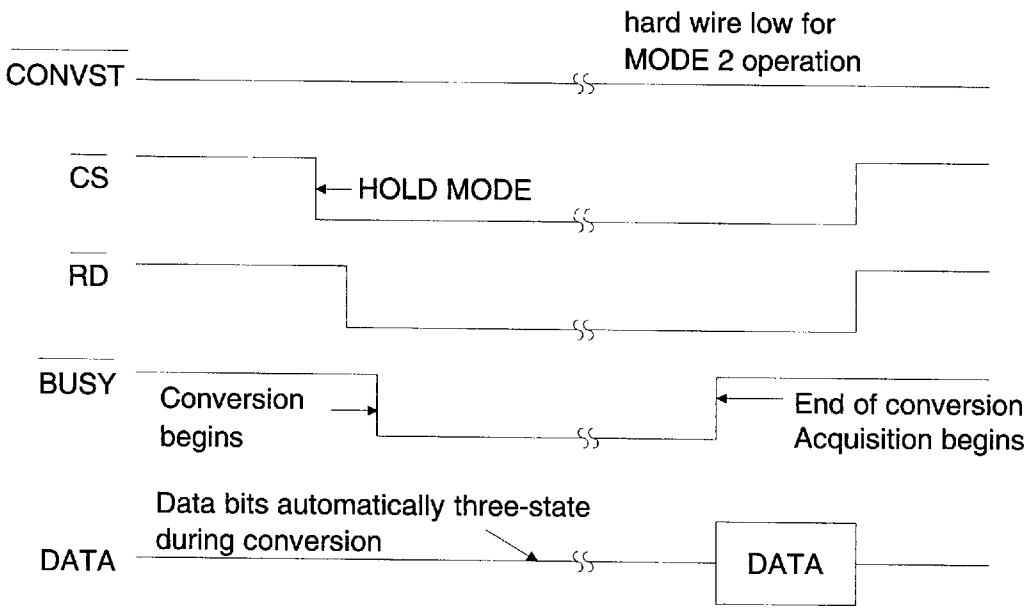


Figure 13. Mode 2 Timing Diagram, 12-bit Parallel Read

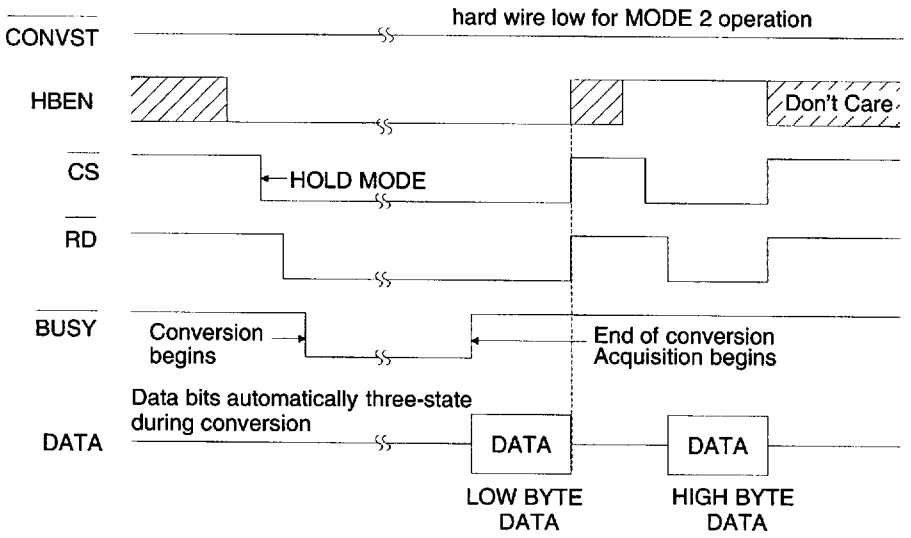


Figure 14. Mode 2 Timing Diagram, Byte Read

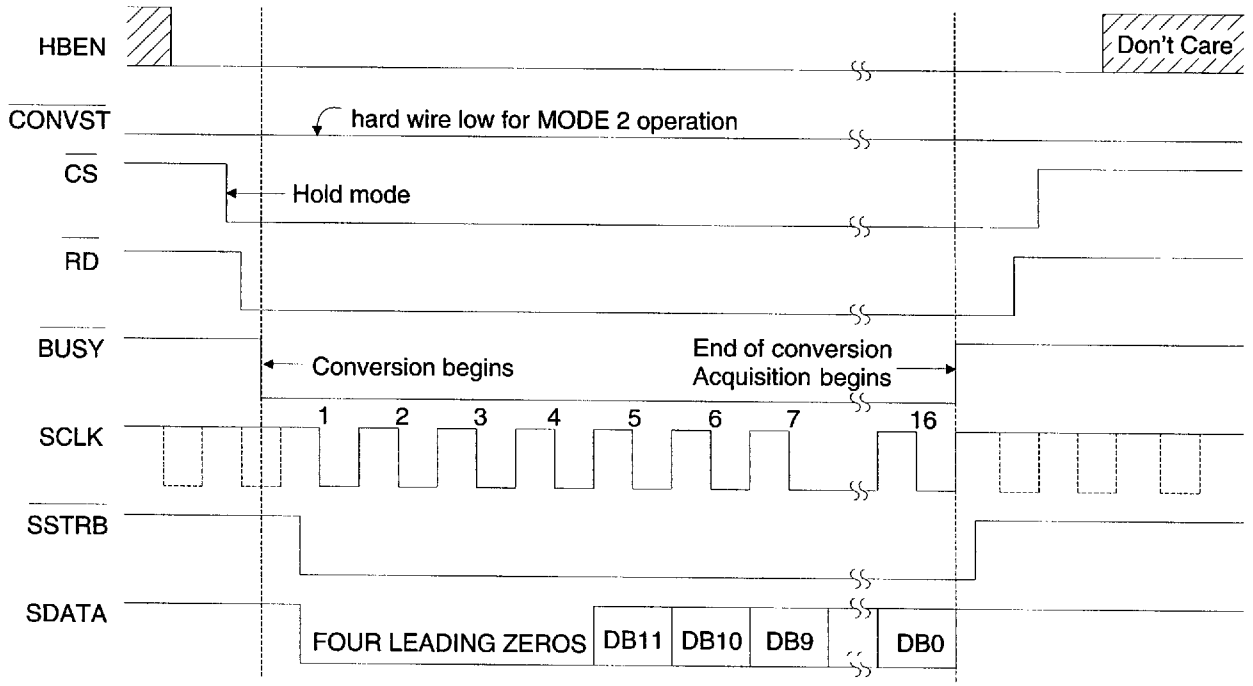


Figure 15. Mode 2 Timing Diagram, Serial Read

STAND-ALONE OPERATION

The CS5032 supports stand-alone conversion when used in MODE 2 parallel interface operation as shown in Figure 16. Conversion is initiated by pulse to the $\overline{CS}$ input of the ADC. The duration of the pulse must be longer than the ADC conversion time. The $\overline{BUSY}$ output drives the $\overline{RD}$ input and data is latched on the rising edge of $\overline{BUSY}$ to an external latch.

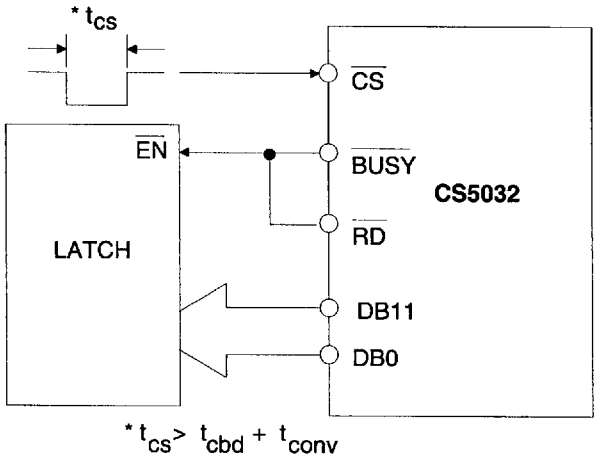


Figure 16. Stand-Alone Operation

Power Supplies, AGND, and DGND

Figure 8 illustrates the recommended power supply decoupling scheme with a 0.1 µF ceramic and a +10 µF tantalum capacitor for both the VA+ and the VA- pins. The capacitors should be located as close as practical to the supply pins. AGND is the power supply current return, and is also the preferred ground reference for the decoupling capacitors.

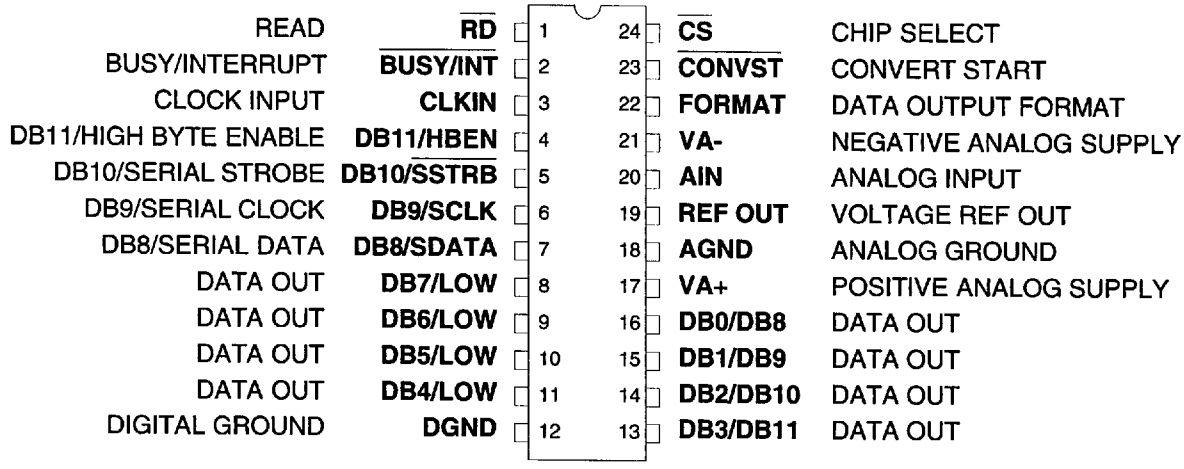
Typically a low-impedance ground plane is used around and under the ADC, with connections to both AGND and DGND. If a split ground is used, DGND is the ground reference for any digital circuits that follow the CS5032. When split grounds are used, the AGND to DGND voltage differential should be kept below ±10 mV for best operation.

Special Note: The CS5032 employs on-chip memory to store power-up reset calibration data. If the power supply voltage is dropped below 3 V, it is possible that this memory may lose the current calibration data. The ADC can be reset by switching power off and then back on, to initiate the power-on reset sequence.

Layout considerations

The CS5032 is a high-speed component which requires adherence to standard high-frequency printed circuit board layout techniques to maintain optimum performance. These include proper supply decoupling, minimum length circuit traces, and physical separation of digital and analog components and circuit traces. See the CDB5032 evaluation board data sheet for more details.

PIN DESCRIPTIONS



Pinout applies to both DIP and SOIC packages.

Power Supply Connections

VA+ – Positive Supply, PIN 17.
+5V±5%.

VA- – Negative Supply, PIN 21.
-5V±5%.

DGND – Digital Ground, PIN 12.
Ground reference for digital circuitry.

AGND – Analog Ground, PIN 18.
Ground reference for track-and-hold, reference and DAC.

Oscillator

CLKIN – Clock Input, PIN 3.
An external 8MHz (CMOS compatible) clock is applied at this pin. Connecting this pin to VA- enables the internal clock oscillator.

Digital Inputs

$\overline{CS}$ – Chip Select, PIN 24.
Active low logic input. The device is selected when this input is active. With $\overline{CONVST}$ tied low, a new conversion is initiated when $\overline{CS}$ goes low.

$\overline{RD}$ – Read, PIN 1.

Active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the data outputs.

FORMAT – Output Mode Selection, PIN 22.

Defines the output data format and serial clock format. With FORMAT at +5V, the output data format is 12-bit parallel only. With FORMAT at 0V, either byte or serial data is available and SCLK is not continuous. With FORMAT at -5V, byte or serial data is again available but SCLK is now continuous.

$\overline{CONVST}$ – Convert Start, PIN 23.

A low to high transition on this input puts the track-and-hold into its hold mode and starts conversion. This input is asynchronous to the CLKIN and independent of $\overline{CS}$ and $\overline{RD}$.

Digital Outputs

$\overline{BUSY}/\overline{INT}$ – Busy/Interrupt, PIN 2.

Active low logic output indicating converter status. See timing diagrams.

DB11/HBEN – Data Bit 11/High Byte Enable, PIN 4.

The function of this pin is dependent on the state of the FORMAT input (see above). When 12-bit parallel data is selected, this pin provides the DB11 output. When byte data is selected, this pin becomes the HBEN logic input. HBEN is used for 8-bit bus interfacing. When HBEN is low, DB7/LOW to DB0/DB8 become DB7 to DB0. With HBEN high, DB7/LOW to DB0/DB8 are used for the upper byte of data (see Table 1).

DB10/$\overline{SSTRB}$ – Data Bit 10/Serial Strobe, PIN 5.

The function of this pin is dependent on the state of the FORMAT input (see above). When 12-bit parallel data is selected, this pin provides the DB10 output. If FORMAT is at either 0V or -5V, $\overline{SSTRB}$ provides a strobe or framing pulse for serial data.

DB9/SCLK – Data Bit 9/Serial Clock, PIN 6.

The function of this pin is dependent on the state of the FORMAT input (see above). When 12-bit parallel data is selected, this pin provides the DB9 output. SCLK is the gated serial clock output derived from the internal or external ADC clock. If FORMAT is at -5V, then SCLK runs continuously. If FORMAT is at 0V, then SCLK goes high after serial transmission is complete.

DB8/SDATA – Data Bit 8/Serial Data, PIN 7.

The function of this pin is dependent on the state of the FORMAT input (see above). When 12-bit parallel data is selected, this pin provides the DB8 output. SDATA is used with SCLK and $\overline{SSTRB}$ for serial data transfer. Serial data is valid on the falling edge of SCLK while $\overline{SSTRB}$ is low.

DB7/LOW, DB6/LOW, DB5/LOW, DB4/LOW – Three-state data outputs, PINS 8, 9, 10, 11.

The outputs of these pins are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the FORMAT and HBEN inputs. With FORMAT high, they are always DB7-DB4. With FORMAT low or -5V, their function is controlled by HBEN (see Table 1).

DB3/DB11, DB2/DB10, DB1/DB9, DB0/DB8 – Three-state data outputs, PINS 13, 14, 15, 16.

The outputs of these pins are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the FORMAT and HBEN inputs. With FORMAT high, they are always DB3-DB0. With FORMAT low or -5V, their function is controlled by HBEN (see Table 1).

HBEN	DB7/LOW	DB6/LOW	DB5/LOW	DB4/LOW	DB3/DB11	DB2/DB10	DB1/DB9	DB0/DB8
HIGH	LOW	LOW	LOW	LOW	DB11/(MSB)	DB10	DB9	DB8
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0/(LSB)

Table 1. Output Data for Byte Interfacing

Analog Output

REF OUT - Voltage Reference Output, PIN 19.

The internal 2.5V reference is provided at this pin. The external load capability is 500µA. This pin should be decoupled to AGND with a +10µF tantalum and a 0.1µF ceramic capacitor. The REF OUT voltage has a settling time of approximately 1.1 sec.

Analog Input

AIN - Analog Input, PIN 20.

The analog input range for the CS5032 is ±2.5V.

Ordering Guide

Model Number	Throughput (kSPS)	Input Range (V)	Linearity Error (LSB)	Temp. Range (°C)	Package
CS5032-BP	400	±2.5	±0.5	-40 to +85	24-Pin 0.3" PDIP
CS5032-BS	400	±2.5	±0.5	-40 to +85	24-Pin 0.3" SOIC

PARAMETER DEFINITIONS

Integral Non-Linearity Error - INL

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code.

REF OUT Tempco

REF OUT Tempco is the worst case slope that is calculated from the change in reference value at +25°C to the value at T_{MIN} or T_{MAX}

i.e. REF OUT Tempco = (V_{ref} @ 25°C - V_{ref} @ T_{MAX})/(T_{MAX} - 25°C) or

REF OUT Tempco = (V_{ref} @ 25°C - V_{ref} @ T_{MIN})/(25°C - T_{MIN}).

Differential Nonlinearity - DNL

The deviation of a code's width from the ideal. Units in LSBs.

Full-Scale Error - FSE_P

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Bipolar Offset - V_{BP}

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below AGND). Units in LSB's.

Bipolar Negative Full-Scale Error - FSE_N

The deviation of the first code transition from the ideal. The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Spurious-Free-Dynamic-Range - SFDR

The ratio of the rms value of the signal, to the rms value of the next largest spectral component (excepting dc). This component is often an aliased harmonic. Units in percent and dBc (decibels relative to the carrier).

Total Harmonic Distortion - THD

The ratio of the rms sum of the significant (2^{nd} thru 5^{th}) harmonics, to the rms value of the signal. Units in percent.

Signal-to-Noise-and-Distortion (s/n) - SNR

The ratio of the rms value of the signal, to the rms sum of all other spectral components (excepting dc and distortion terms). Expressed in decibels.

Signal-to-Noise-and-Distortion (s/[n+d]) - SINAD

The ratio of the rms value of the signal, to the rms sum of all other spectral components (excepting dc), including distortion components. Expressed in decibels.

Intermodulation Distortion - IMD

The ratio of the rms value of the larger of the two test frequencies, which are each 6dB down from full-scale, to the rms value of the largest 2^{nd} order and 3^{rd} order intermodulation component. Units in decibles relative to carrier.

Aperture Delay Time - t_{apd}

The time required, after the converter goes into hold mode, for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Unit in nanoseconds.

Aperture Jitter - t_{apj}

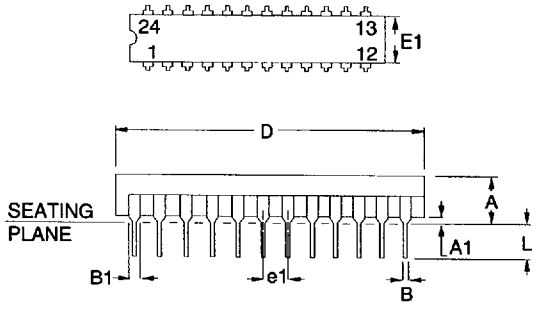
The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy.

$$SNR_{MAXjitter}\,(dB) = 20Log\left[\frac{1}{2\pi f_{IN}\,jitter_{RMS}}\right]$$

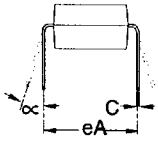
$$jitter_{RMS} = \sqrt{clock\,jitter_{RMS}{}^{2} + analog\,jitter_{RMS}{}^{2}}$$

To ensure that jitter does not affect the quantized signal quality, the jitter induced noise (SNRMAXjitter) must be at least 12dB below other substantial noise sources, such as quantization noise, see *Clock Considerations.* Units in picoseconds.

PACKAGE DIMENSIONS



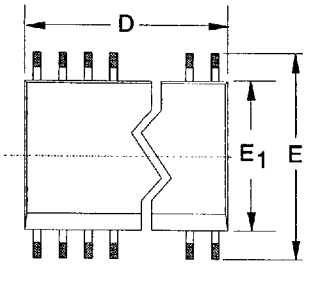
24 pin
Plastic
Skinny DIP



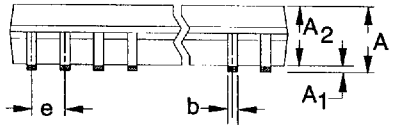
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.94	4.32	4.57	0.155	0.170	0.180
A1	0.51	0.76	1.02	0.020	0.030	0.040
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.02	1.27	1.65	0.040	0.050	0.065
C	0.20	0.25	0.38	0.008	0.010	0.015
D	31.37	31.75	32.13	1.235	1.250	1.265
E1	6.10	6.35	6.60	0.240	0.250	0.260
e1	2.41	2.54	2.67	0.095	0.100	0.105
eA	7.62	-	8.25	0.300	-	0.325
L	3.18	-	3.81	0.125	-	0.150
∝	0°	-	15°	0°	-	15°

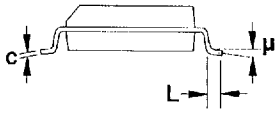
NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION eA TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION E1 DOES NOT INCLUDE MOLD FLASH.



SOIC





pins	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
16	9.91	10.16	10.41	0.390	0.400	0.410
20	12.45	12.70	12.95	0.490	0.500	0.510
24	14.99	15.24	15.50	0.590	0.600	0.610
28	17.53	17.78	18.03	0.690	0.700	0.710

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.41	2.54	2.67	0.095	0.100	0.105
A_1	0.127	-	0.300	0.005	-	0.012
A_2	2.29	2.41	2.54	0.090	0.095	0.100
b	0.33	0.46	0.51	0.013	0.018	0.020
c	0.203	0.280	0.381	0.008	0.011	0.015
D	see table above					
E	10.11	10.41	10.67	0.398	0.410	0.420
E_1	7.42	7.49	7.57	0.292	0.295	0.298
e	1.14	1.27	1.40	0.040	0.050	0.055
L	0.41	-	0.89	0.016	-	0.035
μ	0°	-	8°	0°	-	8°

A Cirrus Logic Company

CDB5030 CDB5031 CDB5032

Evaluation Boards for CS5030, CS5031 & CS5032

Features

- Throughput rates up to 500kHz.
- Operation with on-board or off-board clocks.
- Buffered serial data, 12-bit parallel word, or two 8-bit bytes
- Digital and Analog Patch Areas
- CS5030 ±2.5V input
  CS5031 0V to +5V input
  CS5032 ±2.5V input

General Description

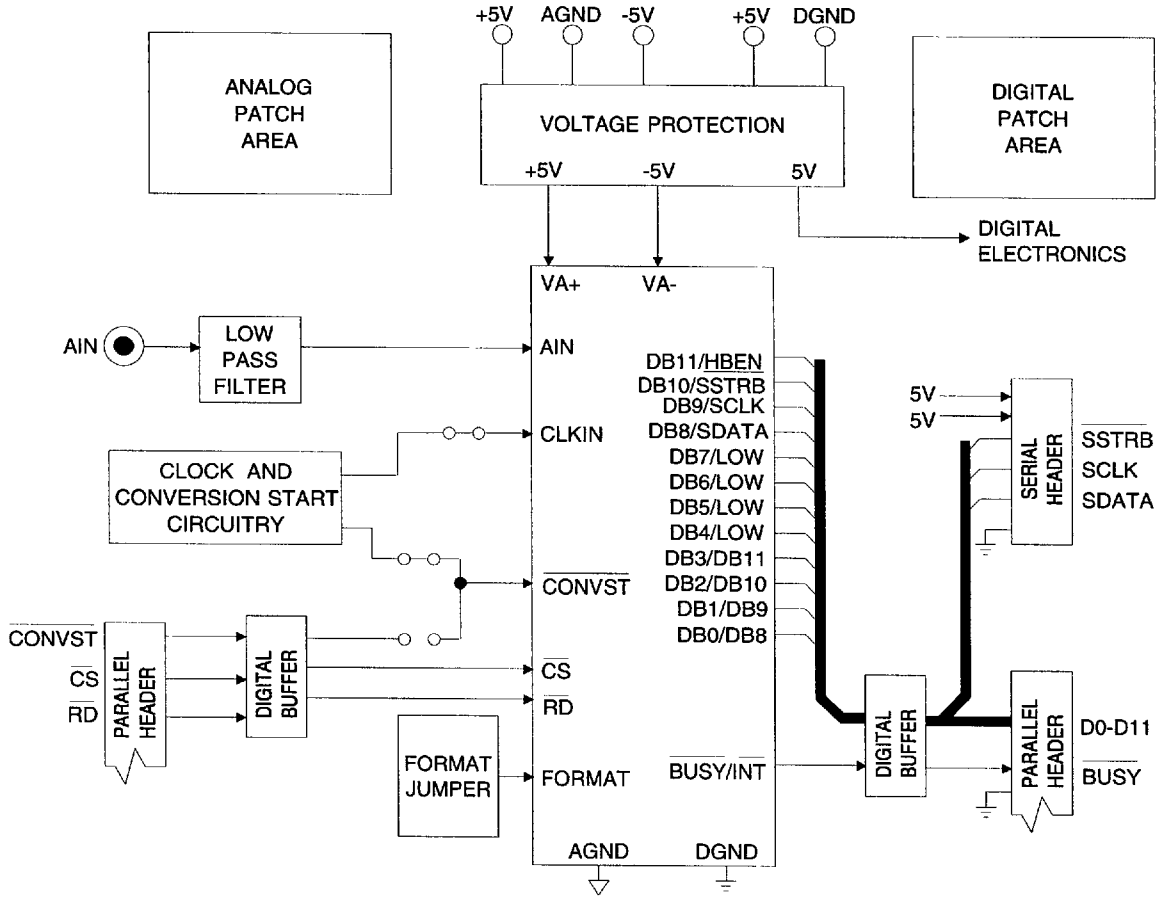
The CDB5030/31/32 Evaluation Boards allow fast evaluation of the CS5030, CS5031 & CS5032 12-bit, 500kHz, sampling A/D Converters.

The board provides a convenient platform for easy circuit development and evaluation. A versatile tool that can simplify design and reduce the design cycle resulting in a quicker time to market.

Analog input is via a BNC connector. Buffered digital outputs are available from the ADC in serial, 12-bit parallel word, or two 8-bit bytes formats.

Ordering Information

CDB5030 Evaluation Board with CS5030-BP Installed
CDB5031 Evaluation Board with CS5031-BP Installed
CDB5032 Evaluation Board with CS5032-BP Installed



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Introduction

The CDB5030, CDB5031, and CDB5032 evaluation boards provide a tool for testing and designing with the CS5030/1/2 series of A/D Converters. The boards are configured for operation from ±5V analog and +5V digital power supplies. A BNC connector is provided for the analog input signal. An on-board jumper selects the output data and serial clock formats. Parallel and serial connectors provide an interface to the digital logic.

Power Supplies

Figure 1 shows the power supply arrangements. ±5V is required to operate the ADC and analog portion of the board. Zener diodes are provided for over-voltage protection. A separate +5V digital supply is required for the digital logic. At least one individual decoupling capacitor is provided for each IC.

Analog Input Circuit

The analog input signal is brought on the evaluation board via the BNC connector J8 (figure 2). Diodes D1 and D2 provide protection against over voltage. R4 and C13 make a low pass filter, whose corner frequency is 318 kHz. Notice that no external trim components are required. R6 is a 10 kΩ terminating resister which provides a load for the signal source. R6 can be changed to match the analog input source impedance if required. The footprint is large enough to accommodate a 50 Ω, 0.5 W resistor.

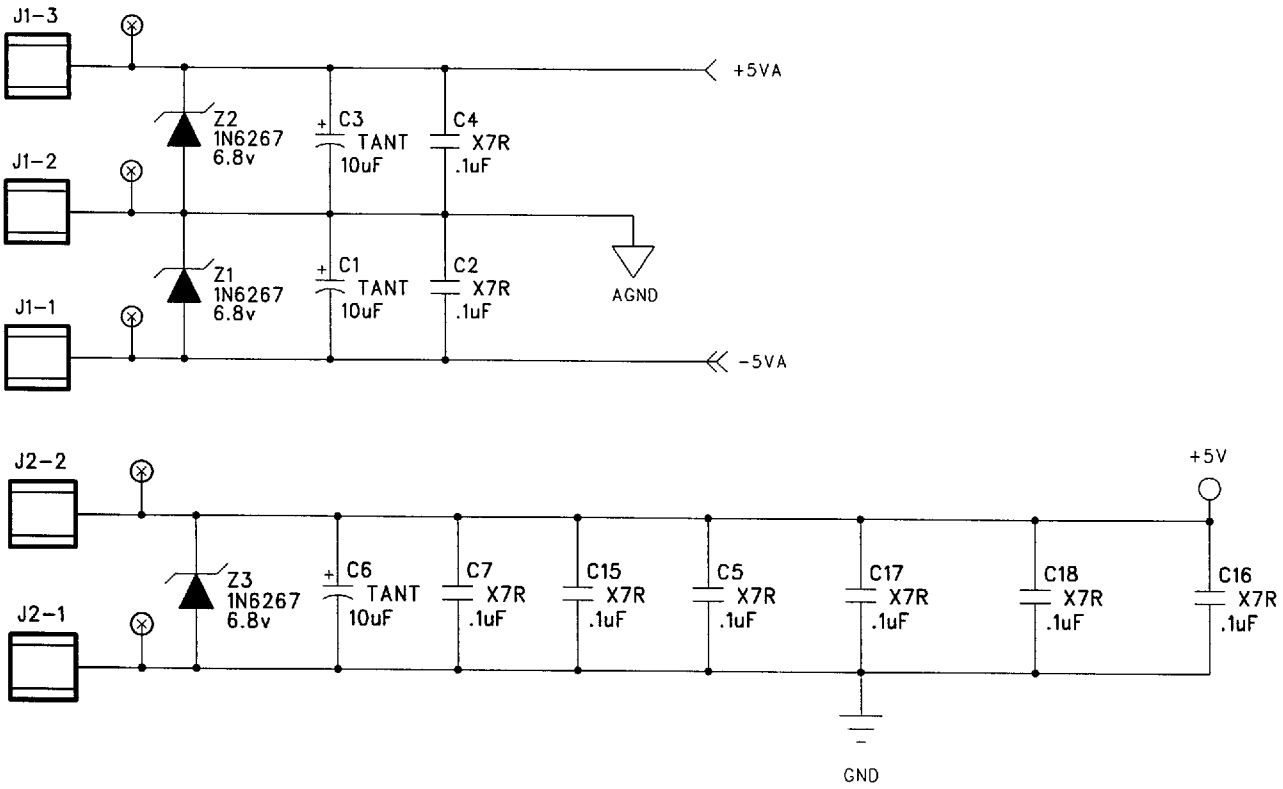


Figure 1. Power Supplies

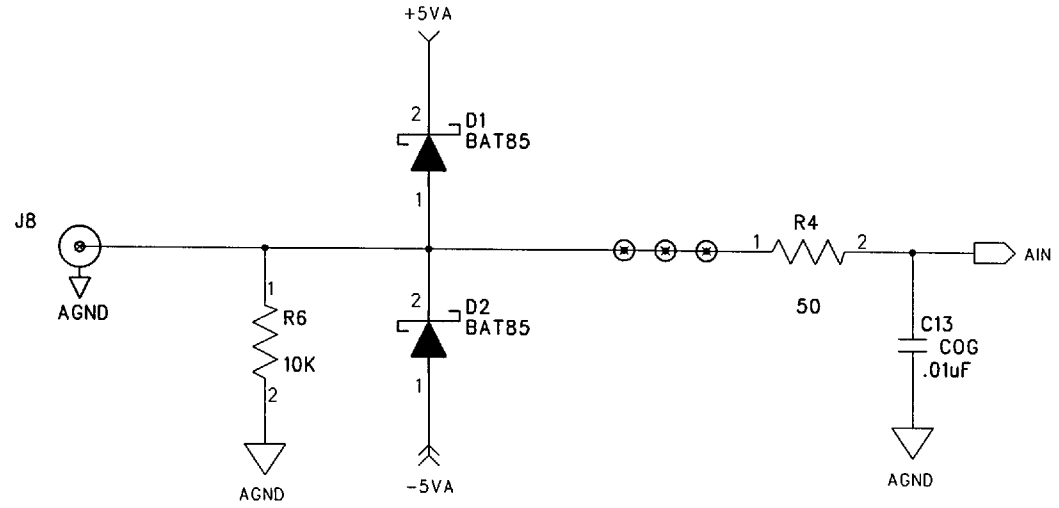


Figure 2. Analog Input Circuit

Clock and Conversion

Figure 3 shows the on-board clock and conversion control circuitry. The evaluation board is designed to run off the on-board 10 MHz oscillator (U4). The ADC can also operate from an internal clock oscillator, by connecting the CLKIN pin to -5VA. Test points are provided to easily implement the internal oscillator.

The $\overline{\text{CONVST}}$ signal on the evaluation board is derived from the on-board 10 MHz clock oscillator. The 10 MHz is divided by 20, providing a 500 kHz signal. External signals can be used by breaking the $\overline{\text{CONVST}}$ jumper at the test points and attaching the external signal at pin 6 of connector J4.

Digital Output Data

The CS5030/31/32 ADCs support three digital output data formats. These include 12-bit parallel, 8-bit byte, and serial interface formats. Several of the ADC output pins have dual roles or modes of operation (see the CS5030/31 or CS5032 data sheets). The position of the "FORMAT" jumper determines which output format is active, with all three formats available through the 40-pin header J4. Serial output data is also available through the 10-pin header J3.

12-Bit Parallel Operation

Selecting the "+" position for the "FORMAT" jumper places the board in 12-bit parallel mode. All parallel output signals are buffered by U1 and U3, and are available on header J4 (figure 4). The rising edge of the $\overline{\text{BUSY}}$ signal, available on pin-40 of J4, can be used to latch the 12-bit parallel data into subsequent digital circuitry.

8-Bit Byte Operation

Selecting the "0" or the "-" position for the "FORMAT" jumper places the board in 8-bit byte mode. The data is available on D0 to D7 of header J4 in two separate read operations. The lower byte is read with HBEN low. The four more significant bits are read with HBEN high. The high byte word includes four leading zeros (D4 to D7) to fill out the remaining four significant bits from the ADC. All byte output signals are buffered by U1 and U3.

Serial Operation

Selecting the "0" or the "-" position for the "FORMAT" jumper also places the board in se-

rial mode. In the "-" position, the serial clock SCLK operates continuously; in the "0" jumper position, the serial clock SCLK is active only when the ADC is outputting serial data. The rising edge of SCLK can be used to latch serial data into subsequent circuitry. The serial data and control lines are available on J3, and the DATA8 (SDATA), DATA9(SCLK), and DATA10 ($\overline{\text{SSTRB}}$) lines of J4. All serial output signals are buffered by U1.

Convert Start Operation

MODE 1 Operation

The $\overline{\text{CONVST}}$ signal is used to put the ADC into hold mode and initiate a conversion. At the end of the conversion, the ADC returns to its tracking mode. Conversion begins on the rising edge of the $\overline{\text{CONVST}}$, provided that $\overline{\text{CS}}$ is high (note that external pull-up resistors on $\overline{\text{CS}}$ and $\overline{\text{RD}}$ default both to logic high if no external logic signal is present for these pins on the J4 header). The $\overline{\text{BUSY}}$ line on J4, which goes low when the output data becomes available, can be used as a microprocessor interrupt. Bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low allows data to be read from the ADC and also resets $\overline{\text{BUSY}}$ high. $\overline{\text{CONVST}}$ must be high when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are brought low in this mode. Data cannot be read during the conversion cycle because the ADC output latches are disabled during this process.

MODE 2 Operation

In this mode, $\overline{\text{CONVST}}$ is held permanently low (Break $\overline{\text{CONVST}}$ jumper at the test points and add jumper between $\overline{\text{CONST\_BUF}}$ and $\overline{\text{CONVST}}$. Ground the HOLD signal J4-6). Bringing $\overline{\text{CS}}$ low (while HBEN is low) through the J4 header, puts the ADC into hold mode and initiates a conversion. The $\overline{\text{BUSY}}$ line on J4 goes low at the start of the conversion and returns high at the end of conversion.

FORMAT JUMPER

+	12-bit parallel mode
0	8-bit byte or serial (16 bit SCLK))
-	8-bit byte or serial (continuous SCLK)

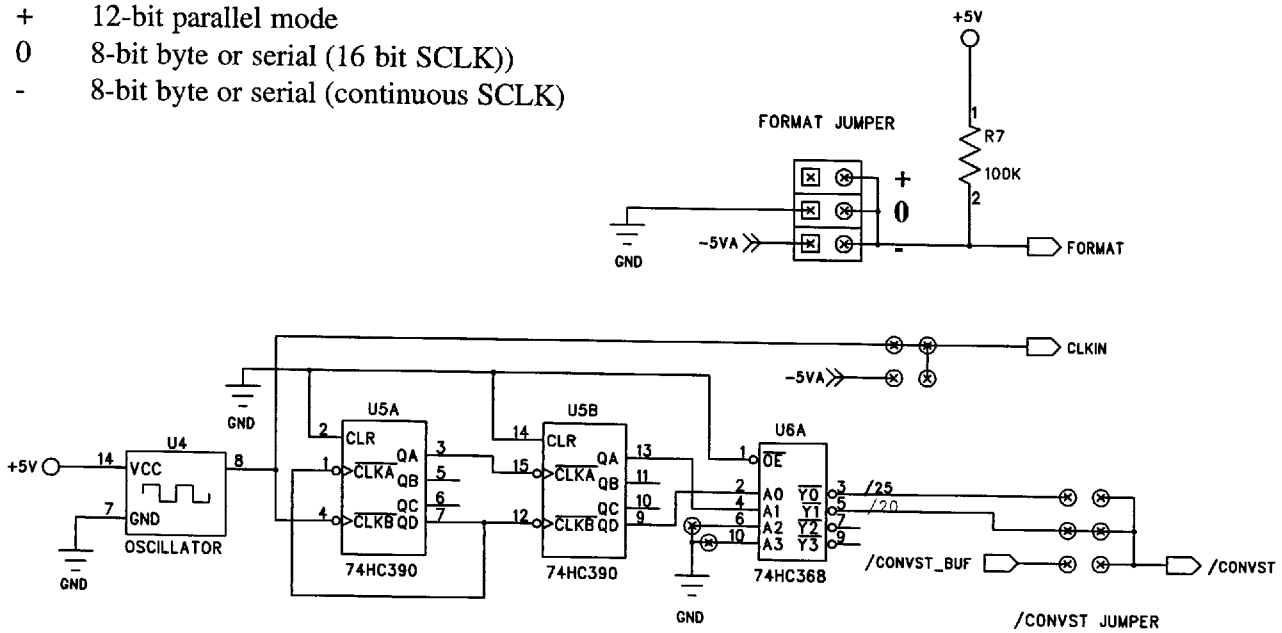


Figure 3. Clock and Convert Start Circuitry

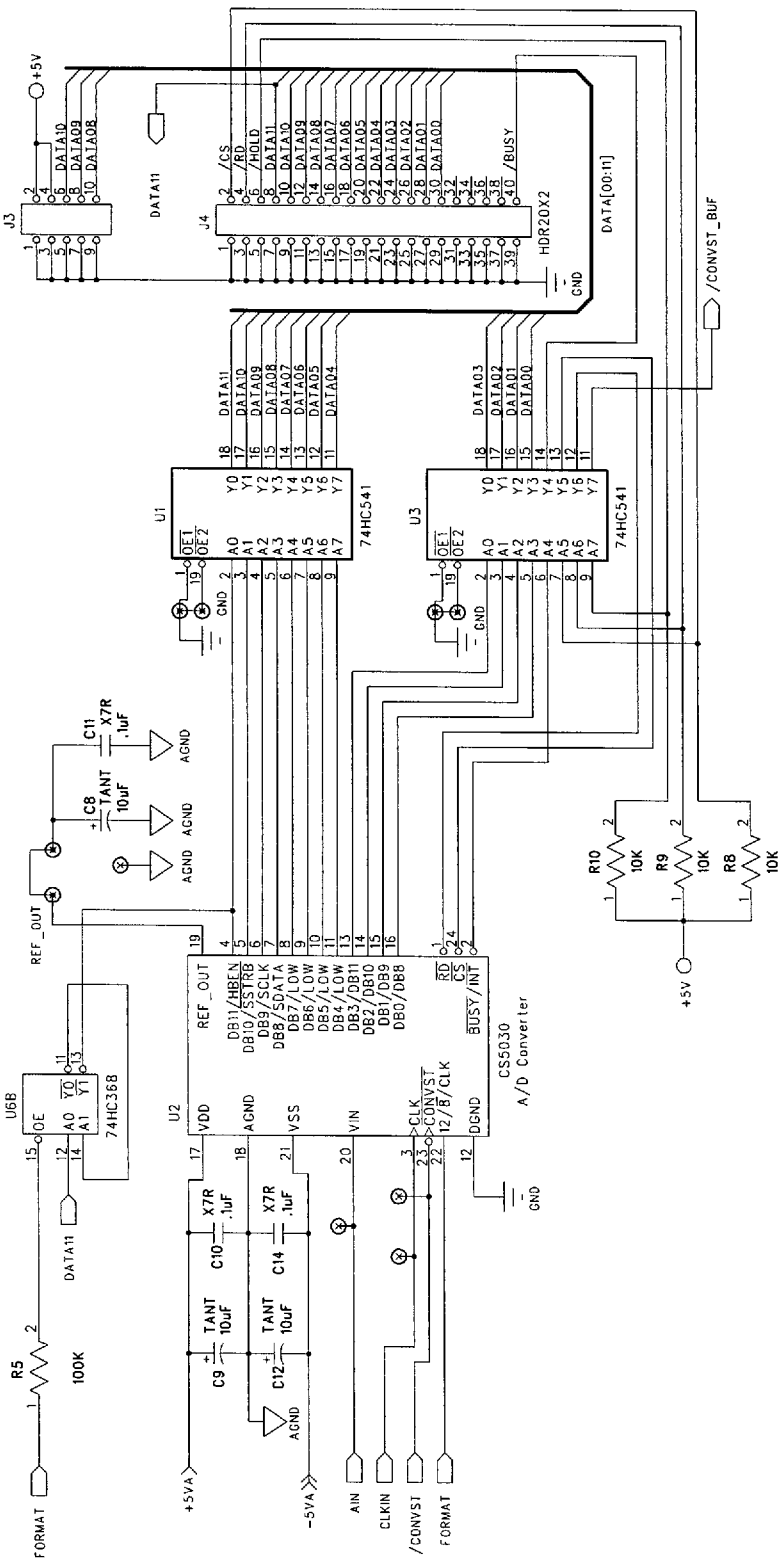


Figure 4. ADC Connections and Digital Output

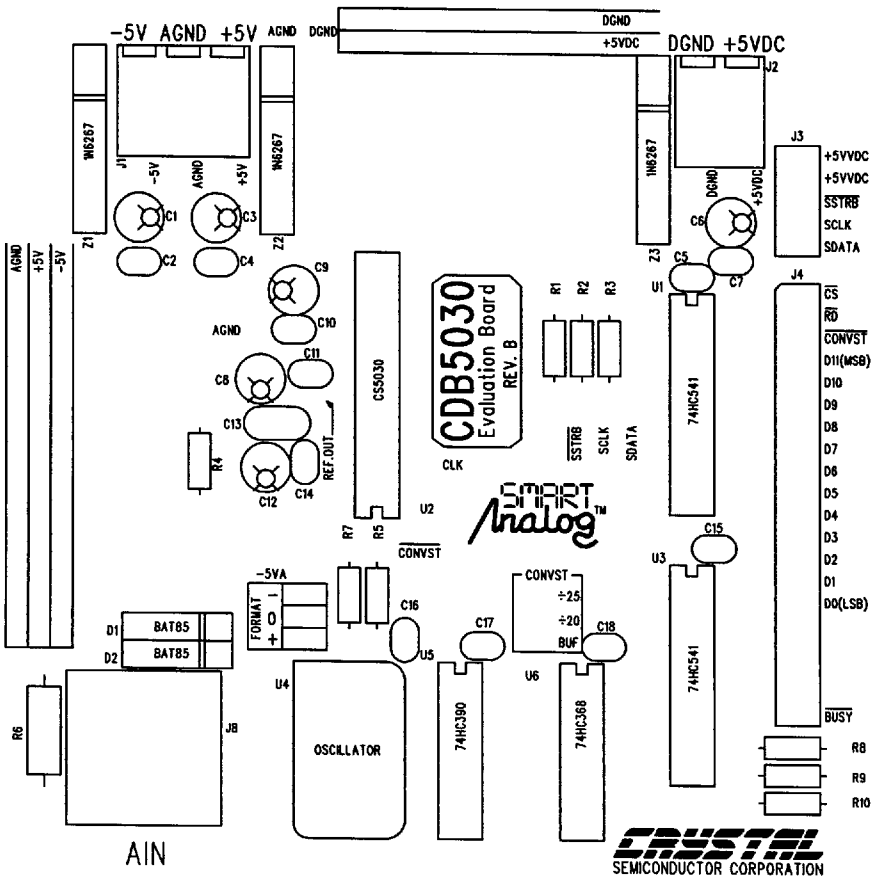


Figure 5. CDB5030/CDB5031/CDB5032 Component Layout

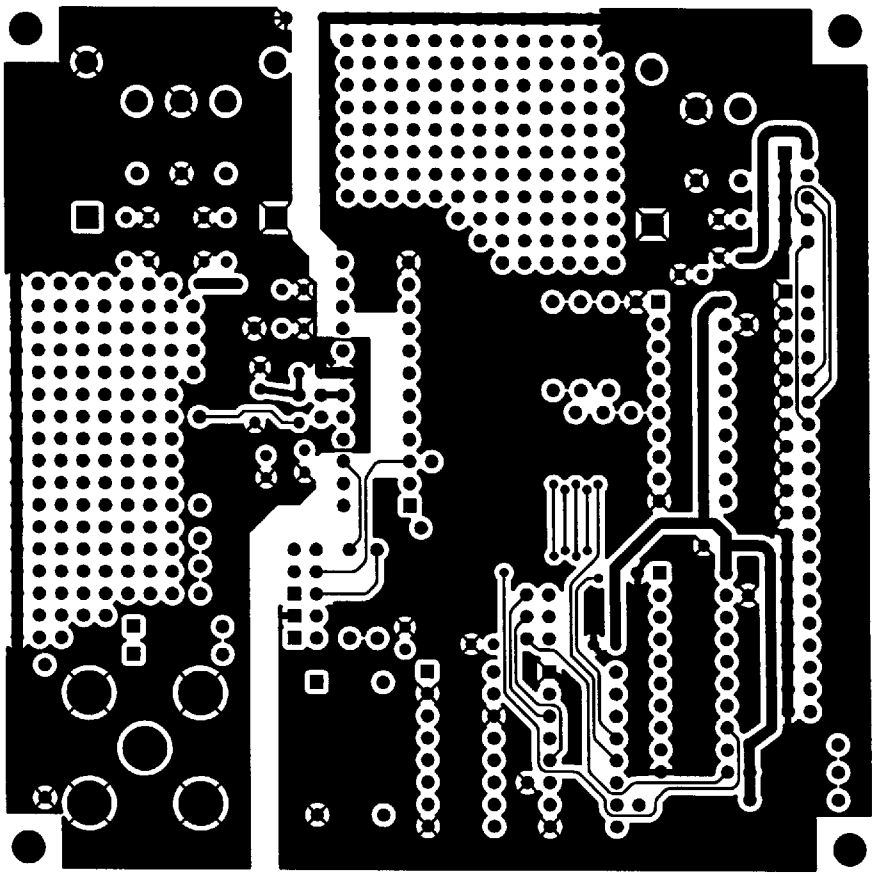


Figure 6. Top Ground Plane Layer (NOT TO SCALE)

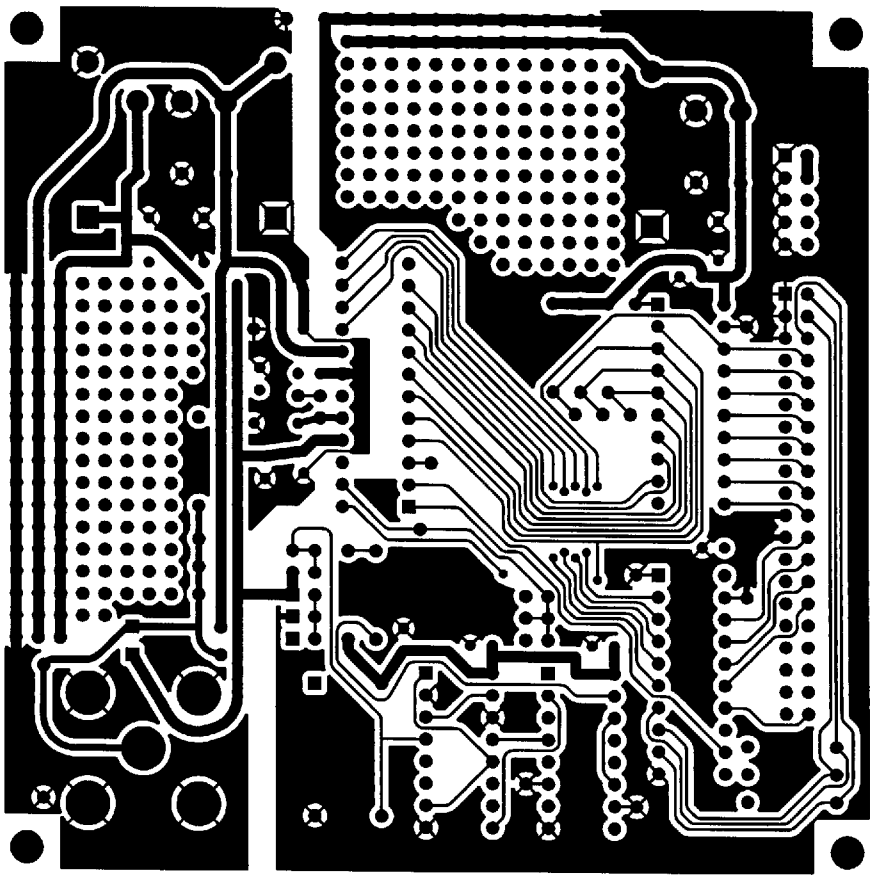


Figure 7. Bottom Trace Layer (NOT TO SCALE)