AK4318

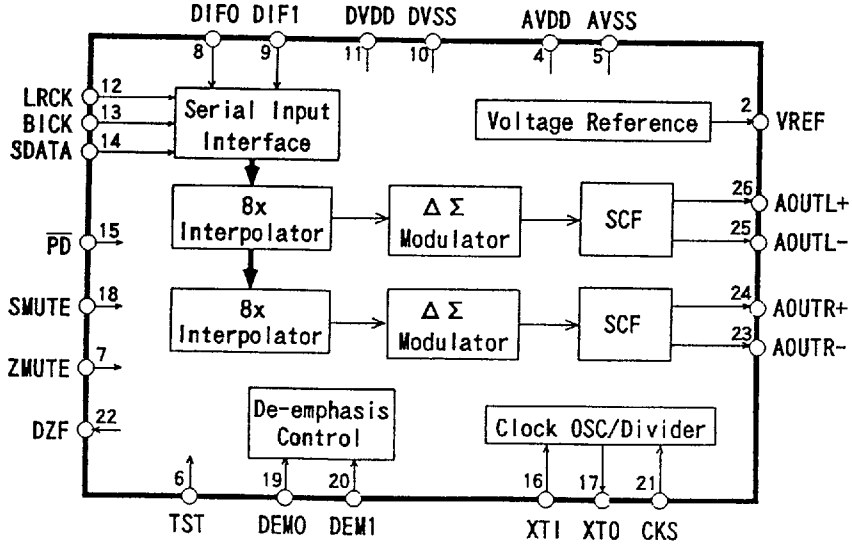
18Bit Stereo Δ Σ DAC for Digital Audio

General Description

The AK4318 i a high performance 1bit stereo DAC for digital audio systems. A 1bit DAC can achieve monotonicity and low distortion with no adjustment and is superior to traditional R-2R ladder based DACs. In the AK4318, the loss of accuracy from clock jitter is also improved by using SCF techniques for on-chip post filter. The AK4318 includes digital de-emphasis filter corresponding to 3 sampling frequencies and soft mute. The master clock can be either 256fs or 384fs, supporting various audio environment. The AK4318 is ideal for digital broadcasting application, DBS, CATV and digital recording application, DAT, MD, DCC etc.

Features

- ☐ High Performance Stereo 1bit DAC
- ☐ 64 times Oversampling
- ☐ On chip 8 times Interpolation Filter
- ☐ On chip Post Filter (SCF)
- ☐ High Tolerance to Clock Jitter
- ☐ Digital de-emphasis for 32, 44.1, 48kHz sampling
- ☐ Soft mute
- ☐ Master Clock: 256fs or 384fs
- ☐ THD+N: -92dB
- ☐ Dynamic Range, S/N: 97dB
- ☐ 28pin SOP Pakage

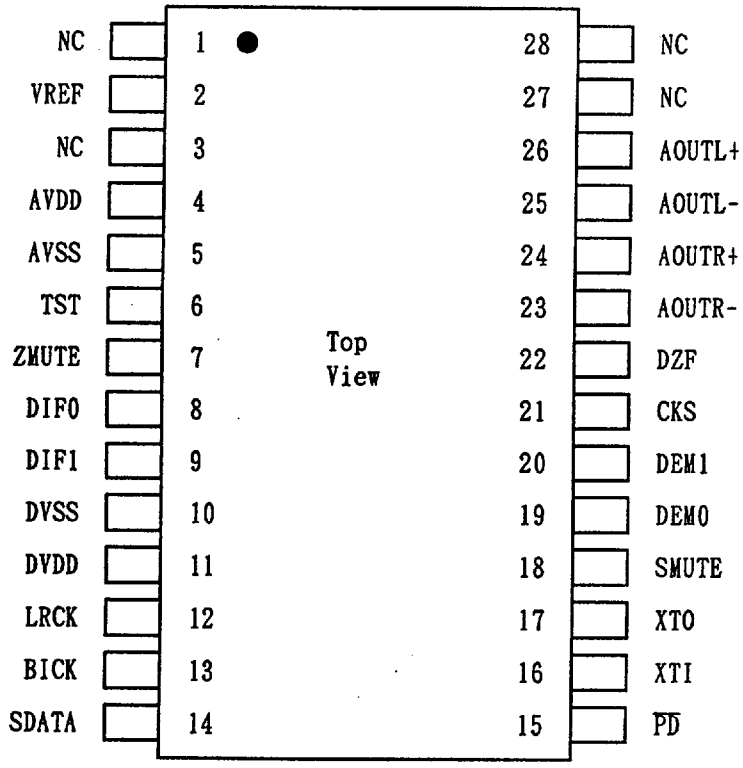


0983635 0001204 390

■ Ordering Guide

AK4318-VS	-10～+70℃	28pin SOP(1.27mm pitch)
AK4318-VM	-10～+70℃	28pin SSOP(0.65mm pitch)
AKD4318	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
2	VREF	O	Voltage Reference Output Pin, (AVDD)-3.6V Normally connected to AVDD with a 0.1uF ceramic capacitor in parallel with a 10uF electrolytic capacitor.
4	AVDD	-	Analog Supply, +5V
5	AVSS	-	Analog Ground Pin
6	TST	I	Test Pin (Pull-down pin) Must be left floating or tied to DGND.
7	ZMUTE	I	ZERO Mute Pin (Pull-down pin) When "H", analog outputs are muted by zero detection.
8 9	DIF0 DIF1	I I	Digital Input Format Pins These two pins select one of four formats for the incoming serial data stream.
10	DVSS	-	Digital Ground Pin
11	DVDD	-	Digital Power Supply Pin, +5V
12	LRCK	I	L/R Clock Pin This input determines which channel is currently being input on the Serial Data Input pin, SDATA. "H": Lch, "L": Rch
13	BICK	I	Serial Data Clock Pin This clock is used to latch SDATA.
14	SDATA	I	Serial Data Input Pin 2's complement MSB-first data is input on this pin.
15	$\overline{PD}$	I	Power-Down Pin When "L", the AK4318 is in power-down mode and is held in reset. The AK4318 should always be reset upon power-up.
16	XTI	I	Master Clock Input Pin A crystal can be connected between this pin and XTO, or an external CMOS clock can be input on XTI. The fs is selected by CKS pin.
17	XTO	O	Crystal Oscillator Output Pin When a crystal is used, it is tied between this pin and XTI. When an external clock is input, this pin should be left floating.
18	SMUTE	I	Soft Mute Pin (Pull-down pin) When this pin goes "H", soft mute cycle is initiated. When returning "L", the output mute releases.
19 20	DEM0 DEM1	I I	De-emphasis Mode Pins This function corresponds to 3 types of sampling rate.
21	CKS	I	Master Clock Select Pin (Pull-down pin) "L": XTI=256fs, "H": XTI=384fs
22	DZF	O	Zero Input Detect Pin When SDATA of both channels follow a total 8192 LRCK cycles with "0" input data, this pin goes "H".
23	AOUTR-	O	Rch analog negative output pin
24	AOUTR+	O	Rch analog positive output pin
25	AOUTL-	O	Lch analog negative output pin
26	AOUTL+	O	Lch analog positive output pin

* All pins except the above pins are NC pins. These pins are not bonded internally.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supplies: Analog	AVDD	-0.3	6.0	V
Digital	DVDD	-0.3	AVDD	V
Input Current, Any Pin Except Supplies	I_{IN}	-	±10	mA
Input Voltage	V_{IND}	-0.3	DVDD+0.3	V
Ambient Operating Temperature	Ta	-10	70	℃
Storage Temperature	Tstg	-65	150	℃

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supplies: Analog	AVDD	4.5	5.0	5.5	V
Digital	DVDD	4.5	5.0	AVDD	V

Notes: 1. All voltages with respect to ground.

* Specifications are subject to change without notice.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25℃; AVDD,DVDD=5.0V; fs=48kHz; Signal Frequency=1kHz; 18bit Input Data; Differential Outputs; Measurement Bandwidth=10Hz～20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
Resolution				18	Bits
Dynamic Characteristics (Please refer to the measuring system section)					
THD+N (0dB Output)	(Note 2)	0.005	0.0025		%
		-86	-92		dB
Dynamic Range (-60dB Output)	(Note 3)	90	97		dB
S/N	(Note 4)	90	97		dB
S/N at Muting (ZMUTE="H")	(Note 4)		110		dB
Interchannel Isolation		90	100		dB
Interchannel Gain Mismatch			0.1		dB
DC Accuracy					
Gain Drift			60		ppm/℃
Output Voltage Range	(Note 5)	±2.20	±2.35	±2.50	Vp-p
Power Supplies					
Power Supply Current					
Normal Operation ($\overline{PD}$="H")	AVDD		17	25	mA
	DVDD		6	9	mA
Power-Down-Mode ($\overline{PD}$="L")	AVDD+DVDD		20		uA
Power Dissipation (AVDD+DVDD)					
Normal Operation			115	170	mW
Power-Down-Mode			0.1		mW
Power Supply Rejection			40		dB

Notes:2. Inverse of S/(N+D).
3. A-weighted. 96dB(typ) at 16bit input data.
4. A-weighted. Digital input all zeros.
5. Summation of the differential outputs, (AOUT+)-(AOUT-). $R_L \geqq 10k\Omega$

FILTER CHARACTERISTICS

(Ta=25℃; AVDD,DVDD=5.0V±10%; fs=48kHz; DEM0="1",DEM1="0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband	±0.04dB (Note 6)	PB	0		21.3	kHz
	-0.23dB		0		21.7	kHz
	-6.0dB		0		24.0	kHz
Stopband	(Note 6)	SB	26.3			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	45			dB
Group Delay	(Note 7)	GD		14.7		1/fs
2nd Order SCF						
Frequency Response	20kHz			-0.04		dB
	24kHz			-0.32		dB
	48kHz			-6.0		dB

Note: 6. The passband and stopband frequencies scale with fs.
For example, PB=0.452*fs(@±0.23dB), SB=0.548*fs.
7. The calculating delay time which occurred by digital filtering. This time is from setting the 18bit data of both channels to input register to the output of analog signal.

DIGITAL CHARACTERISTICS

(Ta=25℃; AVDD, DVDD=5.0V±10%)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		V_{IH}	70%DVDD	-	-	V
Low-Level Input Voltage		V_{IL}	-	-	30%DVDD	V
High-Level Output Voltage	Iout=-20uA	V_{OH}	DVDD-0.1	-	-	V
Low-Level Output Voltage	Iout=20uA	V_{OL}	-	-	0.1	V
Input Leakage Current	(Note 8)	Iin	-	-	±10	uA

Note: 8. TST, ZMUTE, SMUTE, CKS pins have internal pull-down devices, nominally 90kΩ.

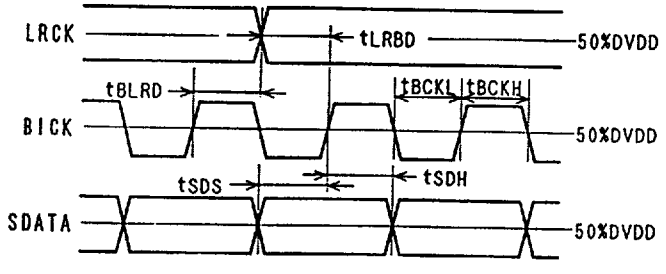
SWITCHING CHARACTERISTICS

(Ta=25℃; AVDD, DVDD=5.0V±10%; C_L=20pF)

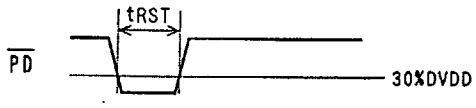
Parameter		Symbol	min	typ	max	Unit
Control Clock Frequency						
Crystal Resonator	256fs:	f_{CLK}	7.10	12.288	13.9	MHz
	384fs:	f_{CLK}	10.70	18.432	20.7	MHz
External Clock	256fs:	f_{CLK}	2.56	12.288	13.9	MHz
	Pulse Width Low	t_{CLKL}	28			ns
	Pulse Width High	t_{CLKH}	28			ns
	384fs:	f_{CLK}	3.84	18.432	20.7	MHz
	Pulse Width Low	t_{CLKL}	20			ns
	Pulse Width High	t_{CLKH}	20			ns
LRCK Frequency		fs	10	48	54	kHz
Serial Interface Timing	(Note 9)					
BICK Period		t_{BCK}	290			ns
BICK Pulse Width Low		t_{BCKL}	100			ns
Pulse Width High		t_{BCKH}	100			ns
BICK rising to LRCK edge	(Note 10)	t_{BLRD}	40			ns
LRCK Edge to BICK rising	(Note 10)	t_{LRBD}	40			ns
SDATA Hold Time		t_{SDH}	40			ns
SDATA Setup Time		t_{SDS}	40			ns
Reset Timing						
PD Pulse Width	(Note 11)	t_{RST}	100			ns

Notes: 9. Refer to the operating overview section "Serial Data Interface".
10. SCLK rising edge must not occur at the same time as L/$\overline{R}$ edge.
11. AK4318 can be reset by bringing $\overline{PD}$ "L" to "H" only upon power up.

■ Timing Diagram



Data Input Timing



Reset Timing

THEORY OF OPERATION

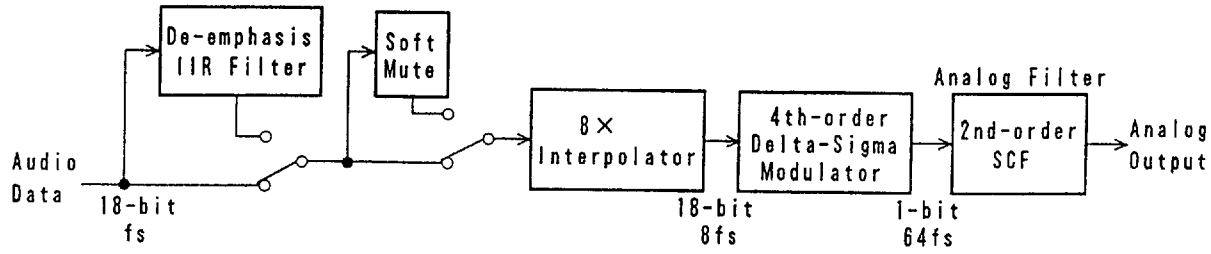


Figure 1. AK4318 Architecture

Audio data is input to the AK4318 digital interpolation filter which removes images of the input signal frequency, fs(Figure 2). Following the interpolation stage, the resulting frequency spectrum has images of the input signal at multiples of eight times the input sample frequency, 8×fs (Figure 3). Eliminating the images between fs and 8×fs greatly relaxes the requirements of the analog filtering, allowing the suppression of images while leaving the audio band of interest unaltered.

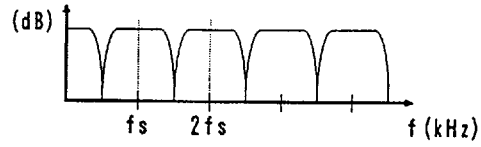


Figure 2. Input Data Spectrum

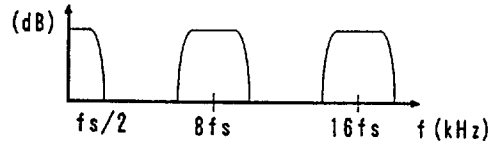


Figure 3. 8X Interpolated Data Spectrum

The AK4318 interpolation stage is followed by a sample-and-hold function where the data points from the interpolator are held for eight(64×fs) clock cycles. The resulting frequency response is a sinx/x characteristics with zeros at 8×fs multiples. The sinx/x zeros completely attenuate signal at 8×fs and largely suppress the remaining energy of the images. The 8× interpolation followed by the 8× sample-and-hold results in data at a rate of 64×fs.

The delta-sigma modulator takes in the 64×fs data and performs 4th order noise shaping. In the digital modulator of the AK4318, 18bit audio data is modulated to a 1-bit, 64×fs signal. The 4th order noise shaper allows 1-bit quantization to support 18-bit audio processing by suppressing quantization noise in the bandwidth of interest. Figure 4 shows the frequency spectrum of the modulator output.

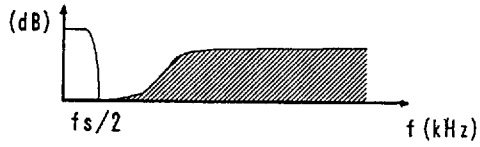


Figure 4. Modulator Output Spectrum

The AK4318's digital modulator is followed by a D-to-A converter that translates the 1-bit signal into a series of charge packets. The magnitude of the charge in each packet is determined by sampling of a voltage reference onto a switched capacitor, where the polarity of each packet is controlled by the 1-bit signal. The result is a 1-bit D/A conversion process that is very insensitive to clock jitter. This is a major improvement over previous generations of 1-bit D/A converters where the magnitude of charge in the D/A process is determined by switching a current reference for a period of time defined by periods of the master clock.

OPERATION OVERVIEW

■ System Clock Input

The external clocks which are required to operate the AK4318 are XTI(256fs/384fs), LRCK(fs), BICK(32fs~). The master clock (XTI) should be synchronized with LRCK but the phase is free of care. The XTI is used to operate the digital interpolation filter and the delta-sigma modulator. The frequency of XTI is determined by the sampling rate(LRCK), and the setting of the Clock Select, CKS pin. Setting CKS "L" selects an XTI frequency of 256fs while setting CKS "H" selects 384fs. When the 384fs is selected, the internal master clock becomes 256fs(=384fs*2/3).

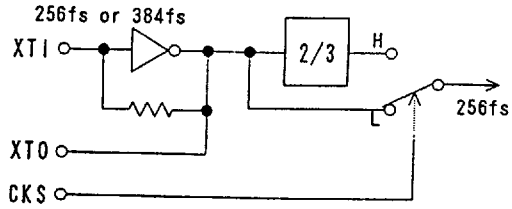


Figure 5. Internal Clock Circuit

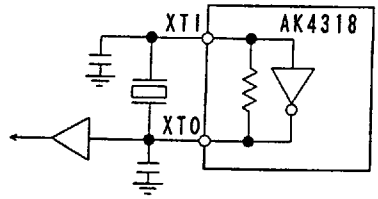


Figure 6. Crystal resonator connection

The master clock can be either a crystal resonator placed across the XTI and XTO pin, or external clock input to the XTI pin with the XTO pin left floating. Not only CMOS clock but sine wave signal with 1Vp-p can be input to the XTI pin by AC coupling. Table 1 illustrates standard audio word rates and corresponding frequencies used in the DAC.

LRCK (fs) (kHz)	CKS	XTI (MHz)
32.0	L	8.1920
	H	12.2880
44.1	L	11.2896
	H	16.9344
48.0	L	12.2880
	H	18.4320

Table 1. Examples of System Clock

As the AK4318 includes the phase detect circuit for LRCK, the AK4318 is reset automatically when the synchronization is out of phase by changing the clock frequencies. Therefore, the reset is not needed except only upon power-up. (Please refer to the "System Reset" section.)

All external clocks(XTI, BICK, LRCK) should always be present whenever the AK4318 is in normal operation mode($\overline{PD}$="H"). If these clocks are not provided, the AK4318 may draw excess current and do not possibly operate properly because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4318 should be in the power-down mode($\overline{PD}$="L").

■ Serial Data Interface

Data is input to the AK4318 via three serial input pins(SDATA, BICK, LRCK). The AK4318 supports four serial data formats which can be selected via DIF0 and DIF1 pins(Table 2). Format 0 is compatible with existing 16-bit DACs and digital filters. Format 1 is an 18-bit version of format 0. Format 2 is similar to AKM ADCs (AK5339/40/45/89/90) and many DSP serial ports. Format 3 is compatible with the I²S serial data protocol. Format 2 and 3 support 18-bit input or 16-bit followed by two zeros. In all serial input modes, the serial data is MSB-first and 2's complement format.

DIF1	DIF0	Mode	Fig
0	0	0: LSB Justified, 16bit	7
0	1	1: LSB Justified, 18bit	7
1	0	2: MSB Justified, 16-18bit	8
1	1	3: I²S Compatible	9

Table 2. Digital Input Formats

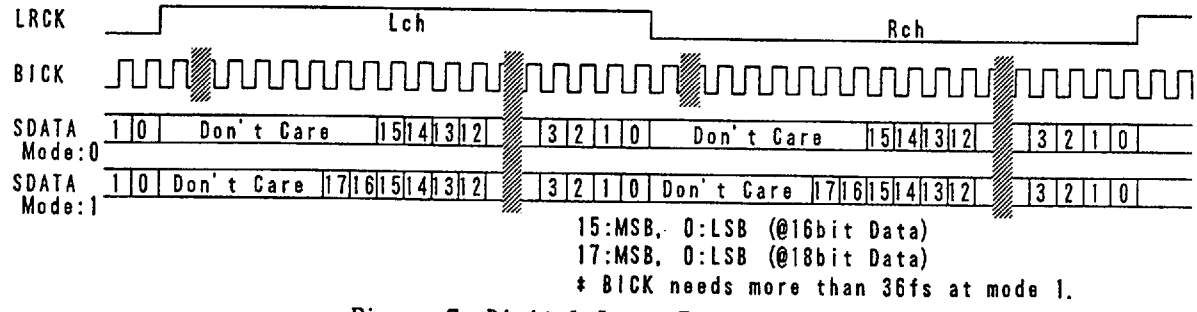


Figure 7. Digital Input Formats 0 & 1

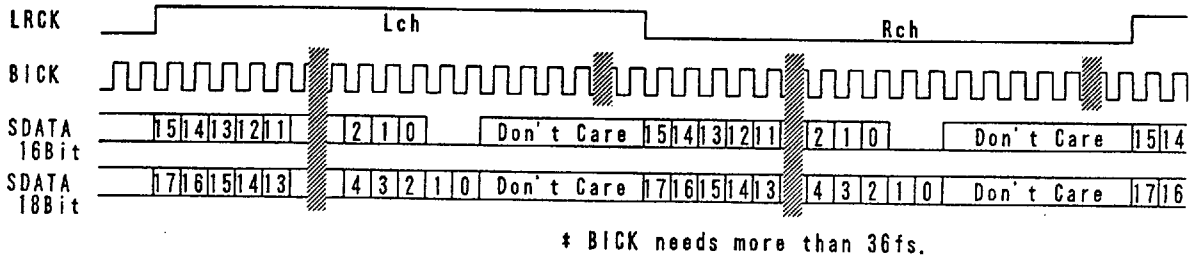


Figure 8. Digital Input Format 2

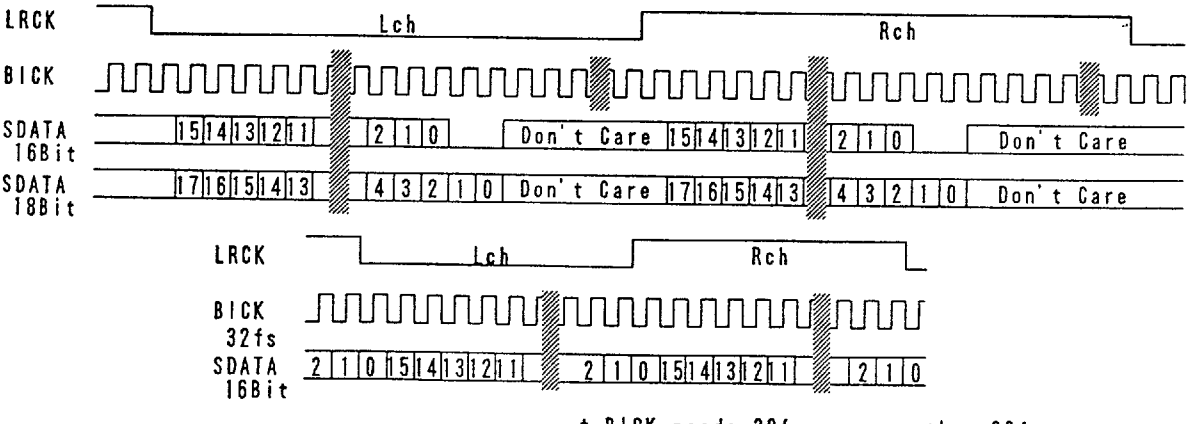


Figure 9. Digital Input Format 3

■ De-emphasis filter

The AK4318 includes the digital de-emphasis filter(tc=50/15us) by IIR filter. This filter corresponds to three sampling frequencies(32kHz, 44.1kHz, 48kHz). The de-emphasis filter selected by DEM0 and DEM1 is enabled for input audio data. The de-emphasis is also disabled at DEM0="1" and DEM1="0".

DEM1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

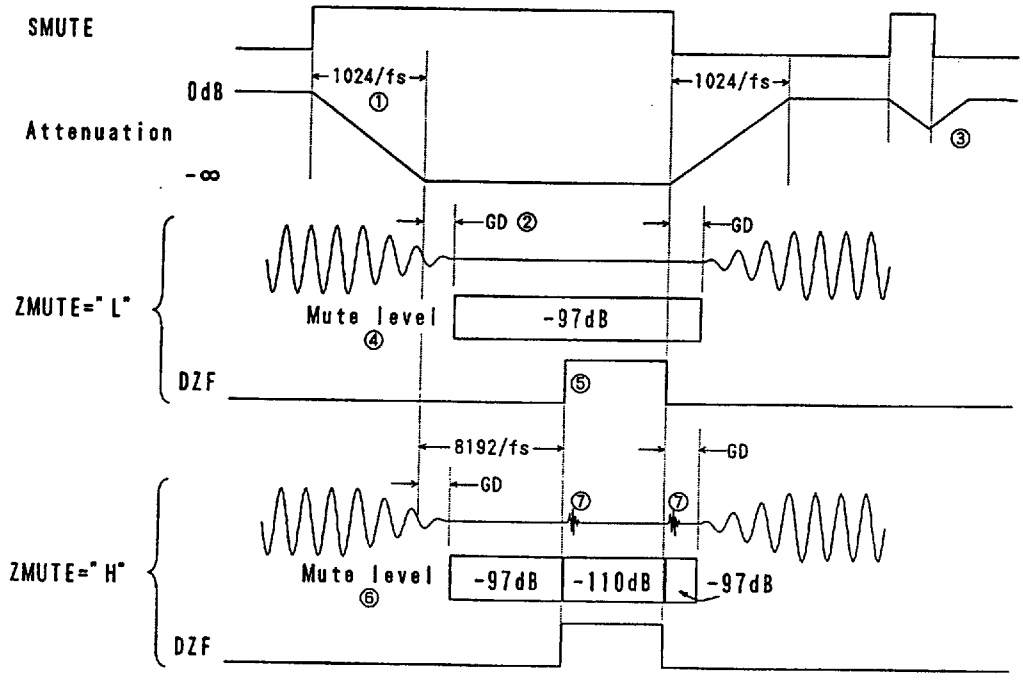
Table 3. De-emphasis filter control

■ Zero detection & Zero mute operation

When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF immediately goes "L" if input data are not zero after going DZF "H". Analog outputs condition at zero detection depends on the setting of ZMUTE pin. If ZMUTE is "H", analog outputs are muted by zero detection. When ZMUTE is "L", Analog outputs aren't muted by zero detection. When muting, the noise level on analog outputs is reduced up to the system noise level and the S/N is improved. However, the click noise occurs at the edges("↑ ↓") of DZF signal(⑦ in Figure 10).

■ Soft mute operation

When SMUTE goes "H", the output signal is attenuated by -∞ during 1024 LRCK cycles. If ZMUTE is set "H" at the same time, analog outputs are muted by zero detection. When SMUTE is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmmision.



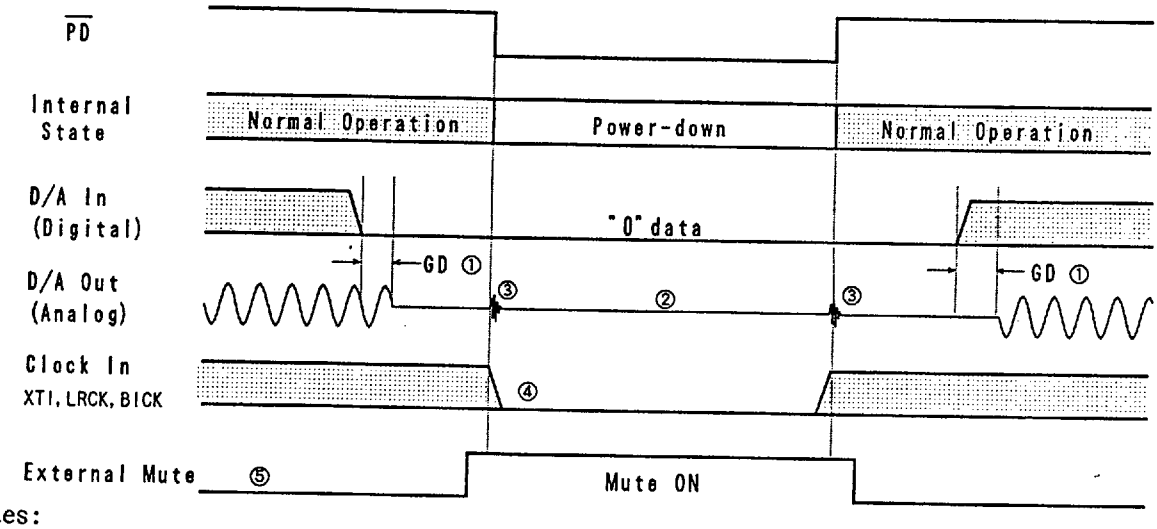
Notes:

①The output signal is attenuated by -∞ during 1024 LRCK cycles(1024/fs).
②Analog output corresponding to digital input have the group delay(GD).
③If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.
④As analog outputs aren't muted at ZMUTE "L", the noise level on analog outputs is -97dB.
⑤When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF immediately goes "L" if input data are not zero after going DZF "H".
⑥As analog outputs are muted at ZMUTE "H", the noise level on analog outputs is about -110dB.
⑦Click noise about -50dB occurs at the edges("↑ ↓") of DZF signal. Please mute the analog output externally if the click noise influences system application(Figure 12).

Figure 10. Soft mute and zero detection

■ Power-Down

The AK4318 are placed in the power-down mode by bringing $\overline{PD}$ pin "L" and the analog outputs are floating(Hi-Z). Figure 11 shows an example of the system timing at the power-down and power-up.



Notes:

①Analog output corresponding to digital input have the group delay(GD).
②Analog outputs are floating(Hi-Z) at the power-down mode. The output noise level is about -110dB.
③Click noise about -50dB occurs at the edges("↑ ↓") of $\overline{PD}$ signal.
④When the external clocks(XTI, BICK, LRCK) are stopped, the AK4318 should be in the power-down mode.
⑤Please mute the analog output externally if the click noise(③) influences system application. The timing example is shown in this figure. Please refer to Figure 12.

Figure 11. Power-down/up sequence example

■ System Reset

The AK4318 should be reset once by bringing $\overline{PD}$ "L" upon power-up. The internal timing starts clocking by LRCK "↑" upon exiting reset.

If the phase difference between LRCK and internal control signals is larger than +1/16～-1/16 of word period(1/fs), the synchronization of internal control signals with LRCK is done automatically at the first rising edge of LRCK. Since RAM address shifts during this synchronization, correct data would not be output until 18 sampled data are input.

■ External mute circuit

Some click noise may occur at the edges("↑ ↓") of $\overline{PD}$ signal and the zero detection with ZMUTE="H". The click noise which occurs at the edges("↑ ↓") of $\overline{PD}$ signal can be avoided by controlling the external mute circuit using the signal like ⑤ in Figure 11. The click noise at the zero detection can be also avoided by muting the analog outputs using DZF signal. The external mute circuit example is shown in Figure 12.

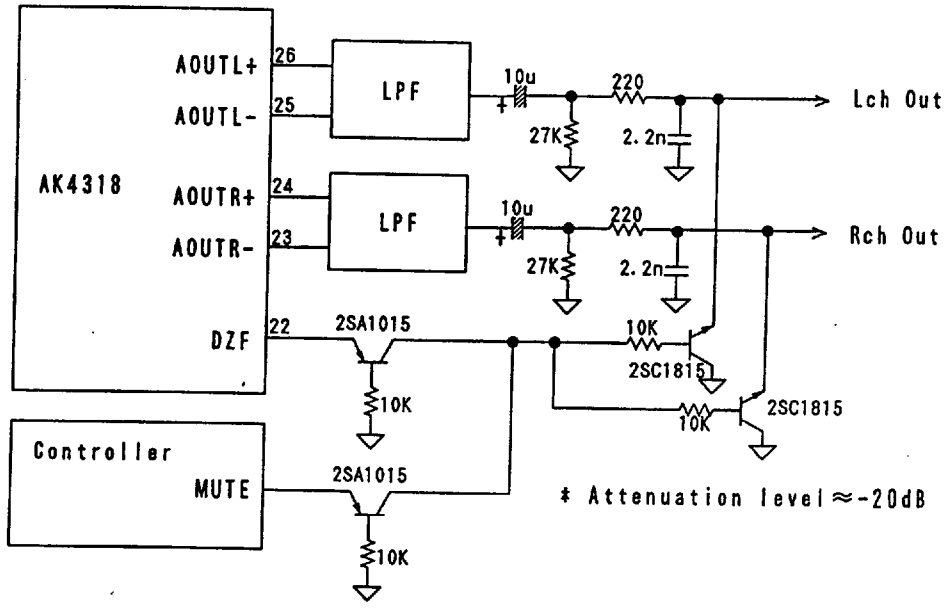


Figure 12. External mute circuit example

SYSTEM DESIGN

Figure 13 shows the system connection diagram. The examples of external analog filter are shown in Figure 15. An evaluation board[AKD4318] is available which demonstrates the optimum layout and power supply arrangements.

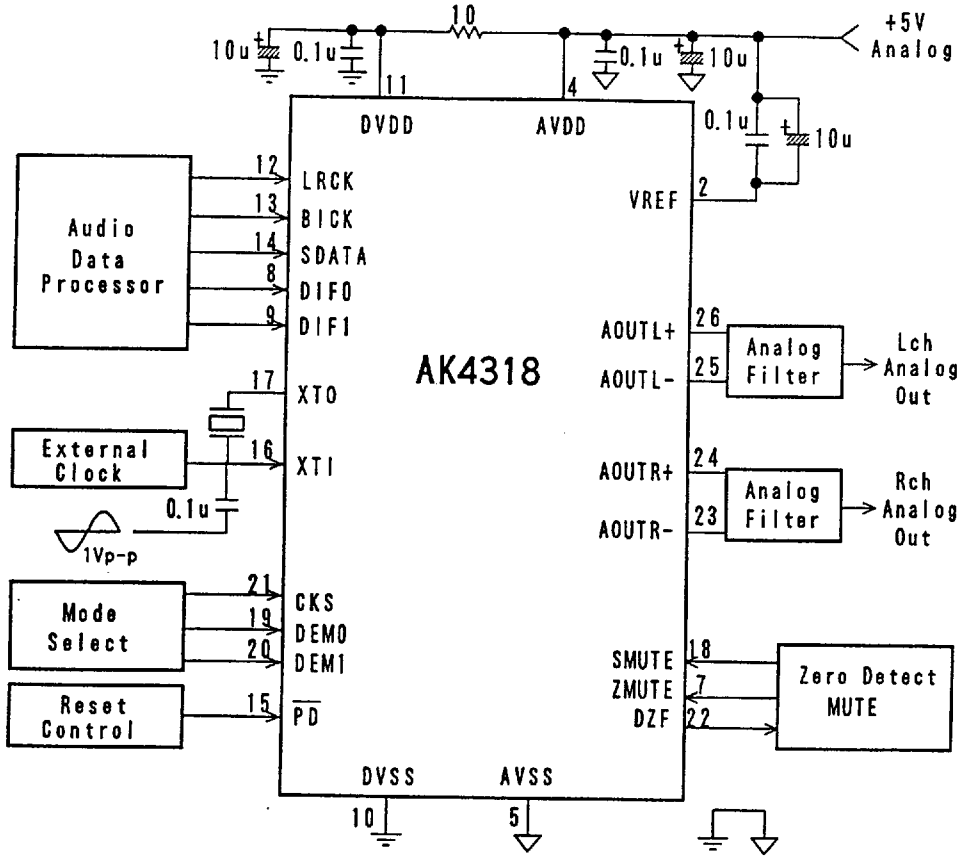


Figure 13. Typical Connection Diagram

■ System design consideration

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. AVDD is supplied from analog supply in system and DVDD is supplied from AVDD via 10Ω resistor. Decoupling capacitors should be as near to the AK4318 device as possible, with the low value ceramic capacitor being the nearest.

2. On-chip voltage reference

The on-chip voltage reference is output on the VREF pin. An electrolytic capacitor less than 10uF in parallel with a 0.1uF ceramic capacitor attached to this pin eliminates the effects of high frequency noise. Especially, the ceramic capacitor should be connected to VREF pin within a few mm as near as possible. No load current may be driven from the VREF output pin. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the AK4318.

3. Output analog filter circuit

The analog signals are output from the differential output pins of each channel. The both outputs are summed externally. The analog outputs are the differential voltage, ΔV_{AOUT}=(AOUT+)-(AOUT-) between AOUT+ and AOUT-. The bias voltage of the external summing circuit is supplied externally. The output signal range is ±1.175V(typ) centered at an internal common voltage. If the summing gain is 1, the output range is ±2.35V(typ). The input data format is 2's complement. The output voltage(ΔV_{AOUT}) is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal ΔV_{AOUT} is 0V for 0000H(@16bit).

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV.

The primary function of the additional analog filter is to attenuate the noise generated by the delta-sigma modulator beyond the audio passband. The AK4318 performance within the audio passband(DC~20kHz, @fs=48kHz) is constant regardless of the outband attenuation of the additional analog filter. Figure 14-1 shows the external 3rd-order LPF for the differential outputs of the AK4318. Only the 1st summing stage is necessary to achieve the specified characteristics of the AK4318 in the audio passband. However, as the outband noise moves into the audible band at low sampling rate, careful attention is required. Another example by one op-amp is shown in Figure 14-2.

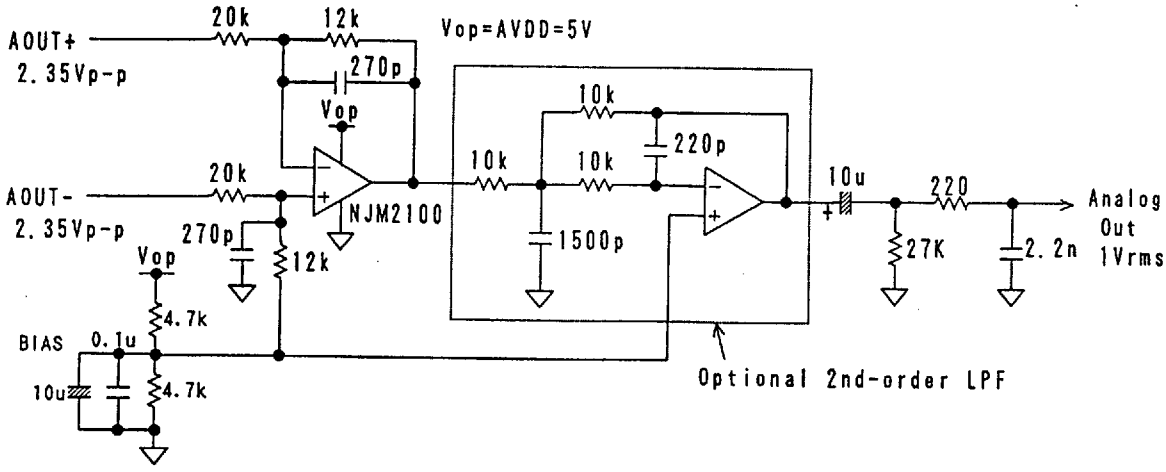


Figure 14-1. 3rd-order LPF example for the differential output

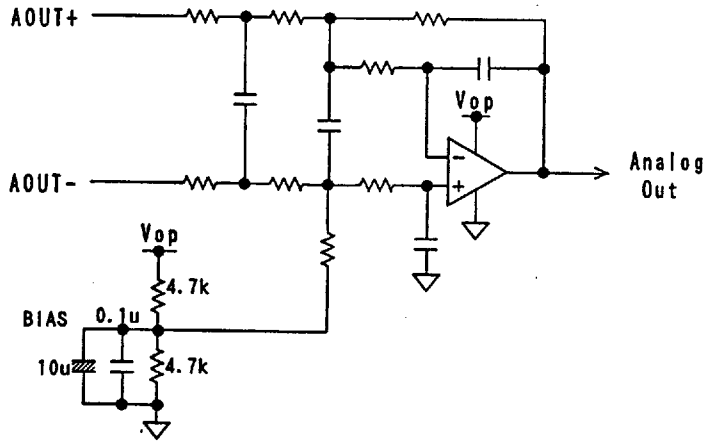


Figure 14-2. 3rd-order LPF example by one op-amp

MEASURING SYSTEM

The measuring system consists of an evaluation board[AKD4318], a digital signal source and a distortion meter[SHIBASOKU, AD725C or equivalent]. The digital signal is taken from the CD test disk or the AKD43XX which generates sine wave using ROM data.

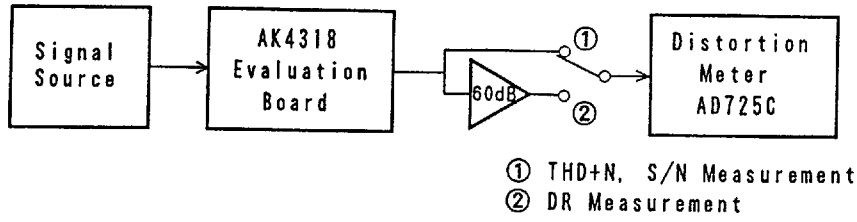


Figure 15. Measuring Block Diagram

The effects of out-of-band noise must be well taken care of when measuring THD+N, dynamic range and S/N. Table 4 shows the conditions of input signal and measurement filter used in the above measurement block. The proper use of a measurement bandlimiting filter is critical for evaluating the in-band performance of systems with low-order analog filters. The measurement bandwidth must be properly limited to prevent outband energy from influencing the measurement. The dynamic characteristics are specified at fs=48kHz. Please refer to the manual of the evaluation board about the measurement example.

parameter	Input signal	Measurement Filter (Shibasoku 725C)
THD+N	1kHz, 0dB	20kHz LPF
Dynamic Range	1kHz, -60dB	20kHz LPF, A-Weight
S/N	1kHz, 0dB/"0"data	20kHz LPF, A-Weight
Interchannel Isolation	1kHz, 0dB	20kHz LPF

Table 4. Measuring Conditions

PACKAGE

● 28pin SOP (Unit: mm)