synchro/resolver to digital converter
3-state tracking 12 bit
series 168T300

FEATURES

- **Three-state bus compatible outputs**
- **8 bit byte or 12 bit parallel addressing**
- **Industry standard low profile module**
- **Low 750 MW power consumption**
- **Broadband 47-2600 Hz, 400-2600 Hz, or 2600 Hz operation**
- **High tracking rates—to 3000 RPM**
- **K_A to 500,000 sec^{-2}**
- **TTL/CMOS compatible**
- **Inhibit does not interrupt tracking**
- **Resistive input scaling option**
- **Velocity output option**

APPLICATIONS

Coordinate Conversion—Antenna Monitoring—Fire Control Systems—Industrial Control—Robotics

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GENERAL DATA

The 168T300 is a modular, low profile, continuous tracking, Synchro/Resolver to Digital converter which employs a "type II" servo loop and contains three-state latches on the digital outputs. Outputs are addressable as either two eight bit bytes or one 12 bit word.

The 168T300 accepts broadband inputs: 47 to 2600 Hz, 360 to 2600 Hz or 2600 Hz. Output angle is natural binary code, parallel positive logic, and TTL/CMOS compatible. Synchronization to a computer is complete via a "Converter Busy" output and "Inhibit" input.

THEORY OF OPERATION

The synchro to digital converter determines the value of the input angle Θ, see block diagram, by comparing a digital feedback angle Φ with the synchro input angle. When the difference between the input angle and the feedback angle is zero, the output angle contained in the up-down counter is equal to the synchro input angle.

The Solid State Control Transformer performs the trigonometric computation:
$\sin(\Theta-\Phi) = (\sin\Theta\cos\Phi - \cos\Theta\sin\Phi)$

Note that for small angles, $\sin(\Theta-\Phi) \simeq (\Theta-\Phi)$. The equality given by the above equation is true only in the first quadrant, i.e., 0° to 90°. The analog inputs to the Solid State Control Transformer have different values, depending on, the quadrant in which the input angle lies.

$\Theta-\Phi$ is an analog representation of the error between Θ the input angle, and Φ the output angle. This analog error is first demodulated then fed to an analog integrator whose output controls the frequency of a voltage-controlled oscillator. The VCO clocks the up-down counter. The up-down counter is functionally an integrator, therefore the tracking converter in itself is a closed-loop servomechanism with two lags, making it a "type II" servo loop. The "type II" servo loop tracking converter exhibits no velocity errors and only minor acceleration errors.

Assuming that the "INHIBIT" is at a logic "1", then the digital word Φ will be strobed into the latches 1 microsecond after the up-down counter has been updated. If the three state "ENABLE" is at a logic "0", then the digital output word will be presented to the ouput pins of the module.

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ELECTRICAL SPECIFICATIONS

Parameter	Value		
Resolution	12 bits		
Accuracy (1)	±8.5 minutes		
Synchro Input Rates:	47-2600 Hz	360-2600 Hz	2600 Hz
Maximum Tracking Rate:	20 RPS	36 RPS	50 RPS
Acceleration Constant (K_a)	6000 sec^{-2}	85,000 sec^{-2}	500,000 sec^{-2}
Settling Time for 179° step	225 ms	75 ms	40 ms

Power Supplies (2)

+15VDC	30ma MAX. (25ma TYP.)
-15VDC	30ma MAX. (25ma TYP.)
+5VDC (LSTTL)	100ma MAX. (70ma TYP.)
+5VDC (CMOS)	10ma MAX. (5ma TYP.)

Digital Outputs	
Parallel Binary Angle	
CMOS	2 TTL loads
LSTTL	5 TTL loads
Converter Busy	
Loading	2 TTL loads (all models)
Pulse Width	3us (max.) positive pulse
Digital Inputs	
Inhibit	logic '0' (33KΩ pull-up resistor to +5V)
Enable (M & L)	logic '0' (33KΩ pull-up resistor to +5V)
Synchro/Resolver Input (3)	
11.8V L-L	75KΩ
90V L-L	600KΩ
Reference Input	
47-2600 Hz	10-130VRMS into 400KΩ
360-2600 Hz	10-130VRMS into 400KΩ
2600 Hz	10-130VRMS into 400KΩ
Temperature Ranges	
Operating	0°C to 70°C -55°C to 105°C (ET)
Storage	-65°C to 125°C
Dimensions	3.125" x 2.625" x .4"
Weight	3.5 oz.

NOTES

(1) Accuracy applies for:
- (a) ±10% signal amplitude variation.
- (b) 25% signal harmonic distortion.
- (c) over power supply range.
- (d) over operating temperature range.

(2) Although specified at ±15VDC all units can operate on voltages between ±12VDC to ±16.5VDC with no degradation in performance. The tolerance on the +5VDC supply is ±5%.

(3) Other signal voltages available.

ANALOG INTERFACE

INPUT SYNCHRO SIGNALS—The input synchro signals are connected to S1, S2, S3. Input resolver signals are connected to S1, S2, S3 and S4. These signals are applied to a solid-state Scott-T or a resolver isolation amplifier. Some of the outstanding features of the solid-state input are: (a) 80DB common-mode rejection, (b) common-mode voltages up to specified L-L voltage have no effect on operation, (c) any one stator and/or rotor line may be grounded, (d) high input impedance at all input levels, (e) overvoltage as high as 1000% without damage and (f) complete frequency independence.

REFERENCE INPUT—the reference input RH-RL is a true differential input with high common mode rejection. Either input can be grounded.

DIGITAL INTERFACE

There are two methods of transferring data, (1) asynchronously and (2) synchronously.

The timing sequence shown in the timing diagram assumes that the synchro input data to the converter is changing.

The asynchronous method is to detect the state of the "Busy" signal, which is high for approximately 2 microseconds while the up-down counters and latches are updating, and transfer data when it is in a low state.

The synchronous method is to use the "Inhibit" which prevents the two monostables from being triggered, and consequently the latches from updating. Data will always be valid 3 useconds after application of the "Inhibit" (i.e., taken to logic "0"). This method is valid regardless of when the "Inhibit" is applied.

The two three-state "Enable" lines can be used at any time in order to present the data in the latches to the output pins. "Enable M" enables the most significant 8 bits while "Enable L" enables the least 4 bits. A logic "0" enables while a logic "1" presents high impedance state.

Note that the operation of the internal converter loop cannot be affected in any way by the logic state present on the "Inhibit" and "Enable" pins. Either may be applied indefinitely without any impact on the converter tracking operation.

CONNECTING THE CONVERTER

The power lines, which must not be reversed, should be connected to the "+15V", "-15V" and "+5V" pins with the common connection to the ground pin "GND". The 168T300 series has adequate internal power supply bypassing which makes it unnecessary for external bypass capacitors.

The digital output is taken from Pin "1" through to "12" where Pin "1" is the MSB, which is equal to 180°.

The reference connections are made to RH and RL.

In the case of a Synchro the signals are connected to "S1", "S2" and "S3" according to the following convention:

$$E_{S1-S3} = E_{RL-RH} \sin \Theta$$
$$E_{S3-S2} = E_{RL-RH} \sin (\Theta + 120°)$$
$$E_{S2-S1} = E_{RL-RH} \sin (\Theta + 240°)$$

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For a Resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

$E_{S1-S3} = E_{RL} - E_{RH} \sin \Theta$
$E_{S2-S4} = E_{RH} - E_{RL} \cos \Theta$

The "Busy", "Inhibit" and "Enable" pins should be connected as described under the Digital Interface Heading.

RESISTIVE INPUT SCALING OPTION

On special order converters can be supplied to accommodate any range of input signal voltage by means of external resistive scaling. Consult factory for details.

VELOCITY OUTPUT OPTION

The velocity output (VEL) is a DC voltage which is proportional to the angular velocity of the synchro shaft. The voltage goes negative for an increasing digital angle and it goes positive for a decreasing digital angle. This voltage is an op amp output with an impedance of less than one ohm and with a 2ma current capability.

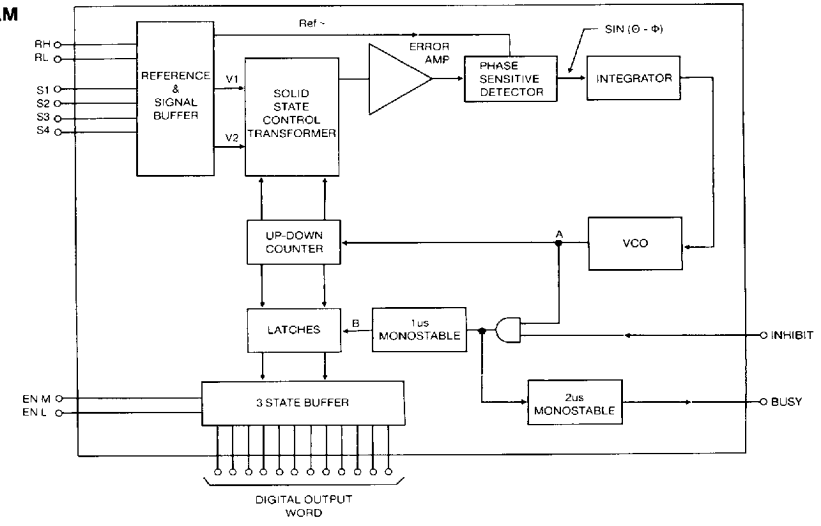
The amplitude is approximately as follows:

% of specified max. velocity	Output
100%	10.000V
80%	7.300V
60%	5.300V
40%	3.300V
20%	1.700V
10%	.850V
5%	.425V

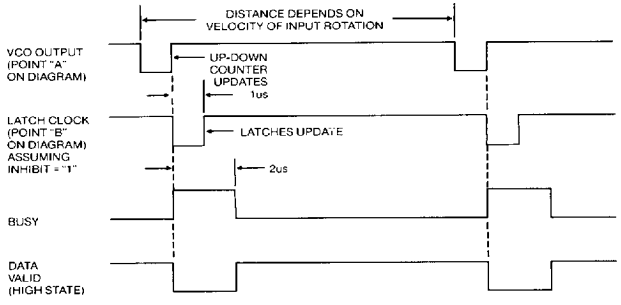
Velocity Output Characteristics

Parameter	Value
Offset	5MV max.
Linearity	
0-20%	1%
0-50%	5%
Power Supply Sensitivity	
±15V ±5%	insensitive
+5V ±5%	±5%
Ripple	
0-20 Hz	5MVRMS
Output Scaling	
Scaling Accuracy	5%
Direction Scaling	5%

BLOCK DIAGRAM 168T300



TIMING DIAGRAM



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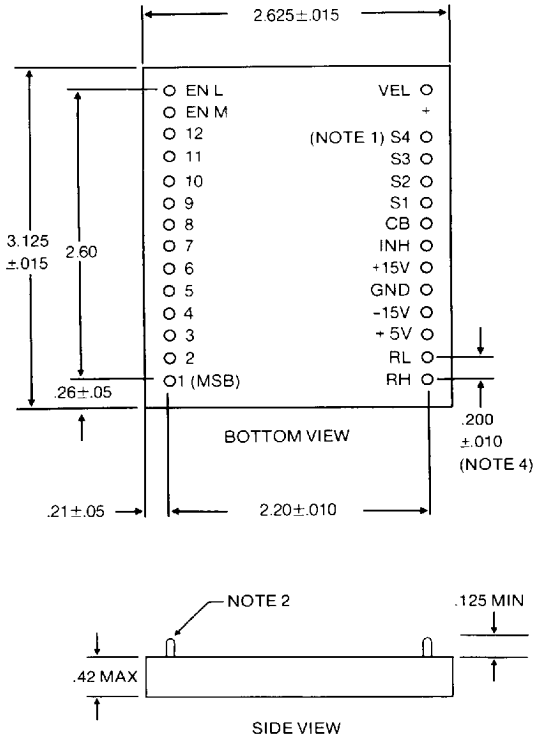
ORDERING INFORMATION

168T SUFFIX	INPUT TYPE	L-L VOLTAGE	REF. FREQ.	LOGIC TYPE
300	SYNC	11.8V	50-2600Hz	CMOS
301	SYNC	90.0V		CMOS
302	SYNC	11.8V		LSTTL
303	SYNC	90.0V		LSTTL
304	RSVR	11.8V		CMOS
305	RSVR	90.0V		CMOS
306	RSVR	11.8V		LSTTL
307	RSVR	90.0V	50-2600Hz	LSTTL
308	SYNC	11.8V	360-2600Hz	CMOS
309	SYNC	90.0V		CMOS
310	SYNC	11.8V		LSTTL
311	SYNC	90.0V		LSTTL
312	RSVR	11.8V		CMOS
313	RSVR	90.0V		CMOS
314	RSVR	11.8V		LSTTL
315	RSVR	90.0V	360-2600Hz	LSTTL
316	SYNC	11.8V	2600Hz	CMOS
317	SYNC	90.0V		CMOS
318	SYNC	11.8V		LSTTL
319	SYNC	90.0V		LSTTL
320	RSVR	11.8V		CMOS
321	RSVR	90.0V		CMOS
322	RSVR	11.8V		LSTTL
323	RSVR	90.0V	2600Hz	LSTTL

Standard temperature range (0° to 70° C), add suffix ET to part number for extended temperature range. (-55° to +105° C) add suffix V for velocity output option.

Example: Part #168T300ETV would be a synchro to digital converter with 11.8V input, 50-2600Hz frequency range, CMOS logic, and extended temperature range with velocity option.

MECHANICAL OUTLINE



NOTES

1. S4 pin appears on multiple input and resolver input models only.
2. Rigid .040 diameter pins suitable for solder-in or plug-in applications.
3. Module size includes 50 to 2600 Hz applications.
4. Non-cumulative.

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