YAMAHA LSI

YGV627

AVDP3E

Advanced Video Display processor 3 Enhanced

Preliminary

■ OUTLINE

YGV627(AVDP3E) is a VDP (Video Display Processor) that realizes higher resolution, multi-color and high speed drawing by adopting a synchronous DRAM as the video memory, while maintaining the register compatibility with YGV617 (AVDP3) that is used for controlling the high minuteness On Screen Display (OSD).

Since the device is compatible freely with display resolution ranging from NTSC to SVGA and with various screen sizes such as a wide screen, it can be used for controlling OSD for various display units. Also, it is capable of representation of varied images in accordance with the application because numerous number of colors can be selected such as the one in the range from 16 to 65536 RGB color display, or natural image display using YCbCr. In addition, the existing system can be up-graded easily thanks to the basic features from YGV617B such as a high speed drawing function, character drawing function, synchronization with external video signal, digital video input / output function, and hardware cursor display function.

■ FEATURES

[Display functions]

- Three screen configuration including bitmap screen, sprite cursor screen and external input video screen (or single color border screen)
- Monitor field and line frequencies, dot clock frequency, and display screen resolution can be specified optionally.
- Display dot clock up to 40 MHz (Example of resolution: NTSC, PAL, VGA, SVGA, NTSC wide, and VGA wide) < 627ENH [1] >
- Support with progressive scanning and interlaced scanning
- Resolution of sprite cursor screen is 32 X 32 digits. (The sprite cursor can also be used as cross-hair line cursor.)
- Smooth hardware scroll function
- Upper / lower two division display on the bitmap screen (The two sections can be scrolled independently.)
- 256 word X 16 bit CLUT is built in (The number of display colors of 32768 colors or 65536 colors can be selected in palette mode)
- Display color modes: 16 palette color mode, 256 palette color mode, 32768 RGB color mode, 65536 RGB color mode, YCbCr422(ITU601) mode < 627ENH >
- YCbCr (ITU601)-to-8 bit RGB decoder is built in. < 627ENH >
- α blending function that mixes with external input screen or single color border screen. (64 intensity levels) < 627ENH >
- Dot clock generation with built-in PLL circuit
  Generates dot clock that synchronizes with external video signal, HSYNC.
  Generates dot clock that synchronizes with external input clock (such as sub-carrier clock).

[1] < 627ENH > is a function expanded from YGV617B.

YAMAHA CORPORATION

YGV627 CATALOG
CATALOG No.: LSI-4GV627A0
2000.2

[Drawing functions]

- Commands — Block transfer by word (CPU to VRAM, VRAM to CPU, VRAM to VRAM)
  Font drawing, dot drawing and rectangular drawing.
- Drawing attribute — Sets drawing clip domain, drawing offset or drawing page, and designates bit mask, color mask, logical operation (NOT, AND, OR, EOR etc.) or direction of transfer.

[Operational clock]

- System clock (clock for drawing system) : up to 33 MHz < 627ENH >
- Dot clock (clock for display system) : up to 40 MHz < 627ENH >

[CPU interface]

- 16 bit or 8 bit asynchronous interface
- Provided with a video memory space up to 8 Mbytes and internal register space of 128 bytes < 627ENH >
- The video memory space and internal register space can be mapped indirectly with 16 byte registers.
- Wait-to-CPU generation avoidance using built-in data FIFO for memory space access and built-in data FIFO for drawing commands
- CPU interruption based on various conditions of display and drawing
- DMA transfer of drawing command data can be made when connected with external DMA controller

[Video memory interface]

- Connected memory: 4 Mbit SDRAM (128 kwords X 16 bits X 2 banks) 1 piece
  or 16 Mbit SDRAM (512 kwords X 16 bits X 2 banks) 1 piece < 627ENH >
  or 64 Mbit SDRAM (1 Mwords X 16 bits X 4 banks) 1 piece < 627ENH >
- SDRAM clock: up to 66 MHz (System clock multiplied by 2 is generated internally.) < 627ENH >
- Built-in FIFO for display data improves the drawing access efficiency and realizes high speed drawing.

[Monitor interface]

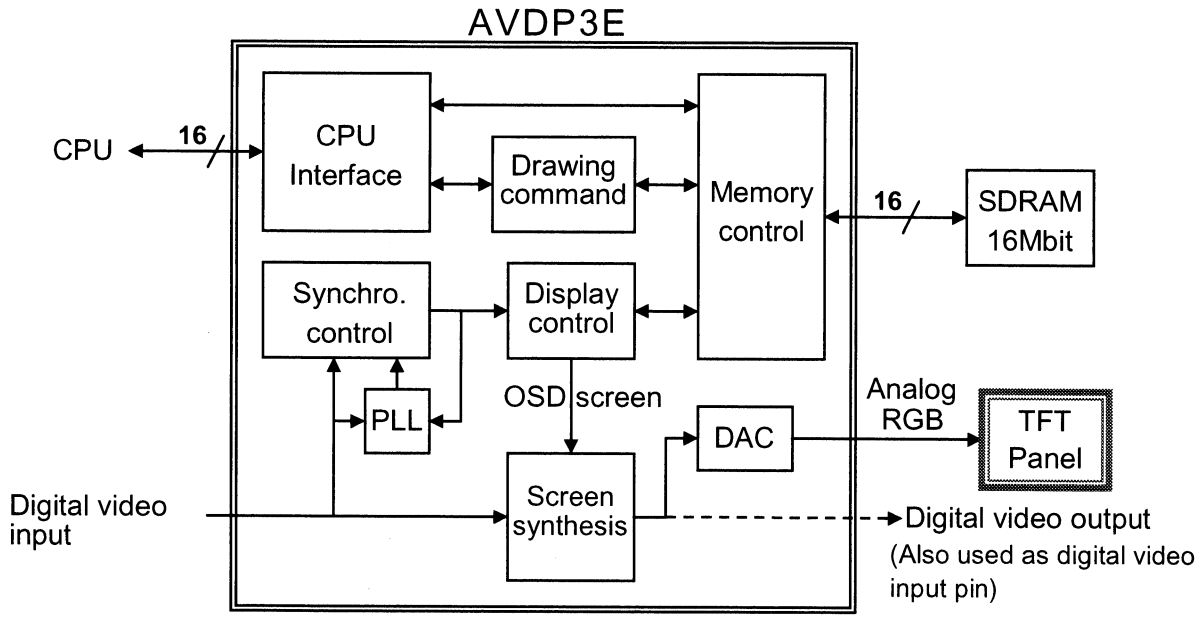
- Analog RGB output with built-in DAC (8 bits for RGB individually) < 627ENH >
- Digital video input / output (6 bits for RGB individually) < 627ENH >
- Sub-carrier clock output and dot clock output

[Others]

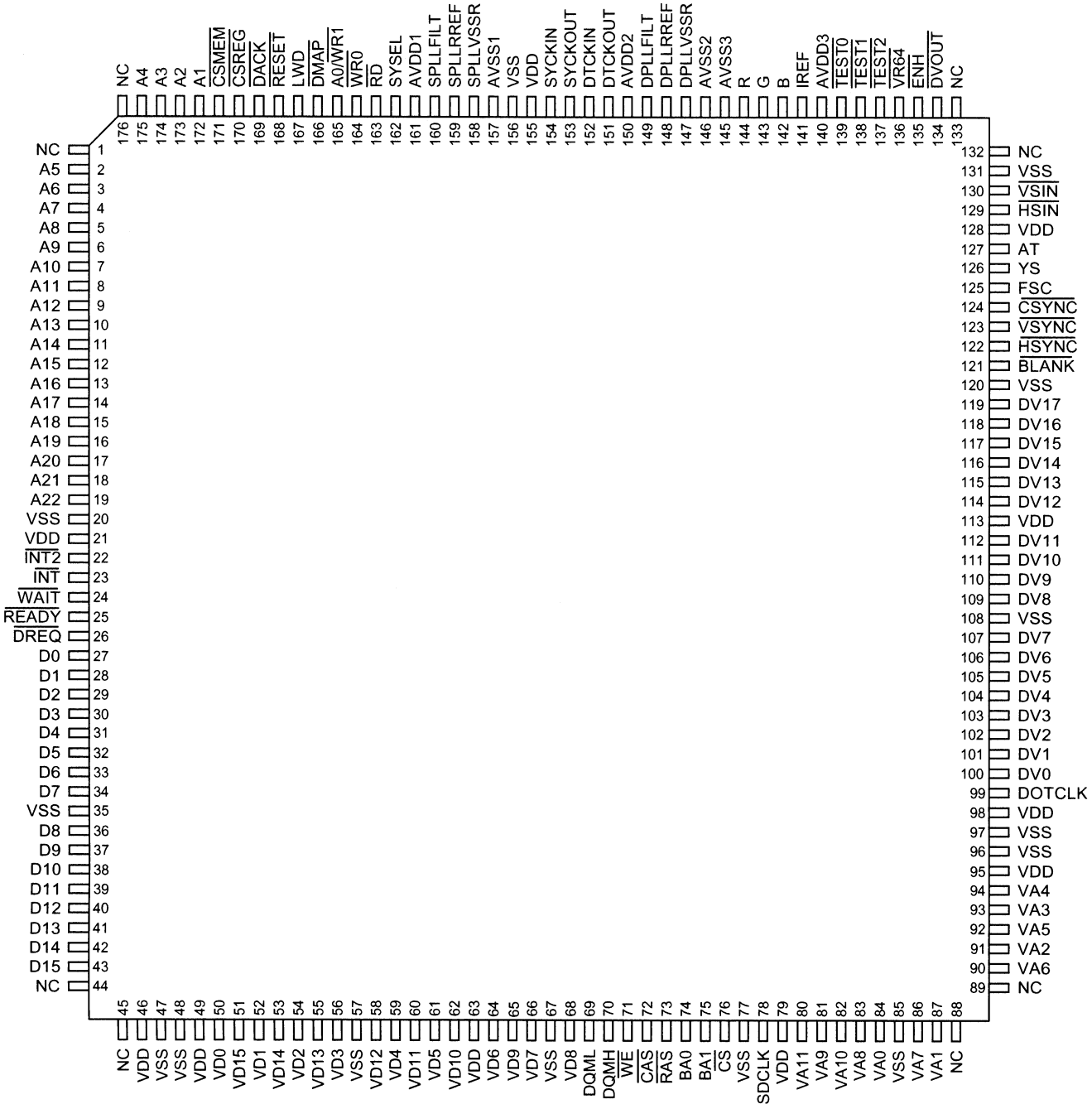
- 176LQFP
- CMOS, 3.3V single power supply
- Operating temperature range: -40 to +85 °C

< 627ENH > is a function expanded from YGV617B.

■ BLOCK DIAGRAM



■ PIN ASSIGNMENT



■ PIN FUNCTIONS

<CPU Interface>

D15 – D0 (CPU Data bus, input / output)

This is a data bus for connecting with external processor. D15 – D8 are not used when the CPU bus with 8 bit type (when low level is inputted to LWD). At this time, keep the D15 – D8 open. These pins are provided with pull-up resistors respectively.

A22 – A1 (CPU address bus, input)

This is an address bus for connecting with external processor. Input to A22 – A4 pins are ignored when high level is inputted to $\overline{\text{ENH}}$ (hereafter referred to as compatible mode) and when accessing $\overline{\text{CSREG}}$ space.
For AVDP3E, the video memory space is expanded from that of AVDP3. AVDP3E can be used as AVDP3 compatible device when A22 and A21 are fixed to low level. Be sure to input low level or high level signal into the pins that are not used.

$\overline{\text{CSREG}}$ (Register space chip select (low active), input)

The function of $\overline{\text{CSREG}}$ is the same as that of $\overline{\text{CSIO}}$ pin of AVDP3. It is chip select signal input to register space (I/O). When this chip select signal is active, the write / read pulses inputted are made valid so that the registers in the AVDP3E are accessed. In compatible mode, A22 – A4 of addresses into which this signal is inputted with low are ignored.
A22 – A8 are ignored when $\overline{\text{ENH}}$ is low level input (hereafter referred to as enhanced mode) and $\overline{\text{DMAP}}$ is low level input.

$\overline{\text{CSMEM}}$ (Memory space chip select (low active), input)

This is a chip select signal input pin for video memory port. When this chip select signal is active, the write / read pulses inputted are made valid so that the video memory managed by AVDP3E can be accessed directly. It is possible not to use $\overline{\text{CSMEM}}$ because the video memory can also be accessed from registers. In such case, it is necessary to input high level to $\overline{\text{CSMEM}}$.

A0/$\overline{\text{WR1}}$, $\overline{\text{WR0}}$ (A0/ write pulse 1, write pulse 0 (low active), input)

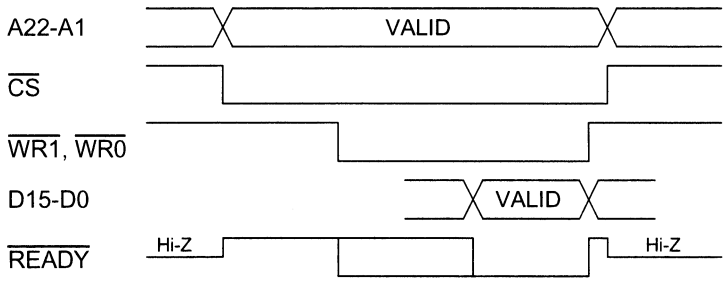
When chip select input is active, these pins control write access to AVDP3E. A0/$\overline{\text{WR1}}$ is for D15 – D8 and $\overline{\text{WR0}}$ is for D7 – D0. When the CPU bus with 8 bit type, A0/$\overline{\text{WR1}}$ functions as CPU address bit 0.

$\overline{\text{RD}}$ (Read pulse (low active), input)

When chip select input is active, $\overline{\text{RD}}$ controls read access to AVDP3E. D15 – D0 are in output state in the period while both this signal and chip select signals are active.

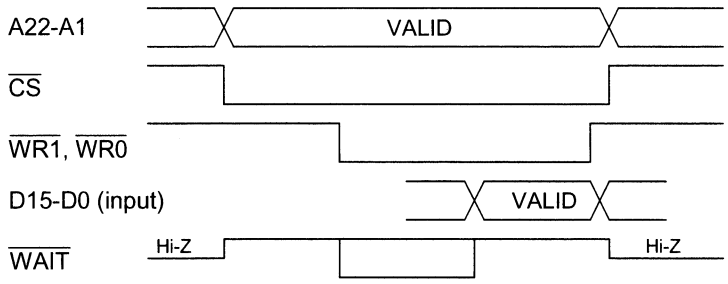
$\overline{\text{READY}}$ (Data ready (low active), 3 state output with pull up resistor)

Data ready signal output. The $\overline{\text{READY}}$ signal is made low when the internal state of AVDP3E is accessible with $\overline{\text{RD}}$ or $\overline{\text{WR1}}$, $\overline{\text{WR0}}$ input signal. $\overline{\text{READY}}$ is a 3 state output. When $\overline{\text{CSREG}}$ or $\overline{\text{CSMEM}}$ (hereafter called $\overline{\text{CS}}$ signals) is not active, it is high impedance state, and when $\overline{\text{CS}}$ signals is active and $\overline{\text{RD}}$ or $\overline{\text{WR1}}$, $\overline{\text{WR0}}$ is not active, high level is outputted from $\overline{\text{READY}}$. Some CPU must use $\overline{\text{WAIT}}$ signal instead of this signal.



$\overline{\text{WAIT}}$ (Data wait (low active), 3 state output with pull up resistor)

Data wait signal output. When $\overline{\text{CS}}$ signals is active, $\overline{\text{WAIT}}$ signal is made low once with respect to $\overline{\text{RD}}$ or $\overline{\text{WR1}}$, $\overline{\text{WR0}}$ in accordance with the internal state of AVDP3E and is made high when it becomes accessible. $\overline{\text{WAIT}}$ is a 3 state output. When $\overline{\text{CS}}$ signals is not active, it is in high impedance state, and when $\overline{\text{CS}}$ signals is active and $\overline{\text{RD}}$ or $\overline{\text{WR1}}$, $\overline{\text{WR0}}$ is not active, high level is outputted from $\overline{\text{WAIT}}$. Some CPU must use $\overline{\text{READY}}$ signal instead of this signal.



$\overline{\text{INT}}$ (Interrupt (low active), open drain output)

Interrupt request signal output. This signal is made low when the internal state of AVDP3E coincides with the setting conditions of registers. This signal is reset with access to AVDP3E's internal register.

$\overline{\text{INT2}}$ (High speed bus interface (low active), output)

This is an interrupt request signal output, and its output logical value is the same as that of $\overline{\text{INT}}$. For high speed CPU bus, this output signal is used to avoid the influence of transit time caused by the pull-up resistor when the interrupt signal is negated. Use $\overline{\text{INT}}$ or $\overline{\text{INT2}}$ in accordance with the requirement of the system into which the AVDP3E is built in.

LWD (CPU data bus width selection, input)

This is used to select width of CPU data bus. When this signal is high level input, the device is compatible with 16 bit system and when low level input, the device is compatible with 8 bit system respectively. Since LWD is used for selection of a mode, always fix it to either level.

$\overline{\text{RESET}}$ (Reset (low active), input)

Initial reset signal is inputted to $\overline{\text{RESET}}$. The reset signal input resets the internal state of the device and the internal registers are cleared to "0". (Some registers are loaded with initial value.) Be sure to input the reset signal after power up. $\overline{\text{RESET}}$ has a pull-up resistor.

$\overline{\text{DREQ}}$ (DMA request (low active), output)
$\overline{\text{DREQ}}$ outputs command data request signal to external DMA controller.

$\overline{\text{DACK}}$ (DMA acknowledge (low active), input)
Command data transfer permission signal is inputted to $\overline{\text{DACK}}$ in response to $\overline{\text{DREQ}}$ signal from external DMA controller. $\overline{\text{DACK}}$ has a pull-up resistor.

$\overline{\text{DMAP}}$ (Register mapping selection (low active), input)
$\overline{\text{DMAP}}$ is used to select a register space mapping method. When high level is inputted, 16 byte indirect mapping is selected. When low level is inputted, all the registers except CLUT are mapped directly in the 128 byte space. The input to $\overline{\text{DMAP}}$ determines the valid address when $\overline{\text{CSREG}}$ signal is active. $\overline{\text{DMAP}}$ input signal is valid regardless of the state of $\overline{\text{ENH}}$ input signal. Input high level to $\overline{\text{DMAP}}$ to make this device compatible with AVDP3.
Since $\overline{\text{DMAP}}$ is for selection of a mode, always fix it to either level. $\overline{\text{DMAP}}$ has a pull-up resistor.

$\overline{\text{ENH}}$ (Enhanced mode (low active), input)
This signal permits enhanced functions for AVDP3. When high level is inputted, only the registers that are compatible with AVDP3 are made valid, and the function of the expansion registers are fixed to their default values. However, the register can be set. When low level is inputted, the function of the expansion register is made valid. The state of signal inputted to $\overline{\text{ENH}}$ determines the timing of access to SDRAM in addition to selection of function of the expansion register. In compatible mode, the timing of access to SDRAM is equal to that of the performance of AVDP3, but in enhanced mode, the access performance is doubled. Since $\overline{\text{ENH}}$ is for selection of a mode, always fix it to either level. $\overline{\text{ENH}}$ has a pull-up resistor.

<Video Memory Interface>

BA1 – BA0, VA11 – VA0 (SDRAM address, output)

These pins output address for SDRAM that is used as a video memory controlled by AVDP3E. They output row address and column address on time sharing basis. BA1 and 0 output bank address. However, when $\overline{VR64}$ is a high level input (16M SDRAM is connected), VA11 becomes bank select. When a read command or write command is sent to the SDRAM, VA10 functions as auto-precharge enable. Since these pins are always driven by AVDP3E, VRAM bus hold function of AVDP3 cannot be used.

VD15 – VD0 (SDRAM data, input / output)

These pins constitute a data bus for SDRAM that is used as video memory controlled by ADVP3E. These pins have a pull-up resistor individually. VRAM bus hold function of AVDP3 cannot be used.

$\overline{RAS}$ (Row address strobe (low active), output)

$\overline{RAS}$ outputs row address strobe signal for SDRAM that is used as a video memory controlled by AVDP3E. Since $\overline{RAS}$ is always driven by AVDP3E, VRAM bus hold function of AVDP3 cannot be used.

$\overline{CAS}$ (Column address strobe (low active), output)

$\overline{CAS}$ outputs column address strobe signal for SDRAM that is used as a video memory controlled by AVDP3E. Since $\overline{CAS}$ is always driven by AVDP3E, VRAM bus hold function of AVDP3 cannot be used.

$\overline{WE}$ (Write enable (low active), output)

$\overline{WE}$ outputs write strobe signal for SDRAM that is used as a video memory controlled by AVDP3E. Since $\overline{WE}$ is always driven by AVDP3E, VRAM bus hold function of AVDP3 cannot be used.

DQMH, DQML (Data bus mask, output)

These pins output data mask signal for SDRAM that is used as a video memory controlled by AVDP3E.
DQMH is for VD15 – VD8, and DQML is for VD7 – VD0.

$\overline{CS}$ (SDRAM chip select (low active), output)

This pin outputs chip select signal for SDRAM that is used as a video memory controlled by AVDP3E.
AVDP3E requires connection to SDRAM because the device uses $\overline{CS}$ control for access to SDRAM for power saving purpose and against switching noise.

SDCLK (SDRAM clock, output)

This pin outputs clock for SDRAM that is used as a video memory controlled by AVDP3E. Every output signal connected to SDRAM is outputted synchronizing with the rising edge of this clock. The read data from SDRAM is latched in the AVDP3E at the rising edge of this clock. The clock enable pin of SDRAM should always be used in enable state.

$\overline{VR64}$ (SDRAM capacity selection, input)

High level is inputted when the capacity of SDRAM that is used as a video memory controlled by AVDP3E is 16 Mbits, or low level is inputted when the capacity is 64 Mbits. This signal determines the function of signal outputted from BA1, BA0, and VA11 – VA0 pins. Since this pin is for selection of a mode, always fix it to either level. $\overline{VR64}$ has a pull-up resistor.

✶ $\overline{VR64}$="H" (When 16 Mbit SDRAM is connected)

Pin name of AVDP3E	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA1	BA0	VA11	VA10	VA9	VA8	VA7-0
Pin name of SDRAM	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	-	-	A11	A10	A9	A8	A7-0

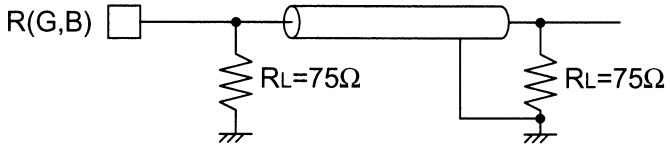
✶ $\overline{VR64}$="L" (When 64 Mbit SDRAM is connected)

Pin name of AVDP3E	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA1	BA0	VA11	VA10	VA9	VA8	VA7-0
Pin name of SDRAM	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A13	A12	A11	A10	A9	A8	A7-0

<Monitor interface>

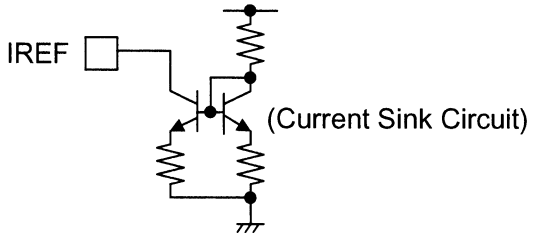
R, G, B (Linear RGB, analog output)

These pins output linear RGB signal. When a termination resistor of 37.5 Ω is connected, about 1 Vp-p with resolution of 8 bits (256 levels) signal is outputted. These pins can directly drive a monitor whose impedance is 75 Ω as shown below.



IREF (RGB DAC reference current, analog input)

Reference current for RGB DAC is inputted to this pin. The reference current of -8.88 mA provides amplitude of 0.76 Vp-p (typical value). When supplying the reference current, use a current sink circuit as shown below.



$\overline{\text{CSYNC}}$ (Composite sync (low active), output)

This pin outputs a composite sync signal to external monitor. In interlace mode, it outputs equivalent pulse.

$\overline{\text{VSYNC}}$ (Vertical sync signal (low active), output)

This pin outputs vertical sync signal to external monitor.

$\overline{\text{HSYNC}}$ (Horizontal sync signal (low active), output)

This pin outputs horizontal sync signal to external monitor.

$\overline{\text{BLANK}}$ (Valid display period, output)

This pin outputs low active signal that indicates non-display period (blank period). Therefore, it can be used as high active signal that indicates valid display period for LCD panel.

FSC (Sub-carrier clock, output)

This pin outputs sub-carrier clock for video encoder. This pin can output a clock inputted to DCKIN pin divided by 1, 2, 4 or 8 which may be selected in accordance with the register setting. Inputting a clock of 14.318 MHz into DCKIN pin provides sub-carrier clock of 3.5795 MHz when divided by 4.

$\overline{\text{DVOUT}}$ (External video data input/output control, input)

When internal register EXIO(R#05) is "0", this pin specifies input/output of the external video data pins (DV17-0). The external video data pins become input pins when high level is inputted to $\overline{\text{DVOUT}}$, or becomes output pins when low level is inputted to $\overline{\text{DVOUT}}$. When specifying the input/output of the external video data pins with EXIO(R#05), input high level to $\overline{\text{DVOUT}}$ or keep it open. $\overline{\text{DVOUT}}$ has a pull up resistor.

DV17 – DV0 (External video data, input/output)

These are input / output pins for digital external video data. Specification of input or output of these pins is controlled with $\overline{\text{DVOUT}}$ pin and internal register (R#05:EXIO).

For the external video data, a format with 6 bits for digital RGB individually, or a format with 6 bits for CbYCr individually can be selected. The format of the input / output data is as shown below. These pins have a pull-up resistor.

DV17 16 15 14 13 12	11 10 9 8 7 6	5 4 3 2 1 0
R (Cr) 5-0 (I/O)	G (Y) 5-0 (I/O)	B (Cb) 5-0 (I/O)

YS (Superimpose timing, output)

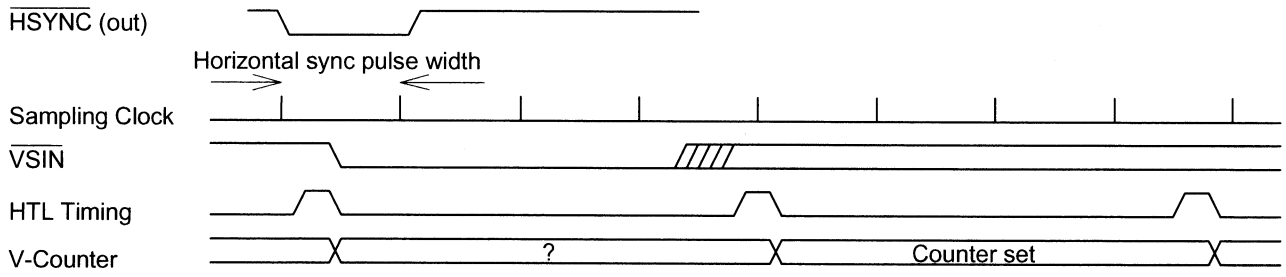
When performing superimpose, this pin outputs a signal that controls switching with external signal. When displaying bitmap plane, this pin outputs inversion signal for YSN bits that can be set by dot. In the border displaying period or blank period, this pin outputs inversion signal of border YS data.

AT (Display dot attribute, output)

This pin outputs 1 bit attribute data that can be set by display dot. When ATE signal of internal register is set to "0", the value set in the ATD bit of register is outputted without regarding to the display data. When "1" is set for ATE signal, B0 (LSB of Blue) that is inputted to DAC for blue is outputted from AT pin. At this time, the same data of MSB is inputted to LSB of DAC for blue. During the blank period, B0 of border is outputted when ATE signal is set to "1". When the signal is set to "1", the value set to ATD bit is outputted. This signal can be used, for example, for specifying semi-transparency (YM) when externally mixing display data.

$\overline{\text{VSIN}}$ (Vertical timing reset (low active), input)

This signal resets the vertical timing of CRT controller block of AVDP3E (This function is the same as $\overline{\text{VRESET}}$ pin of AVDP3). When this input signal is sampled with period equal to the pulse width of horizontal sync signal, and low level is detected three times consecutively, the internal counter is set at the first HTL timing (horizontal sync signal start timing) immediately after the moment. In interlace mode, field identification is performed at the resetting of vertical timing by inputting composite sync signal of external video through this pin. This feature allows the superimposition synchronizing with frame period easily. If this signal is inputted during the display period, the display data of the next field is not guaranteed. Since $\overline{\text{VSIN}}$ has a built-in pull-up resistor, it can be kept open when this function is not used.



$\overline{\text{HSIN}}$ (Horizontal timing reset (low active), input)

This signal resets the horizontal timing of CRT controller block of AVDP3E (This function is the same as $\overline{\text{HRESET}}$ pin of AVDP3). The horizontal timing is set to the horizontal sync starting position at the moment this signal falls from high level to low level, and at the same time, the phase of dot clock is reset. If this signal is inputted during the display period, the display data of the next line is not guaranteed. When the built-in PLL is used, the input signal of this pin and output of $\overline{\text{HSYNC}}$ pin are locked. Since $\overline{\text{HSIN}}$ has a built-in pull-up resistor, it can be kept open when this function is not used.

DOTCLK (Dot clock, output)

Output signal of display data (analog R, G, B, DV17 – DV0, YS, AT) is outputted synchronizing with DOTCLK.

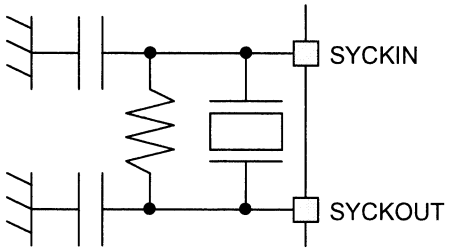
<Clock>

SYCKIN, SYCKOUT (XTAL input / output, input / output)

Crystal is connected to these pins to generate system clock. This clock is supplied to CPU interface and individual blocks of the drawing processor. The built-in PLL produces SDRAM clock based on this clock. When supplying system clock and dot clock using the same clock through SYSEL pin (when low level is inputted to SYSEL), input the common clock through DTCKIN pin. At this time, input low level or high level signal into SYCKIN pin. SYCKOUT pin can be kept open.

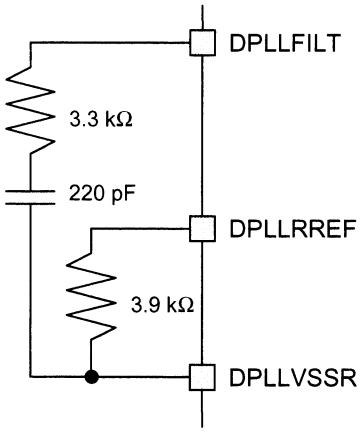
When inputting externally generated clock, input it into SYCKIN pin.

SYCKIN and SYCKOUT pins are the same as VCKIN and VCKOUT pins of AVDP3.



SPLLVSSR, SPLLRREF, SPLLFILT (SDRAM clock PLL pins, analog)

These pins are used to connect external resistors and capacitors for the built-in PLL that produces SDRAM clock.



Notes:

1. Arrange the components so that the parasitic capacitance among SPLLFILT, SPLLRREF and SPLLVSSR is minimized and the signals do not cross each other.
2. PLL may not lock if there is a time difference between the rising moment of AVDD (for PLL) and the rising moment of VDD (for Digital Logic).

SYSEL (SYCK signal select, input)

This signal selects the source of system clock. When low level is inputted to SYSEL, the system clock and dot clock use the same source of the clock. In this case, the common clock is inputted into DTCKIN. Therefore, there is no need to input clock into SYCKIN. When high level is inputted to SYSEL, the system clock is supplied from the source of SYCKIN input clock independent from the dot clock.

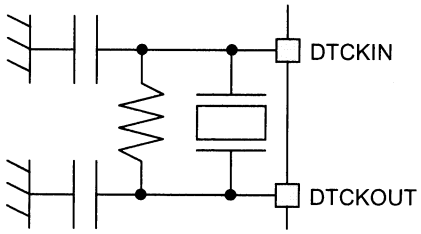
When SYSEL is used with low input, be sure to input stable clock into DCKIN even if the clock produced by the built-in PLL is used as the dot clock. Since SYSEL is used for selection of a mode, always fix it to either level. SYSEL has a pull-up resistor. SYSEL is the same as VCKS pin of AVDP3.

DTCKIN, DTCKOUT (XTAL input / output, input / output)

Crystal is connected to these pins to input dot clock. When operating the built-in PLL in FSC sync mode, the reference clock is inputted to these pins. At this time, the clock with multiple of fsc is to be inputted. When PLL function is not used, this input clock is supplied directly to the CRTC block and display data control block. When low level is inputted to SYSEL, it is also supplied to blocks including VRAM interface, CPU interface and drawing processor.

When inputted externally generated clock, input it into DTCKIN.

DTCKIN and DTCKOUT are the same as DCKIN and DCKOUT of AVDP3.



DPLLVSSR, DPLLRREF, DPLLFILT (Dot clock PLL pin, analog)

These pins are used to connect external resistors and capacitors for the built-in PLL that produces dot clock. When directly using DTCKIN input signal as dot clock without using the built-in PLL, keep DPLLFILT open and short-circuit between DPLLRREF and DPLLVSSR. The notes on the configuration of external circuit and layout of the components for SPLLFILT, SPLLRREF, SPLLVSSR also apply to these pins.

<Other pins>

$\overline{\text{TEST2}}$ - $\overline{\text{TEST0}}$ (Test, input)

These pins are used for testing internal circuit of AVDP3E. Be sure to keep them open (without connecting any component) when using the device.

AVDD1, AVSS1 (SDRAM clock generation VCO analog power supply)

These pins supply power to VCO analog circuit that generates SDRAM clock. Connect +3.3 V to AVDD1 and ground level to AVSS1.

AVDD2, AVSS2 (Dot clock generation VCO analog power supply)

These pins supply power to VCO analog circuit that generates dot clock. Connect +3.3 V to AVDD2 and ground level to AVSS2.

AVDD3, AVSS3 (DAC analog power supply)

These pins supply power to analog circuit of RGB DAC section. Connect +3.3 V to AVDD3 and ground level to AVSS3.

VDD, VSS (Digital power supply)

These pins supply power to digital circuit of AVDP3E. Connect +3.3 V to VDD and ground level to VSS. AVDP3E has several VDD and VSS, all of which require power supply. Connect a bypass capacitor between VDD and VSS as a noise killer as close as possible to the pins.

■ ELECTRICAL CHARACTERISTICS

Note!
The values of electrical characteristics shown in this section are target data, and do not guarantee the specifications at the shipment of this product. The specification data may be changed without prior notice. Therefore, please confirm the newest data when using this product.

● Absolute maximum ratings

Items	Symbol	Ratings	Unit
Supply Voltage	V_{DD} *1	-0.5 – +4.6	V
Input terminal voltage (DTCKIN,SYCKIN,VD15-0)	V_I *1	-0.5 – V_{DD}+0.5	V
Input terminal voltage (Other than above pins)	V_I *1	-0.5 – 5.5	V
Output terminal voltage	V_O *1	-0.5 – V_{DD}+0.5	V
Output terminal current	I_O	-20 – +20	mA
Storage temperature	Tstg	-50 – +125	°C

*1 Value with respect to Vss(GND)=0V

● Recommended operating conditions

Items	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD} *1	3.0	3.3	3.6	V
Low level input voltage (VD15-0)	V_{IL} *1	-0.3		0.8	V
High level input voltage (VD15-0)	V_{IH} *1	2.2		V_{DD} +0.3	V
Low level input voltage (DTCKIN,SYCKIN)	V_{IL} *1	-0.3		V_{DD} x0.3	V
High level input voltage (DTCKIN,SYCKIN)	V_{IH} *1	V_{DD} x0.7		V_{DD} +0.3	V
Low level input voltage ($\overline{\text{RESET}}$)	V_{IL} *1	-0.3		0.8	V
High level input voltage ($\overline{\text{RESET}}$)	V_{IH} *1	2.4		5.3	V
Low level input voltage (Other than above pins)	V_{IL} *1	-0.3		0.8	V
High level input voltage (Other than above pins)	V_{IH} *1	2.2		5.3	V
Ambient operating temperature	T_{OP}	-40		85	°C

*1 Value with respect to Vss(GND)=0V

● Electrical characteristics under recommended operating conditions

• DC characteristics

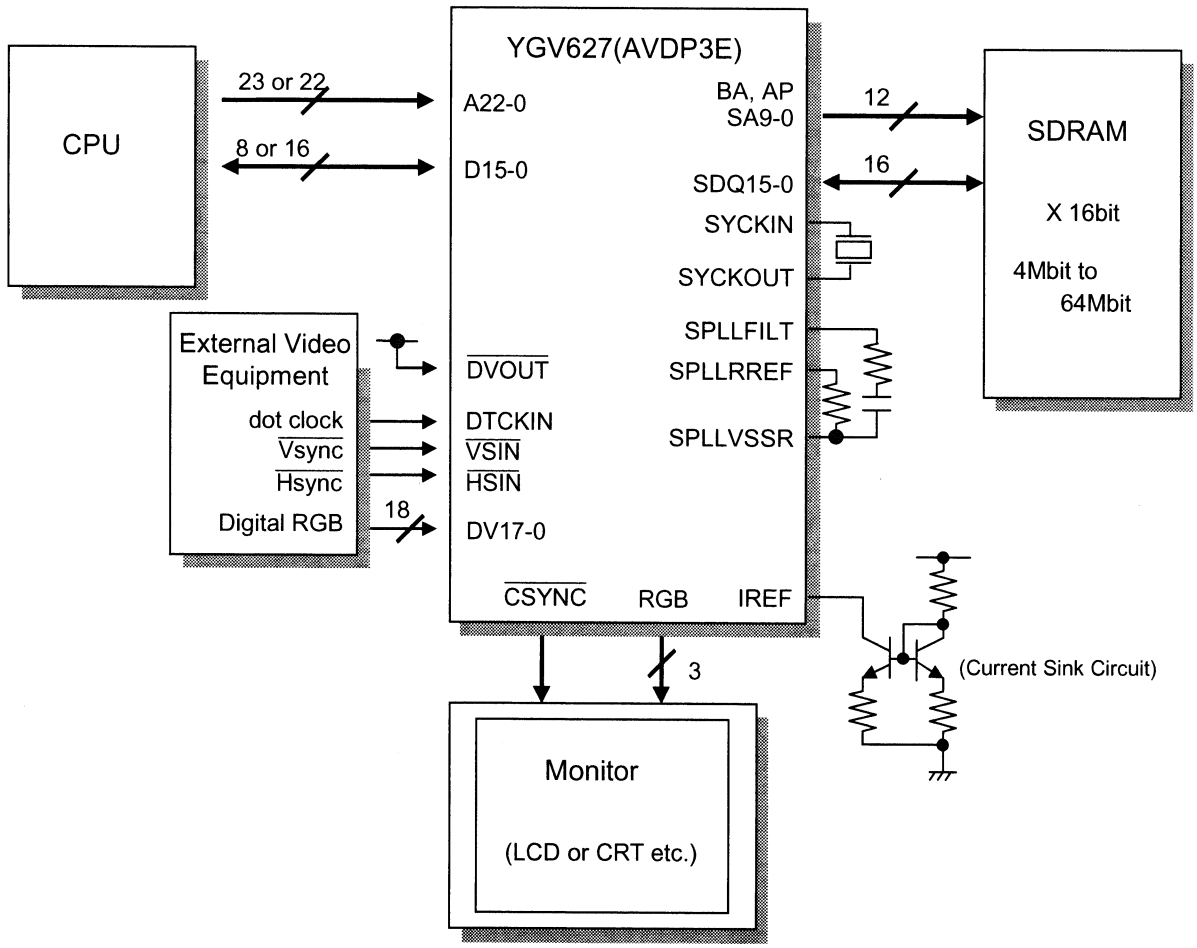
Items	Symbol	Min.	Typ.	Max.	Unit
Low level output voltage	V_{OL} *1			0.4	V
High level output voltage *2	V_{OH} *3	2.4			V
Input leakage current	I_{LI}			10	µA
Output leakage current	I_{LO}			25	µA
Power consumption	I_{DD}*4*5				mA

*1 Measurement condition I_{OL}=1.6mA (Value with respect to Vss(GND)=0V)
*2 Except Open Drain terminal
*3 Measurement condition I_{OH}= -1.0mA (Value with respect to Vss(GND)=0V)
*4 Typical value means average value obtained when a general image is displayed.
*5 Maximum value means instantaneous maximum value obtained when the internal circuit is fully operated.

• Terminal capacity

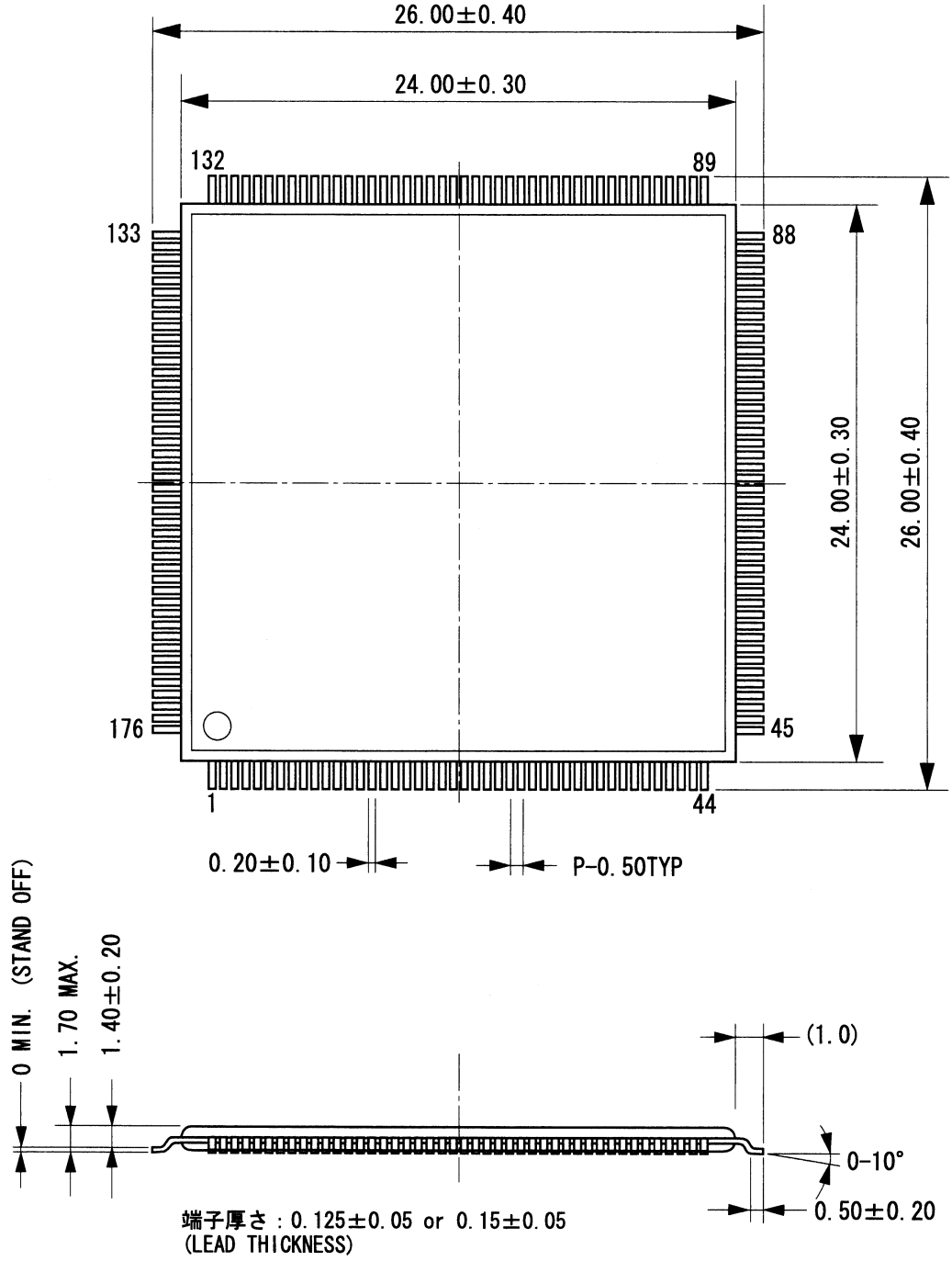
Items	Symbol	Min.	Typ.	Max.	Unit
Input terminal capacity	C_I			8	pF
Output terminal capacity	C_O			10	
Input / Output terminal capacity	C_{IO}			12	

■ Example of System Configuration



■ External Dimensions of Package

C-PK176VP-1



モールドコーナー形状は、この図面と若干異なるタイプのものもあります。
カッコ内の寸法値は参考値とする。
モールド外形寸法はバリを含まない。
単位(UNIT)：mm(millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.
The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

注） 表面実装LSIは保管条件及び、半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせ下さい。

Note: The LSIs for surface mount need special consideration on storage and soldering conditions.
For detailed information, Please contact your nearest Yamaha agent.

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