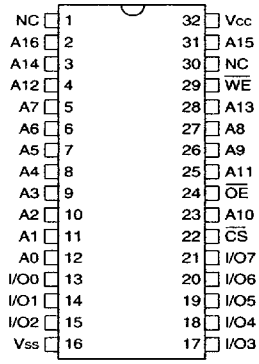
128Kx8 SRAM MODULE

FIG. 1

PIN CONFIGURATION
TOP VIEW



PIN DESCRIPTION

A_{0-16}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground

FEATURES

- Access Times 25, 35, 45ns
- Standard Microcircuit Drawing, 5962-93156
- MIL-STD-883 Compliant Devices Available
- Rad Tolerant Devices Available
- JEDEC Standard 32 pin, Hermetic Ceramic DIP (Package 300)
- Commercial, Industrial and Military Temperature Ranges
- Organized as 128K x 8
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Battery Back-Up Operation

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	Vcc + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	40	pF
Output capicitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	40	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	-25		-35		-45		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10		10		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		110		110		70	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz		30		30		25	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		2.4		2.4		V

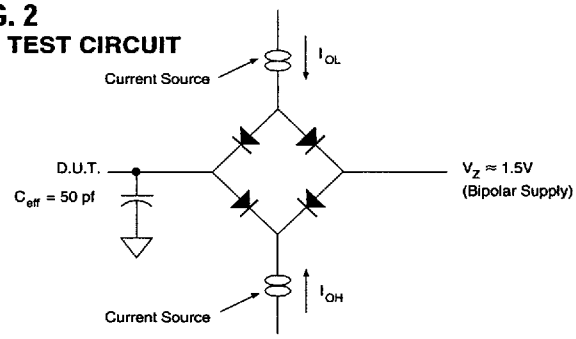
NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-25			-35			-45			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V_{DR}	$\overline{CS}$ ≥ V_{CC} -0.2V	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		.10	3.5		.10	3.5		.10	3.5	mA
	I_{CCDR2}	V_{CC} = 2V		.05	2.0		.05	2.0		.05	2.0	mA

FIG. 2
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_O = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

SRAM MODULES

AC CHARACTERISTICS

(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Parameter Read Cycle	Symbol	-25		-35		-45		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	25		35		45		ns
Address Access Time	tAA		25		35		45	ns
Output Hold from Address Change	tOH	5		5		5		ns
Chip Select Access Time	tACS		25		35		45	ns
Output Enable to Output Valid	tOE		20		25		35	ns
Chip Select to Output in Low Z	tCLZ[1]	5		5		5		ns
Output Enable to Output in Low Z	tOLZ[1]	5		5		5		ns
Chip Disable to Output in High Z	tCHZ[1]		15		20		30	ns
Output Disable to Output in High Z	tOHZ[1]		15		20		25	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS

(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Parameter Write Cycle	Symbol	-25		-35		-45		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	25		35		45		ns
Chip Select to End of Write	tCW	20		25		30		ns
Address Valid to End of Write	tAW	20		25		30		ns
Data Valid to End of Write	tDW	15		20		25		ns
Write Pulse Width	tWP	20		25		30		ns
Address Setup Time	tAS	0		0		0		ns
Address Hold Time	tAH	0		0		0		ns
Output Active from End of Write	tOW[1]	5		5		5		ns
Write Enable to Output in High Z	tWHZ[1]	0	15	0	20	0	25	ns
Data Hold Time	tDH	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 3
TIMING WAVEFORM - READ CYCLE

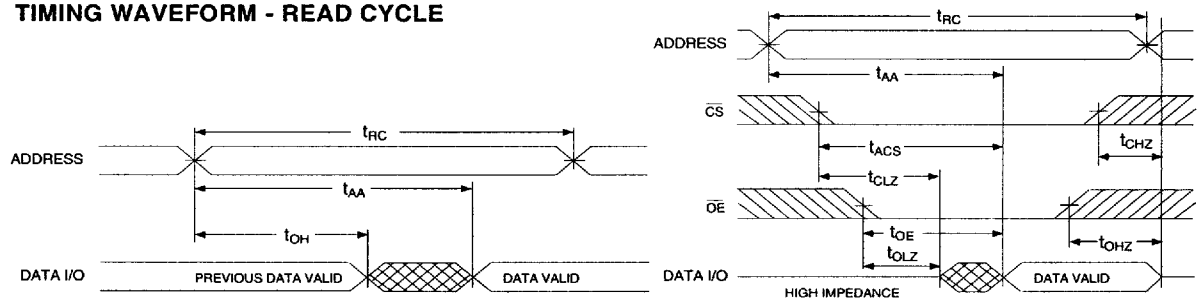


FIG. 4
WRITE CYCLE - $\overline{WE}$ CONTROLLED

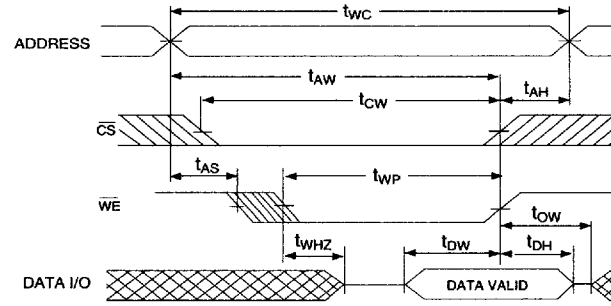
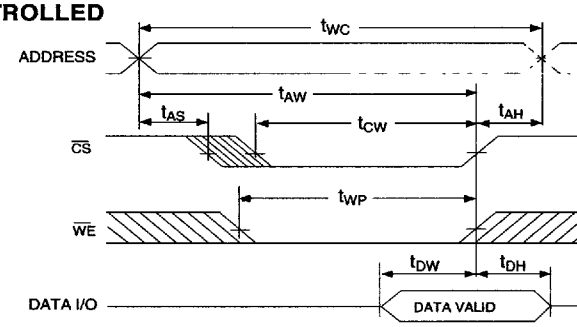
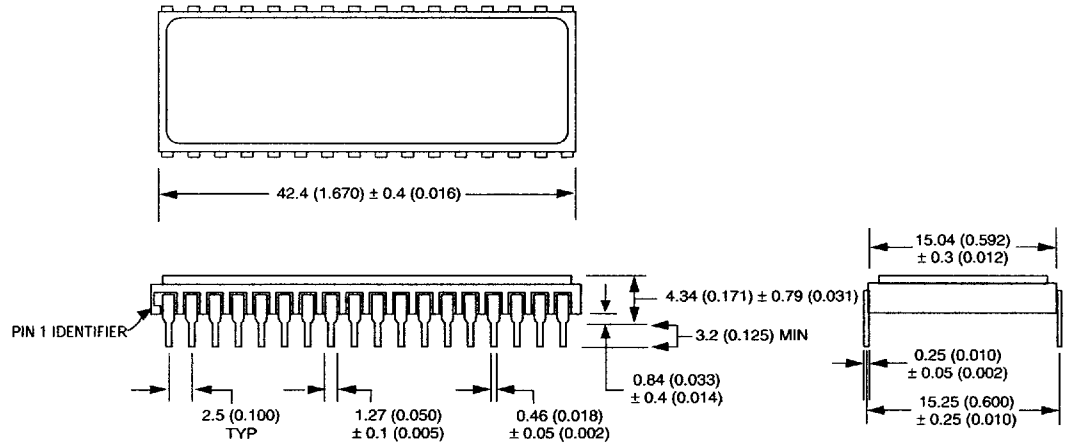


FIG. 5
WRITE CYCLE - $\overline{CS}$ CONTROLLED



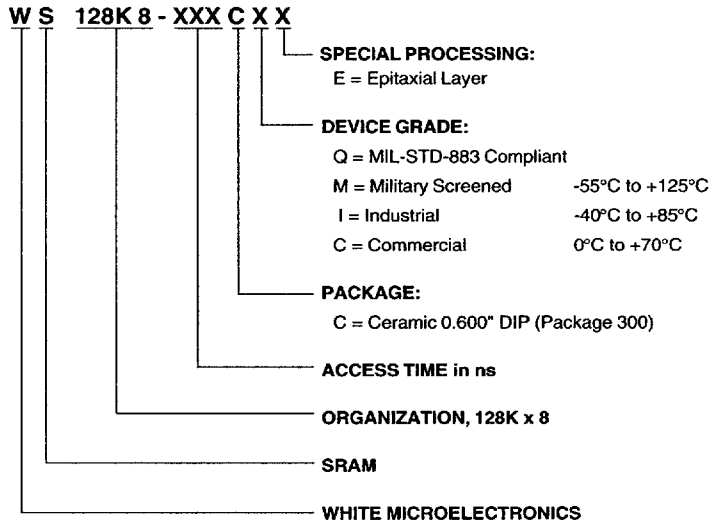
SRAM MODULES

PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 8 SRAM	45ns	32 pin DIP	5962-93156 06HXX
128K x 8 SRAM	35ns	32 pin DIP	5962-93156 07HXX
128K x 8 SRAM	25ns	32 pin DIP	5962-93156 08HXX