Fast Infrared Transceiver Module (FIR, 4 Mbit/s) for 2.4 V to 5.5 V Operation

FEATURES

- Supply voltage 2.4 V to 5.5 V, operating idle current (receive mode) < 3.3 mA, shutdown current < 1 µA over full temperature range
- Surface mount package, top and side view, 9.7 mm x 4.7 mm x 4 mm
- Operating temperature - 25 °C to 85 °C
- Transmitter wavelength typ. 886 nm, supporting IrDA and remote control
- IrDA compliant, link distance > 1 m, ± 15°, window losses are allowed to still be inside the IrDA spec.
- Remote control range > 8 m, typ. 22 m
- ESD > 1 kV
- Latchup > 100 mA
- EMI immunity > 550 V/m for GSM frequency and other mobile telephone bands/(700 MHz to 2000 MHz, no external shield)
- Split power supply, LED can be driven by a separate power supply not loading the regulated supply. U.S. pat. no. 6,157,476
- Tri-state-receiver output, floating in shut down with a weak pull-up
- Eye safety class 1 (IEC 60825-1, ed. 2001), limited LED on-time, LED current is controlled, no single fault to be considered
- Qualified for lead (Pb)-free and Sn/Pb processing (MSL4)
- Compliant to RoHS directive 2002/95/EC and in accordance to WEEE 2002/96/EC

DESCRIPTION

The TFDU6103 is a low-power infrared transceiver module compliant to the latest IrDA® physical layer standard for fast infrared data communication, supporting IrDA speeds up to 4 Mbit/s (FIR), and carrier based remote control modes up to 2 MHz. Integrated within the transceiver module are a PIN photodiode, an infrared emitter (IRED), and a low-power CMOS control IC to provide a total front-end solution in a single package.

Vishay FIR transceivers are available in different package options, including this BabyFace package (TFDU6103). This wide selection provides flexibility for a variety of applications and space constraints. The transceivers are capable of directly interfacing with a wide variety of I/O devices which perform the modulation/demodulation function, including National Semiconductor's PC87338, PC87108 and PC87109, SMC's FDC37C669, FDC37N769 and CAM35C44, and Hitachi's SH3. TFDU6103 has a tri-state output and is floating in shut-down mode with a weak pull-up.

APPLICATIONS

- Notebook computers, desktop PCs, palmtop computers (Win CE, Palm PC), PDAs
- Digital still and video cameras
- Printers, fax machines, photocopiers, screen projectors
- Telecommunication products (cellular phones, pagers)
- Internet TV boxes, video conferencing systems
- External infrared adapters (dongles)
- Medical an industrial data collection

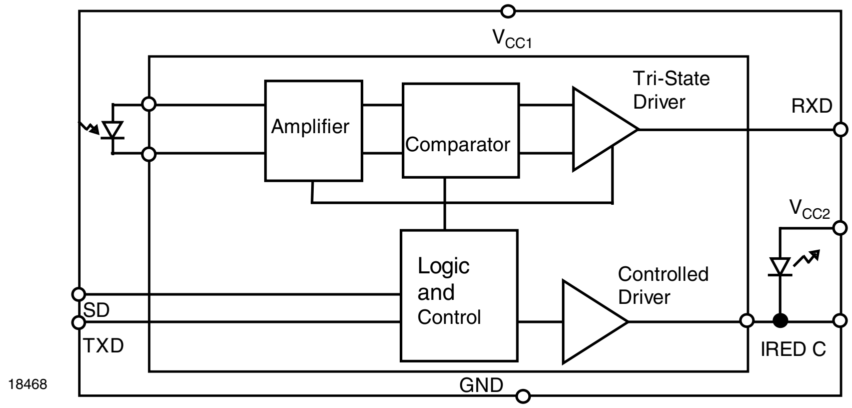
PRODUCT SUMMARY

PART NUMBER	DATA RATE (kbit/s)	DIMENSIONS H x L x W (mm x mm x mm)	LINK DISTANCE (m)	OPERATING VOLTAGE (V)	IDLE SUPPLY CURRENT (mA)
TFDU6103	4000	4 x 9.7 x 4.7	0 to ≥ 1	2.4 to 5.5	2

PARTS TABLE

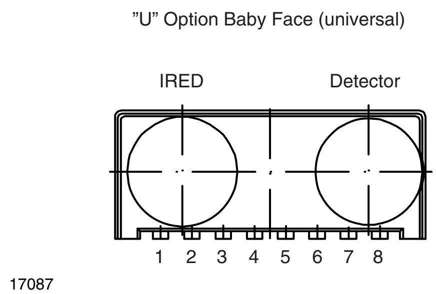
PART	DESCRIPTION	QTY/REEL
TFDU6103-TR3	Oriented in carrier tape for side view surface mounting	1000 pcs
TFDU6103-TT3	Oriented in carrier tape for top view surface mounting	1000 pcs

FUNCTIONAL BLOCK DIAGRAM



PINOUT

TFDU6103
weight 0.2 g



Definitions:

In the Vishay transceiver datasheets the following nomenclature is used for defining the IrDA operating modes:
SIR: 2.4 kbit/s to 115.2 kbit/s, equivalent to the basic serial infrared standard with the physical layer version IrPhy 1.0
MIR: 576 kbit/s to 1152 kbit/s
FIR: 4 Mbit/s
VFIR: 16 Mbit/s
MIR and FIR were implemented with IrPhy 1.1, followed by IrPhy 1.2, adding the SIR low power standard. IrPhy 1.3 extended the low power option to MIR and FIR and VFIR was added with IrPhy 1.4. A new version of the standard in any case obsoletes the former version.

Note

We apologize to use sometimes in our documentation the abbreviation LED and the word light emitting diode instead of infrared emitting diode (IRED) for IR-emitters. That is by definition wrong; we are here following just a bad trend.
Typical values are for design aid only, not guaranteed nor subject to production testing and may vary with time.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	DESCRIPTION	I/O	ACTIVE
1	V_{CC2} IRED anode	Connect IRED anode directly to V_{CC2}. For voltages higher than 3.6 V an external resistor might be necessary for reducing the internal power dissipation. An unregulated separate power supply can be used at this pin		
2	IRED cathode	IRED cathode, internally connected to driver transistor		
3	TXD	This input is used to transmit serial data when SD is low. An on-chip protection circuit disables the LED driver if the TXD pin is asserted for longer than 100 µs. When used in conjunction with the SD pin, this pin is also used to set receiver speed mode	I	High
4	RXD	Received data output, push-pull CMOS driver output capable of driving a standard CMOS or TTL load. No external pull-up or pull-down resistor is required. **Floating with a weak pull-up of 500 kΩ (typ.) in shutdown mode**	O	Low
5	SD	Shutdown, also used for dynamic mode switching. Setting this pin active places the module into shutdown mode. On the falling edge of this signal, the state of the TXD pin is sampled and used to set receiver low bandwidth (TXD = low, SIR) or high bandwidth (TXD = high, MIR and FIR) mode	I	High
6	V_{CC1}	Supply voltage		
7	NC			
8	GND	Ground		

ABSOLUTE MAXIMUM RATINGS

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage range, transceiver	0 V < V_{CC2} < 6 V	V_{CC1}	- 0.5		+ 6	V
Supply voltage range, transmitter	0 V < V_{CC1} < 6 V	V_{CC2}	- 0.5		+ 6.5	V
Input currents	For all pins, except IRED anode pin				10	mA
Output sinking current					25	mA
Power dissipation	See derating curve, figure 6	P_D			500	mW
Junction temperature		T_J			125	°C
Ambient temperature range (operating)		T_{amb}	- 25		+ 85	°C
Storage temperature range		T_{stg}	- 25		+ 85	°C
Soldering temperature	See recommended solder profile (see figure 4)				260	°C
Average output current		I_{IRED} (DC)			125	mA
Repetitive pulse output current	< 90 µs, t_{on} < 20 %	I_{IRED} (RP)			600	mA
IRED anode voltage		V_{IREDA}	- 0.5		+ 6.5	V
Voltage at all inputs and outputs	V_{IN} > V_{CC1} is allowed	V_{IN}			5.5	V

Note

Reference point ground pin 8, unless otherwise noted.
Typical values are for design aid only, not guaranteed nor subject to production testing and may vary with time.

EYE SAFETY INFORMATION

STANDARD	CLASSIFICATION
IEC/EN 60825-1 (2007-03), DIN EN 60825-1 (2008-05) “SAFETY OF LASER PRODUCTS - Part 1: equipment classification and requirements”, simplified method	Class 1
IEC 62471 (2006), CIE S009 (2002) “Photobiological Safety of Lamps and Lamp Systems”	Exempt
DIRECTIVE 2006/25/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 5th April 2006 on the minimum health and safety requirements regarding the exposure of workers to risks arising from physical agents (artificial optical radiation) (19th individual directive within the meaning of article 16(1) of directive 89/391/EEC)	Exempt

Note

Vishay transceivers operating inside the absolute maximum ratings are classified as eye safe according the above table.

ELECTRICAL CHARACTERISTICS (1)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
TRANSCEIVER						
Supply voltage		V_{CC}	2.4		5.5	V
Dynamic supply current	Receive mode only, idle In transmit mode, add additional 85 mA (typ.) for IRED current. Add RXD output current depending on RXD load.					
	SIR mode	I_{CC}		1.8	3	mA
	MIR/FIR mode	I_{CC}		2	3.3	mA
Shutdown supply current	SD = high T = 25 °C, not ambient light sensitive, detector is disabled in shutdown mode	I_{SD}		0.01		µA
	SD = high, full specified temperature range, not ambient light sensitive	I_{SD}			1	µA
Operating temperature range		T_A	- 25		+ 85	°C
Input voltage low (TXD, SD)		V_{IL}	- 0.5		0.5	V

ELECTRICAL CHARACTERISTICS (1)						
PARAMETER	**TEST CONDITIONS**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
TRANSCEIVER						
Input voltage high (TXD, SD)	CMOS level (2)	V_{IH}	V_{CC} - 0.3		6	V
Input leakage current (TXD, SD)	V_{IN} = 0.9 x V_{CC1}	I_{ICH}	- 1		+ 1	µA
Input capacitance, TXD, SD		C_I			5	pF
Output voltage low	I_{OL} = 500 µA, C_{load} = 15 pF	V_{OL}			0.4	V
Output voltage high	I_{OH} = 250 µA, C_{load} = 15 pF	V_{OH}	0.9 x V_{CC1}			V
Output RXD current limitation high state low state	Short to ground Short to V_{CC1}				20 20	mA mA
SD shutdown pulse duration	Activating shutdown		30		∞	µs
RXD to V_{CC1} impedance		R_{RXD}	400	500	600	kΩ
SD mode programming pulse duration	All modes	t_{SDPW}	200			ns

Note

(1) T_{amb} = 25 °C, V_{CC1} = V_{CC2} = 2.4 V to 5.5 V unless otherwise noted.
Typical values are for design aid only, not guaranteed nor subject to production testing.

(2) The typical threshold level is 0.5 x V_{CC1} (V_{CC1} = 3 V). It is recommended to use the specified min./max. values to avoid increased operating current.

OPTOELECTRONIC CHARACTERISTICS (1)						
PARAMETER	**TEST CONDITIONS**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
RECEIVER						
Minimum irradiance E_e in angular range (3) SIR mode	9.6 kbit/s to 115.2 kbit/s λ = 850 nm to 900 nm	E_e		25 (2.5)	35 (3.5)	mW/m² (µW/cm²)
Minimum irradiance E_e in angular range, MIR mode	1.152 Mbit/s λ = 850 nm to 900 nm	E_e		65 (6.5)		mW/m² (µW/cm²)
Minimum irradiance E_e inangular range, FIR mode	4 Mbit/s λ = 850 nm to 900 nm	E_e		80 (8)	90 (9)	mW/m² (µW/cm²)
Maximum irradiance E_e in angular range (4)	λ = 850 nm to 900 nm	E_e		5 (500)		kW/m² (mW/cm²)
Maximum no detection irradiance	(2)	E_e	4 (0.4)			mW/m² (µW/cm²)
Rise time of output signal	10 % to 90 %, 15 pF	$t_{r\ (RXD)}$	10		40	ns
Fall time of output signal	90 % to 10 %, 15 pF	$t_{f\ (RXD)}$	10		40	ns
RXD pulse width of output signal, 50 %, SIR mode	Input pulse length, 1.4 µs < P_{Wopt} < 25 µs	t_{PW}		2.1		µs
	Input pulse length, 1.4 µs < P_{Wopt} < 25 µs, - 25 °C < T < 85 °C (5)	t_{PW}	1.5	1.8	2.6	µs
RXD pulse width of output signal, 50 %, MIR mode	Input pulse length, P_{Wopt} = 217 ns, 1.152 Mbit/s	t_{PW}	110	250	270	ns
RXD pulse width of output signal, 50 %, FIR mode	Input pulse length, P_{Wopt} = 125 ns, 4 Mbit/s	t_{PW}	100		140	ns
	Input pulse length, P_{Wopt} = 250 ns, 4 Mbit/s	t_{PW}	225		275	ns
Stochastic jitter, leading edge	Input irradiance = 100 mW/m², 4 Mbit/s				20	ns
	Input irradiance = 100 mW/m², 1.152 Mbit/s				40	ns
	Input irradiance = 100 mW/m², 576 kbit/s				80	ns
	Input irradiance = 100 mW/m², ≤ 115.2 kbit/s				350	ns
Receiver start up time	After completion of shutdown programming sequence power on delay				250	µs
Latency		t_L		40	100	µs

OPTOELECTRONIC CHARACTERISTICS (1)						
PARAMETER	**TEST CONDITIONS**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
TRANSMITTER						
IRED operating current, switched current limiter	Note: no external current limiting resistor is needed for $V_{CC1} = V_{CC2}$ = 3.3 V	I_D	330	440	600	mA
Output pulse width limitation	Input pulse width t < 20 µs	t_{pw}		t		µs
	Input pulse width 20 µs < t < 150 µs	t_{pw}	18		150	µs
	Input pulse width t ≥ 150 µs	t_{pw_lim}			150	µs
Output leakage IRED current		I_{IRED}	- 1		1	µA
Output radiant intensity, see figure 1, recommended application circuit	$V_{CC} = V_{IRED}$ = 3.3 V, α = 0° TXD = high, SD = low, R1 = 1 Ω	I_e	110	170	468 (6)	mW/sr
Output radiant intensity, see figure 1, recommended application circuit	$V_{CC} = V_{IRED}$ = 3.3 V, α = 0°, 15° TXD = high, SD = low, R1 = 1 Ω	I_e	100	130	468 (6)	mW/sr
Output radiant intensity	V_{CC1} = 3.3 V, α = 0°, 15° TXD = low or SD = high (receiver is inactive as long as SD = high)	I_e			0.04	mW/sr
Output radiant intensity, angle of half intensity		α		± 24		deg
Peak - emission wavelength (7)		λ_p	875	886	900	nm
Spectral bandwidth		Δλ		45		nm
Optical rise time, Optical fall time		t_{ropt}, t_{fopt}	10		40	ns
Optical output pulse duration	Input pulse width 217 ns, 1.152 Mbit/s	t_{opt}	207	217	227	ns
	Input pulse width 125 ns, 4 Mbit/s	t_{opt}	117	125	133	ns
	Input pulse width 250 ns, 4 Mbit/s	t_{opt}	242	250	258	ns
Optical overshoot					25	%

Notes

(1) T_{amb} = 25 °C, V_{CC} = 2.4 V to 5.5 V unless otherwise noted. All timing data measured with 4 Mbit/s are measured using the IrDA FIR transmission header. The data given here are valid 5 µs after starting the preamble.
Typical values are for design aid only, not guaranteed nor subject to production testing.

(2) This parameter reflects the backlight test of the IrDA physical layer specification to guarantee immunity against light from fluorescent lamps.

(3) IrDA sensitivity definition: minimum irradiance E_e in angular range, power per unit area. The receiver must meet the BER specification while the source is operating at the minimum intensity in angular range into the minimum half-angular range at the maximum link length.

(4) Maximum irradiance E_e in angular range, power per unit area. The optical delivered to the detector by a source operating at the maximum intensity in angular range at minimum link length must not cause receiver overdrive distortion and possible related link errors. If placed at the active output interface reference plane of the transmitter, the receiver must meet its bit error ratio (BER) specification. For more definitions see the document “Symbols and Terminology” on the Vishay website

(5) Retriggering once during applied optical pulse may occur.

(6) Maximum value is given by eye safety class 1, IEC 60825-1, simplified method.

(7) Due to this wavelength restriction compared to the IrDA spec of 850 nm to 900 nm the transmitter is able to operate as source for the standard remote control applications with codes as e.g. Philips RC5/RC6® or RECS 80. When operated under IrDA full range conditions (125 mW/sr) the RC range to be covered is in the range from 8 m to 12 m, provided that state of the art remote control receivers are used.

RECOMMENDED CIRCUIT DIAGRAM

Vishay Semiconductors transceivers integrate a sensitive receiver and a built-in power driver. The combination of both needs a careful circuit board layout. The use of thin, long, resistive and inductive wiring should be avoided. The inputs (TXD, SD) and the output RXD should be directly (DC) coupled to the I/O circuit.

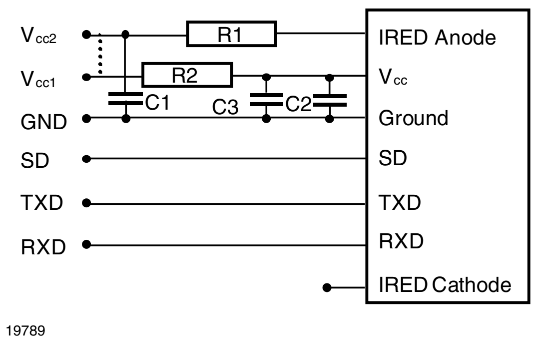


Fig. 1 - Recommended Application Circuit

The capacitor C1 is buffering the supply voltage and reduces the influence of the inductance of the power supply line. This one should be a Tantalum or other fast capacitor to guarantee the fast rise time of the IRED current. The resistor R1 is only necessary for higher operating voltages and elevated temperatures, see derating curve in figure 6, to avoid too high internal power dissipation.

The capacitors C2 and C3 combined with the resistor R2 (as the low pass filter) is smoothing the supply voltage V_{CC1}. R2, C1, C2, and C3 are optional and dependent on the quality of the supply voltages V_{CC1} and V_{CC2} and injected noise. An unstable power supply with dropping voltage during transmission may reduce sensitivity (and transmission range) of the transceiver. The placement of these parts is critical. It is strongly recommended to position C2 and C3 as close as possible to the transceiver power supply pins. An tantalum capacitor should be used for C1 and C3 while a ceramic capacitor is used for C2.

In addition, when connecting the described circuit to the power supply, low impedance wiring should be used.

When extended wiring is used the inductance of the power supply can cause dynamically a voltage drop at V_{CC2}. Often some power supplies are not able to follow the fast current rise time. In that case another 4.7 µF (type, see table under C1) at V_{CC2} will be helpful.

Keep in mind that basic RF-design rules for circuit design should be taken into account. Especially longer signal lines should not be used without termination. See e.g. “The Art of Electronics” Paul Horowitz, Wienfield Hill, 1989, Cambridge University Press, ISBN: 0521370957.

TABLE 1 - RECOMMENDED APPLICATION CIRCUIT COMPONENTS

COMPONENT	RECOMMENDED VALUE	VISHAY PART NUMBER
C1, C3	4.7 µF, 16 V	293D 475X9 016B
C2	0.1 µF, ceramic	VJ 1206 Y 104 J XXMT
R1	**3.3 V supply voltage:** no resistors necessary, the internal controller is able to control the current	e.g. 2 x CRCW-1206-1R0-F-RT1
R2	10 Ω, 0.125 W	CRCW-1206-10R0-F-RT1

I/O AND SOFTWARE

In the description, already different I/Os are mentioned. Different combinations are tested and the function verified with the special drivers available from the I/O suppliers. In special cases refer to the I/O manual, the Vishay application notes, or contact directly Vishay Sales, Marketing or Application.

MODE SWITCHING

The TFDU6103 is in the SIR mode after power on as a default mode, therefore the FIR data transfer rate has to be set by a programming sequence using the TXD and SD inputs as described below. The low frequency mode covers speeds up to 115.2 kbit/s. Signals with higher data rates should be detected in the high frequency mode. Lower frequency data can also be received in the high frequency mode but with reduced sensitivity.

To switch the transceivers from low frequency mode to the high frequency mode and vice versa, the programming sequences described below are required.

SETTING TO THE HIGH BANDWIDTH MODE (0.576 Mbit/s to 4 Mbit/s)

1. Set SD input to logic “high”.
2. Set TXD input to logic “high”. Wait $t_s \geq 200$ ns.
3. Set SD to logic “low” (this negative edge latches state of TXD, which determines speed setting).
4. After waiting $t_h \geq 200$ ns TXD can be set to logic “low”. The hold time of TXD is limited by the maximum allowed pulse length.

After that TXD is enabled as normal TXD input and the transceiver is set for the high bandwidth (576 kbit/s to 4 Mbit/s) mode.

SETTING TO THE LOWER BANDWIDTH MODE (2.4 kbit/s to 115.2 kbit/s)

1. Set SD input to logic "high".
2. Set TXD input to logic "low". Wait $t_s \geq 200$ ns.
3. Set SD to logic "low" (this negative edge latches state of TXD, which determines speed setting).
4. TXD must be held for $t_h \geq 200$ ns.

After that TXD is enabled as normal TXD input and the transceiver is set for the lower bandwidth (9.6 kbit/s to 115.2 kbit/s) mode.

Note

When applying this sequence to the device already in the lower bandwidth mode, the SD pulse is interpreted as shutdown. In this case the RXD output of the transceiver may react with a single pulse (going active low) for a duration less than 2 µs. The operating software should take care for this condition.
In case the applied SD pulse is longer than 4 µs, no RXD pulse is to be expected but the receiver startup time is to be taken into account before the device is in receive condition.

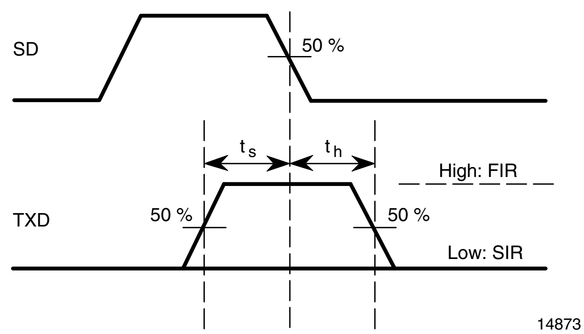


Fig. 2 - Mode Switching Timing Diagram

TABLE 2 - TRUTH TABLE

INPUTS			OUTPUTS	
SD	**TXD**	**OPTICAL INPUT IRRADIANCE mW/m²**	**RXD**	**TRANSMITTER**
High	x	x	Weakly pulled (500 kΩ) to V_{CC1}	0
Low	High	x	Low (active)	I_e
	High > 150 µs	x	High	0
	Low	< 4	High	0
	Low	> min. irradiance E_e < max. irradiance E_e	Low (active)	0
	Low	> max. irradiance E_e	x	0

RECOMMENDED SOLDER PROFILES

Solder Profile for Sn/Pb Soldering

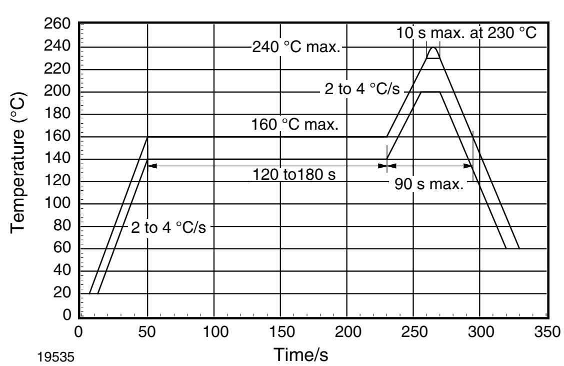


Fig. 3 - Recommended Solder Profile for Sn/Pb soldering

Lead (Pb)-free, Recommended Solder Profile

The TFDU6103 is a lead (Pb)-free transceiver and qualified for lead (Pb)-free processing. For lead (Pb)-free solder paste like Sn $_{(3.0 - 4.0)}$ Ag $_{(0.5 - 0.9)}$ Cu, there are two standard reflow profiles: Ramp-Soak-Spike (RSS) and Ramp-To-Spike (RTS). The Ramp-Soak-Spike profile was developed primarily for reflow ovens heated by infrared radiation. With widespread use of forced convection reflow ovens the Ramp-To-Spike profile is used increasingly. Shown in figure 4 and 5 are Vishay's recommended profiles for use with the TFDU6103 transceivers. For more details please refer to the application note "SMD Assembly Instructions".
A ramp-up rate less than 0.9 °C/s is not recommended. Ramp-up rates faster than 1.3 °C/s could damage an optical part because the thermal conductivity is less than compared to a standard IC.

Wave Soldering

For TFDUxxxx and TFBSxxxx transceiver devices wave soldering is not recommended.

Manual Soldering

Manual soldering is the standard method for lab use. However, for a production process it cannot be recommended because the risk of damage is highly dependent on the experience of the operator. Nevertheless, we added a chapter to the above mentioned application note, describing manual soldering and desoldering.

Storage

The storage and drying processes for all Vishay transceivers (TFDUxxxx and TFBSxxx) are equivalent to MSL4. The data for the drying procedure is given on labels on the packing and also in the application note “Taping, Labeling, Storage and Packing”.

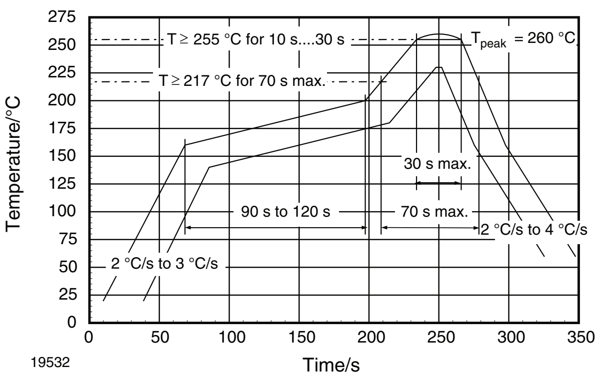


Fig. 4 - Solder Profile, RSS Recommendation

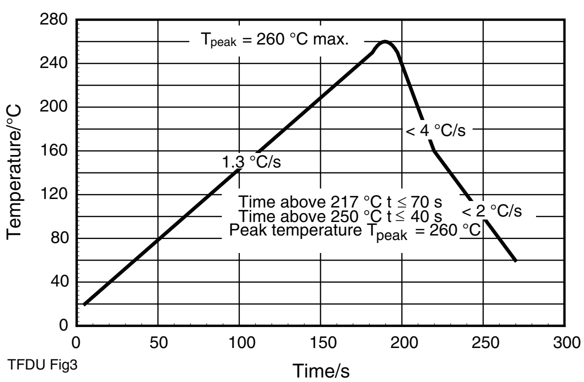


Fig. 5 - RTS Recommendation

CURRENT DERATING DIAGRAM

Figure 6 shows the maximum operating temperature when the device is operated without external current limiting resistor. A power dissipating resistor of 2 Ω is recommended from the cathode of the IRED to ground for supply voltages above 4 V. In that case the device can be operated up to 85 °C, too.

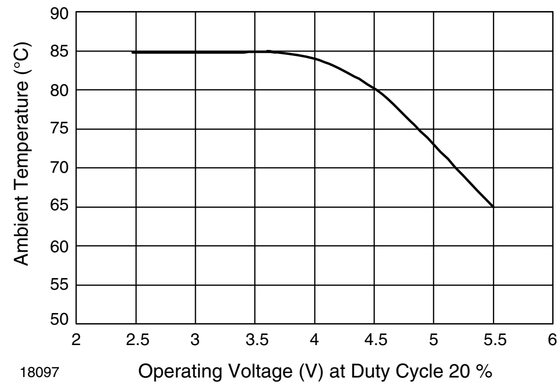


Fig. 6 - Temperature Derating Diagram

PACKAGE DIMENSIONS in millimeters

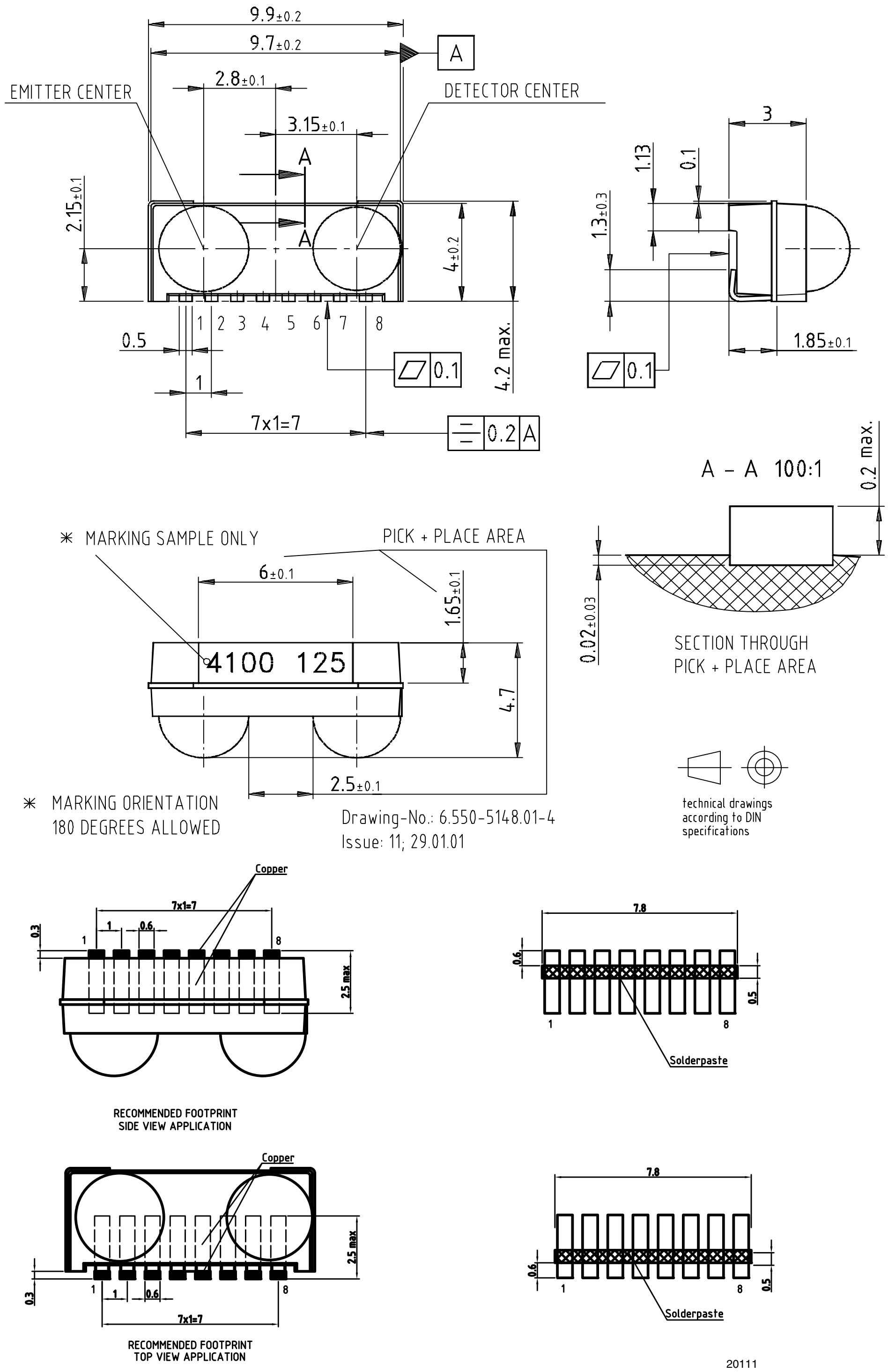
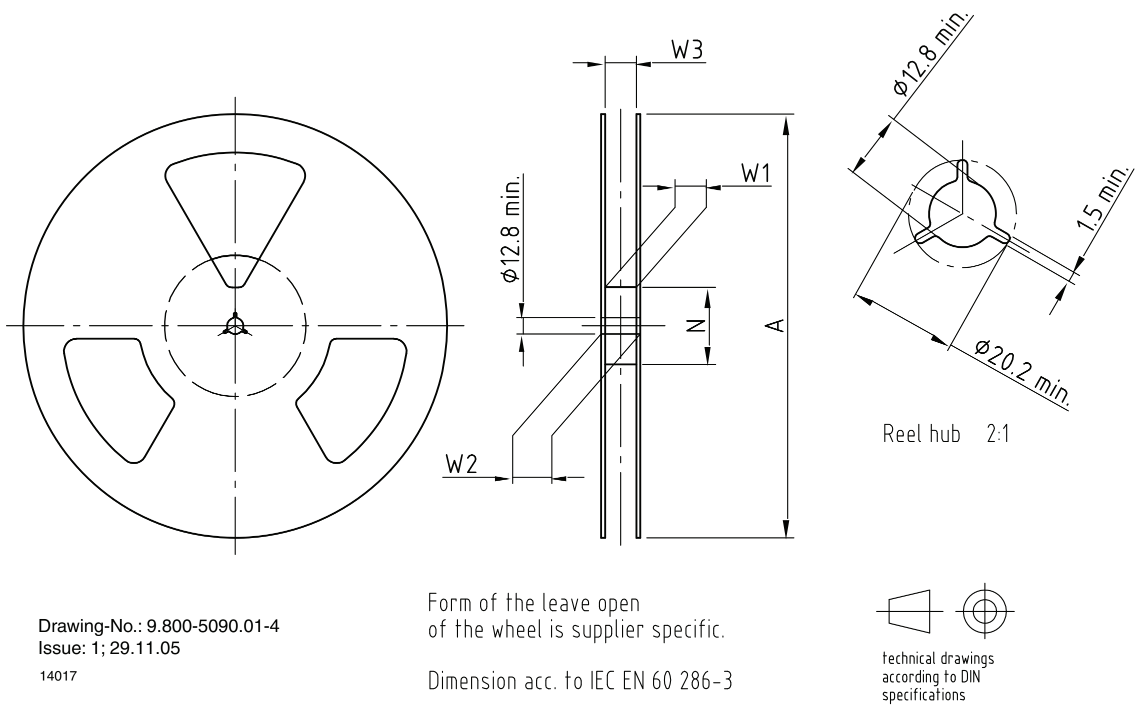


Fig. 7 - Package Drawing and Solder Footprints for Top and Side View Mounting TFDU6103,
Tolerance ± 0.2 mm if not otherwise mentioned

REEL DIMENSIONS in millimeters



TAPE WIDTH (mm)	A MAX. (mm)	N (mm)	W_1 MIN. (mm)	W_2 MAX. (mm)	W_3 MIN. (mm)	W_3 MAX. (mm)
24	330	60	24.4	30.4	23.9	27.4

TAPE DIMENSIONS in millimeters

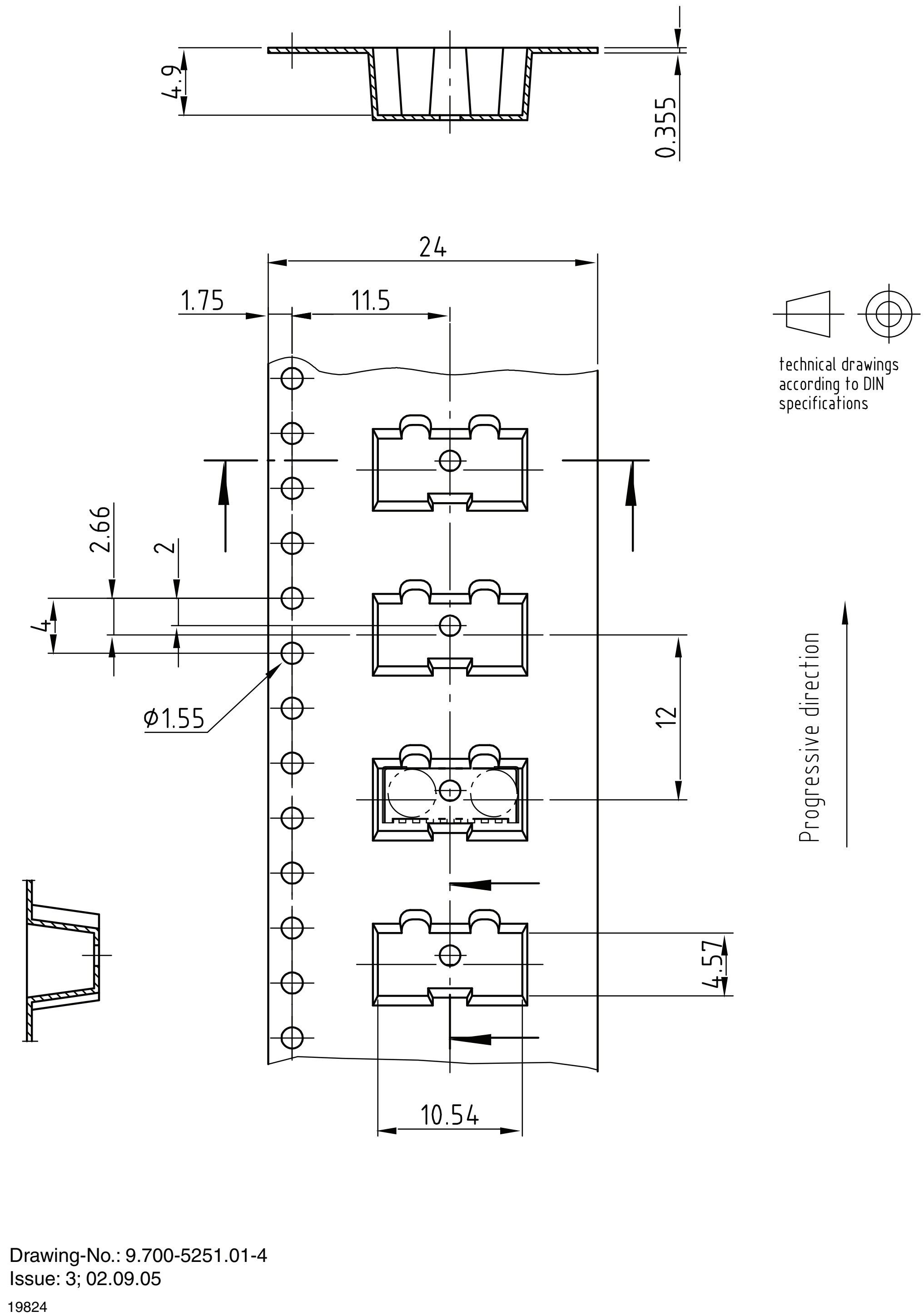


Fig. 8 - Tape Drawing, TFDU6103 for Top View Mounting, Tolerance ± 0.1 mm

TAPE DIMENSIONS in millimeters

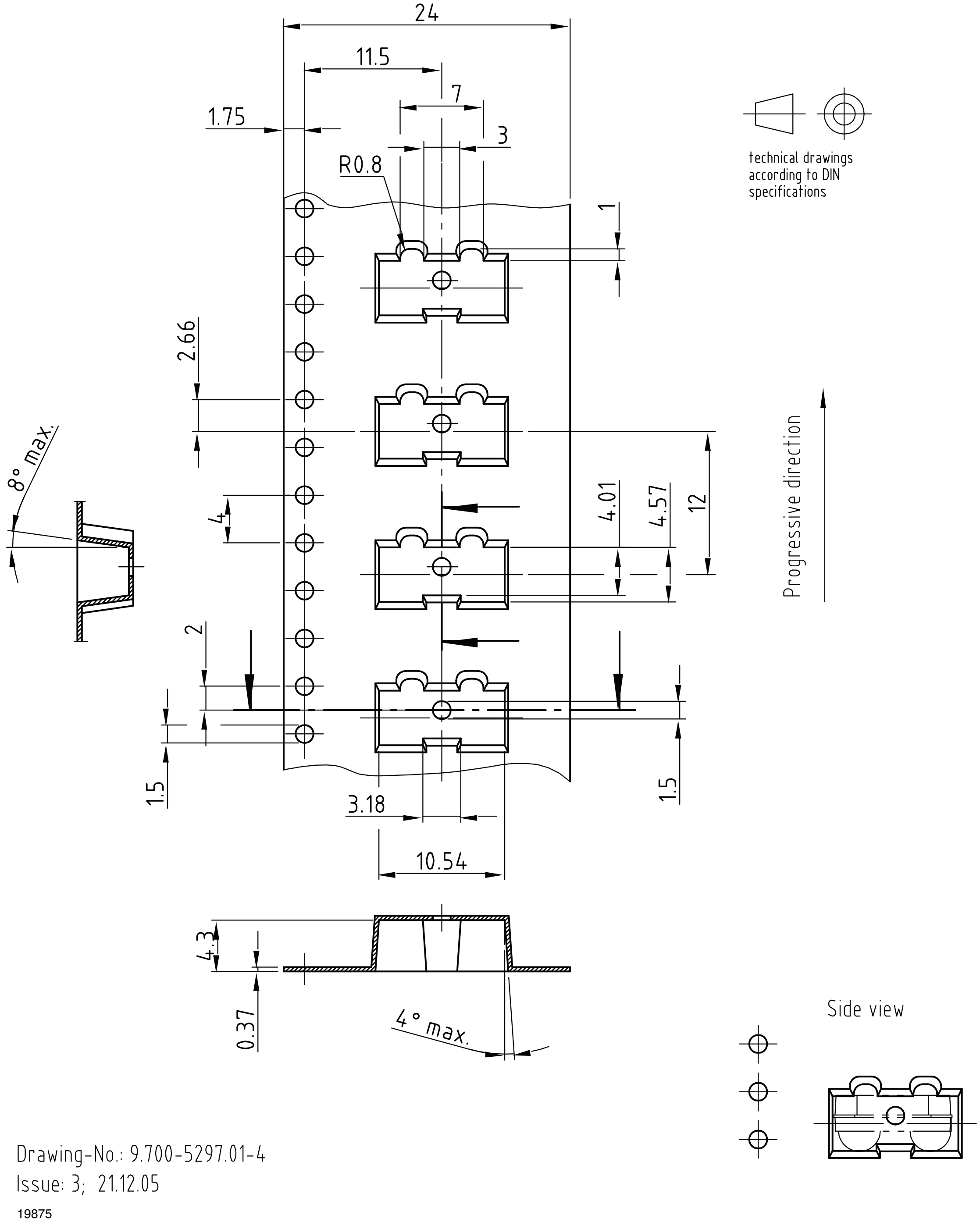


Fig. 9 - Tape Drawing, TFDU6103 for Side View Mounting, Tolerance ± 0.1 mm

Disclaimer

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