silicon systems®
A TDK Group Company

# SSI 32F8021/8023
## Low-Power Programmable Electronic Filter
## Preliminary Data

T-64-05 November 1991

3

### DESCRIPTION

The SSI 32F8021/8023 Programmable Electronic Filter provides an electronically controlled low–pass filter. A seven–pole, .05° Equiripple-type linear phase, low–pass filter is provided. This programability combined with low group delay variation makes the SSI 32F8021/8023 ideal for use in constant density recording applications. Double differentiation pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The SSI 32F8021/8023 programmable equalization and bandwidth characteristics are controlled by external DACs. The circuit is optimized to be used with the SSI 32P4620 and 54x series pulse detectors.

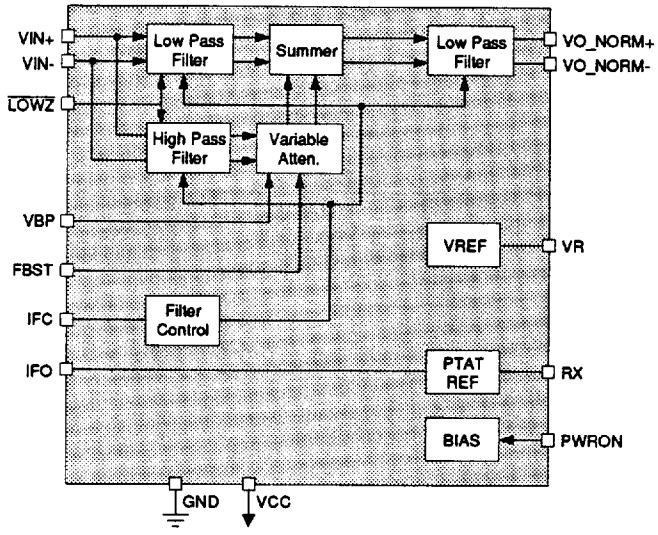
The 32F8023 is the same as the 8021, but with a low impedance switch instead of the frequency boost enable pin.

The SSI 32F8021/8023 requires only a +5V supply and is available in 16-pin DIP, SON, and SOL packages.

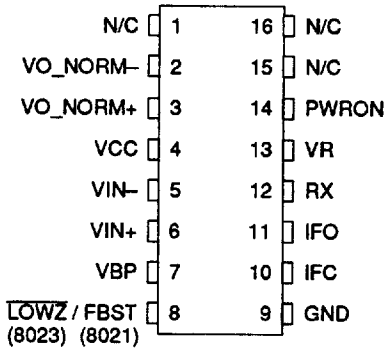
### FEATURES

- **Ideal for constant density recording applications**
- **Programmable filter cutoff frequency (*fc* = 1.5 to 8 MHz)**
- **Programmable pulse slimming equalization (0 to 9 dB boost at the filter cutoff frequency)**
- **Differential filter input and outputs**
- **±10% cutoff frequency accuracy**
- **±2% maximum group delay variation from 1.5 - 8 MHz**
- **Total harmonic distortion less than 1%**
- **No external filter components required**
- **+5V only operation**
- **16-pin DIP, SON, and SOL package**

### BLOCK DIAGRAM




### PIN DIAGRAM




CAUTION: Use handling procedures necessary for a static sensitive component.

## PIN DESCRIPTIONS

| NAME | DESCRIPTION |
|---|---|
| VIN+, VIN- | DIFFERENTIAL SIGNAL INPUTS. The input signals must be AC coupled to these pins. |
| VO_NORM+, VO_NORM- | DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to the pulse detector. |
| IFC | FREQUENCY PROGRAM CONTROL. The filter cutoff frequency FC, is set by an external current sink, from this pin. IFC must be proportional to current IFO. This current can be set with an external current generator such as a DAC, referenced to IFO. |
| IFO | PTAT CURRENT REFERENCE OUTPUT. This pin ouputs a PTAT reference current which is externally scaled for control input into IFC. IFO is proportional to absolute temperature (PTAT). |
| RX | PTAT REFERENCE CURRENT SET. PTAT (proportional to absolute temperature) reference current IFO is equivalent to the current set on this pen. |
| VBP | FREQUENCY BOOST PROGRAM INPUT. The slimmer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low. |
| FBST | FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry (32F8021 only). |
| $\overline{\text{LOWZ}}$ | A high logic level or open input selects the high-impedance mode, at VIN±, a low-logic level selects the low impedance input state (32F8023 only). |
| PWRON | POWER ON. A high logic level enables the chip. A low level puts the chip in a low power state. A low or open circuit disables the chip. |
| VR | REFERENCE VOLTAGE. Internally generated reference voltage. |
| VCC | +5 VOLT SUPPLY. |
| GND | GROUND |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

| PARAMETER | RATINGS | UNIT |
|---|---|---|
| Storage Temperature | -65 to +150 | °C |
| Junction Operating Temperature, Tj | +130 | °C |
| Supply Voltage, VCC | -0.5 to 7 | V |
| Voltage Applied to Inputs | -0.5 to VCC | V |
| Maximum Power Dissipation, $f$c = 8 MHz, Vcc = 5.5V | 198 | mW |

# SSI 32F8021/8023
# Low-Power Programmable Electronic Filter

T-64-05

3

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | RATINGS | UNIT |
|---|---|---|
| Supply voltage, VCC | 4.5 < VCC < 5.50 | V |
| Ambient Temperature Range | 0 < Ta < 70 | °C |

## ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| *Power Supply Characteristics* | | | | | | |
| ICC, Power Supply Current | | PWRON = 0.8V | | | 0.5 | mA |
| ICC, Power Supply Current | | PWRON ≥ 2.2V | | 26 | 32 | mA |
| PD | Power Dissipation | PWRON ≥ 2.2V, VCC = 5.0V | | 130 | 160 | mW |
| | | PWRON ≥ 2.2V, VCC = 5.5V | | 143 | 176 | mW |
| *DC Characteristics* | | | | | | |
| VIH | High Level Input Voltage | TTL input | 2.0 | | | V |
| VIL | Low Level Input Voltage | | | | 0.8 | V |
| IIH | High Level Input Current | VIH = 2.7V | | | 20 | µA |
| IIL | Low Level Input Current | VIL = 0.4V | | | −1.5 | mA |
| *Filter Characteristics* | | | | | | |
| *fc* | Filter Cutoff Frequency | Rx = 5 kΩ<br>$fc = 8.0\ \text{MHz} \times \frac{\text{IFC}}{4\ \text{IFO}}$ | 1.5 | | 8.0 | MHz |
| FCA | Filter *fc* Accuracy | *fc* = 8 MHz | −10 | | +10 | % |
| AO | VO_NORM Diff Gain | F = 0.67 *fc*, FB = 0 dB | 0.8 | | 1.2 | V/V |
| FB | Frequency Boost at *fc* | $FB(dB) = 20\ \log\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$<br>VBP = VR | | 9.2 | | dB |
| FBA | Frequency Boost Accuracy | FB = 9.0 dB | −1 | | +1 | dB |
| TGD0 | Group Delay Variation Without Boost | *fc* = 8 MHz, VBP = 0V<br>F = 0.2 *fc* to *fc* | −1.3 | | +1.3 | ns |
| | | *fc* = 1.5 MHz - 8 MHz<br>F = 0.2 *fc* to *fc*, VBP=0V | −2 | | +2 | % |

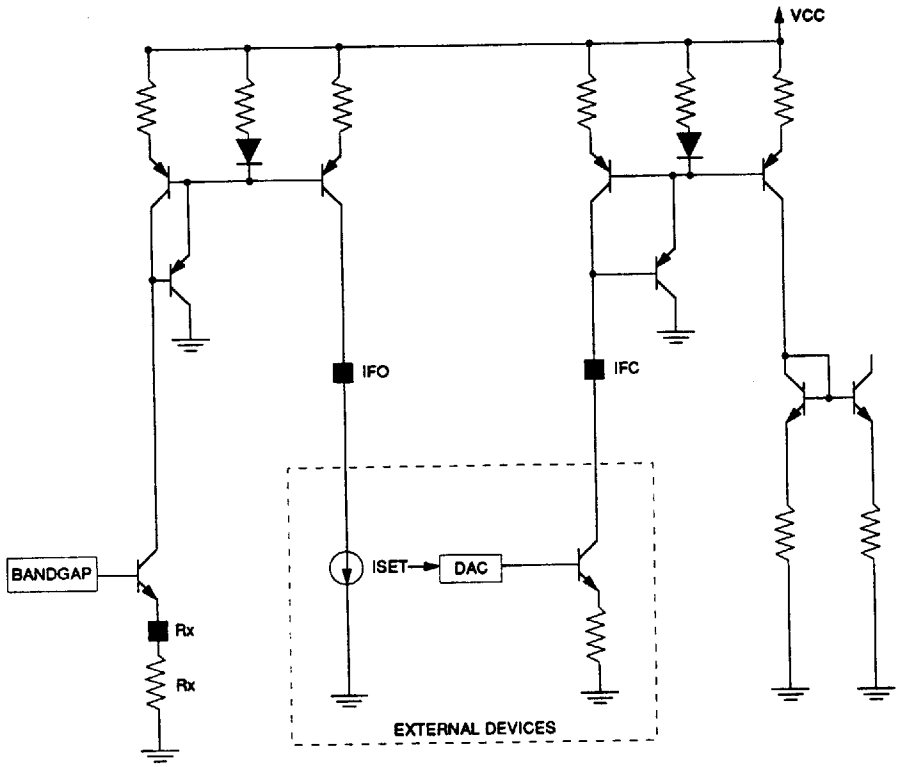
**ELECTRICAL CHARACTERISTICS,** (Continued)
Unless otherwise specified recommended operating conditions apply.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| *Filter Characteristics, continued* | | | | | | |
| TGDB | Group Delay Variation With Boost | $fc$ = 8 MHz, VBP = VR<br>F = 0.2 $fc$ to $fc$ | −1.3 | | +1.3 | ns |
| | | $fc$ = 1.5 MHz - 8 MHz<br>F = 0.2 $fc$ to $fc$, VBP=VR | −2 | | +2 | % |
| VIF | Filter Input Dynamic Range | THD = 1% max, F = 0.67 $fc$ | 1.0 | | | Vpp |
| VOF | Filter Output Dynamic Range | THD = 1% max, F = 0.67 $fc$ | 1.0 | | | Vpp |
| VIF | Filter Input Dynamic Range | THD = 3% max, F = 0.67 $fc$ | 2.0 | | | Vpp |
| VOF | Filter Output Dynamic Range | THD = 3% max, F = 0.67 $fc$ | 2.0 | | | Vpp |
| RIN | Filter Diff Input Resistance | LOWZ = high or open | 3.0 | 4.0 | | kΩ |
| | | LOWZ = low | | 150 | 300 | Ω |
| CIN | Filter Input Capacitance | | | | 7 | pF |
| EOUT | Output Noise Voltage Normal Output | BW = 100 MHz, Rs = 50Ω<br>IFC = 0.6 mA, VBP = VR | | 4.1 | | mVRms |
| EOUT | Output Noise Voltage Normal Output | BW = 100 MHz, Rs = 50Ω<br>IFC = 0.6 mA, VBP = 0.0V | | 2.7 | | mVRms |
| IO− | Filter Output Sink Current | | 1.0 | | | mA |
| IO+ | Filter Output Source Current | | 2.0 | | | mA |
| RO | Filter Output Resistance (Single ended) | IO+ = 1.0 mA | | | 60 | Ω |
| *Filter Control Characteristics* | | | | | | |
| VR | Reference Voltage | | 2.0 | | 2.40 | V |
| VBP | Frequency Boost Control Voltage Range | VR = 2.2V<br>FBOOST = 0 to 9.2 dB | 0 | | 2.2 | V |
| VRX | PTAT Reference Current Set Output Voltage | TA = 25°C<br>IRX = 0 - 0.6 mA<br>Rx > 1.25 kΩ | | 750 | | mV |
| IFO | PTAT Reference Current, Output Current Range | TA = 25°C<br>1.25 kΩ < Rx < 6.8 kΩ<br>IFO = VRX/Rx<br>VRX = 750 mV | 0.11 | | 0.6 | mA |
| IFC | PTAT Programming Current Range | TA = 25°C, VRX = 750 mV | 0.11 | | 0.6 | mA |

**TIMING CHARACTERISTICS**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Transition to/from $\overline{\text{LOWZ}}$ (8023) | | | TBD | | ns |
| Transition to Idle Mode | PWRON switches from high to low | | TBD | | ns |
| Transition from Idle Mode | PWRON switches from low to high | | TBD | | µs |

3




VRX = 750 mV @25°C

IRX = IFO

IFC programming range: 0.11 mA to 0.60 mA @25°C
(1.5 to 8.0 MHz: No Boost)

The IFC (programming current) is scaled from IFO (reference current) by the set-up shown above. Assuming the DAC current gain = 8.0, then programming is accomplished as follows:

MAX programming current required: IFC = 0.6 mA ($fc$ = 8.0 MHz) @25°C

IFO = IFC/8 = 0.075 mA (MAX) @25°C

IRX = IFO

IRX = 750mV/Rx @25°C

Rx = 10 kΩ

**FIGURE 1: 32F8021/8023 Frequency Programming**

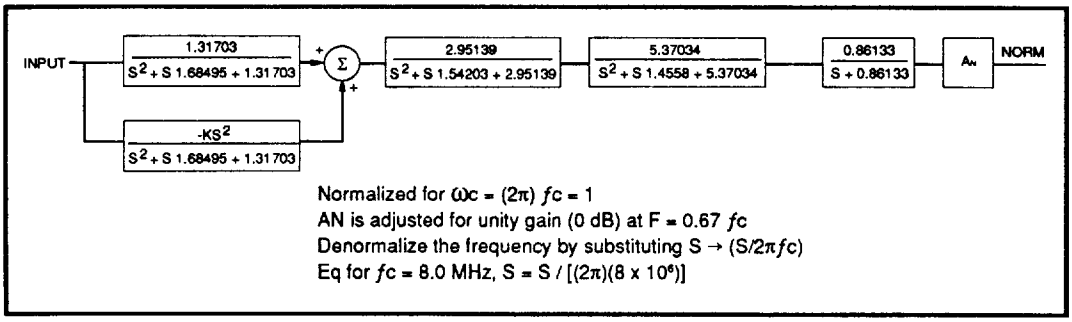



**FIGURE 2: 32F8021/8023 Normalized Block Diagram**

**TABLE 1: 32F8011 Frequency Boost Calculations**

| Assuming 9.2 dB boost for **VBP = VR** | **Boost** | **VBP/VR** |
|---|---|---|
| | 1 dB | 0.065 |
| | 2 dB | 0.137 |
| | 3 dB | 0.219 |
| | 4 dB | 0.310 |
| $\frac{VBP}{VR} \cong \frac{(10^{(FB/20)})-1}{1.884}$ | 5 dB | 0.413 |
| | 6 dB | 0.528 |
| | 7 dB | 0.658 |
| | 8 dB | 0.802 |
| | 9 dB | 0.965 |
| **or,** | **VBP/VR** | **Boost** |
| | 0.1 | 1.499 dB |
| | 0.2 | 2.777 dB |
| | 0.3 | 3.891 dB |
| | 0.4 | 4.879 dB |
| $\text{boost in dB} \cong 20\log\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$ | 0.5 | 5.765 dB |
| | 0.6 | 6.569 dB |
| | 0.7 | 7.305 dB |
| | 0.8 | 7.984 dB |
| | 0.9 | 8.613 dB |
| | 1.0 | 9.200 dB |

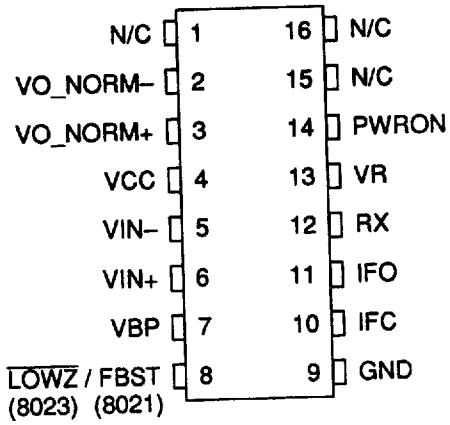
# SSI 32F8021/8023
# Low-Power Programmable Electronic Filter

T-64-05

3

## PIN DIAGRAM

(Top View)




**32F8021/8023**
**16-pin DIP, SON, SOL**

## ORDERING INFORMATION

| PART DESCRIPTION | ORDERING NUMBER | PACKAGE MARK |
|---|---|---|
| SSI 32F8021 Low-Power Programmable Electronic Filter | | |
| 16-Lead SON (150 mil) | 32F8021-CN | 32F8021 |
| 16-Lead SOL (300 mil) | 32F8021-CL | 32F8021 |
| 16-Lead PDIP | 32F8021-CP | 32F8021-CP |
| SSI 32F8023 Low-Power Programmable Electronic Filter | | |
| 16-Lead SON (150 mil) | 32F8023-CN | 32F8023 |
| 16-Lead SOL (300 mil) | 32F8023-CL | 32F8023 |
| 16-Lead PDIP | 32F8023-CP | 32F8023-CP |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914