RICOH CORP/ ELECTRONIC

No.80-01 3-1-1986

# CMOS STANDARD CELL RSC-20 Series

## GENERAL DESCRIPTION

RSC-20 series is a Standard Cell series using 2μm silicon gate CMOS with double layer metal interconnection.

It is possible to develop full custom LSIs quickly by utilizing the full CAD support system and the abundant function cell library.

RSC-20 series also allows user to utilize the one chip system easily and utilize high-speed, high-reliability and cost-reduction.

## FEATURES

- Advanced CMOS Technology for high Speed, High Density and Low Power Dissipation.
- Abundant Cell Library for Easy Design.
- Full CAD Support System.
- Various CAD Interface Support. (FUTURE NET, MENTOR IDEA 1000, DAISY LOGICIAN etc.)

## STANDARD FUNCTIONAL SPECIFICATION *1

| GRID COUNT *2 (internal cells) | GATE COUNT (typical) | I/O COUNT (maximum) | AVAILABLE PACKAGE | | | |
|---|---|---|---|---|---|---|
| | | | DIP | FLAT | PLCC | PGA |
| 200×20 | 900 | 40 | 14, 16, 18, 20, 22, 24, 28, 40 | 44 | 18, 20, 28, 44 | 68 |
| 300×30 | 1900 | 60 | 24, 28, 40, 42, 48, 64-S | 44, 60 | 18, 20, 28, 44, 68 | 68 |
| 400×40 | 3250 | 80 | 24, 28, 40, 42, 48, 64-S | 44, 60, 80 | 20, 28, 44, 68, 84 | 68, 84 |
| 500×50 | 4700 | 100 | 40, 42, 48, 64-S | 80, 100 | 28, 44, 68, 84 | 68, 84, 100 |
| 600×60 | 6250 | 120 | 40, 48, 64-S | 80, 100 | 44, 68, 84 | 68, 84, 100, 120 |

*1 · · This table indicates nominal value for reference purpose, because routing area is depend on the complexity of designed circuit.

*2 · · GRID COUNT = COLUMN GRID number × ROW GRID number

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameters | Condition | Limits | Units |
|---|---|---|---|---|
| Vcc | Supply Voltage | With respect to GND | −0.3 ~ 7 | V |
| $V_I$ | Input Voltage | | −0.3 ~ Vcc+0.3 | V |
| Vo | Output Voltage | | −0.3 ~ Vcc+0.3 | V |
| Topr | Operating Ambient Temperature | | 0 ~ 70 | ℃ |
| Tstg | Storage Temperature | | −40 ~ 125 | ℃ |

## ELECTRICAL CHARACTERISTICS

I/O CELL'S DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%)

| Symbol | Parameters | Measuring Condition | Limits | | | Units |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{IH}$ | Input "H" Voltage (TTL compatible) | | 2.0 | | Vcc+0.3 | V |
| $V_{IL}$ | Input "L" Voltage (TTL compatible) | | −0.3 | | 0.8 | V |
| $V_{OH}$ | Output "H" Voltage | $I_{OH}$ = −4mA | 2.4 | | | V |
| $V_{OL}$ | Output "L" Voltage | $I_{OL}$ = 4mA | | | 0.4 | V |
| $I_{LI}$ | Input Leakage Current | $V_I$ = 0~Vcc | −10 | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | Vo = 0~Vcc | −10 | | 10 | μA |

AC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%)

| Symbol | Parameters | Measuring Condition | Limits | | | Units |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| tpdo | Output Buffer's Delay Time | $C_L$ = 50pF | | 5.9 | | ns |
| tpdi | Input Buffer's Delay Time | FAN OUT= 1, Wire length= 3mm | | 2.9 | | ns |
| tpd | Internal Gate's Delay Time | FAN OUT= 3, Wire length= 3mm | | 2.0 | | ns |
| tacc1 | RAM's Address Access Time | FAN OUT= 3, Wire length= 3mm | | | 50 | ns |
| tacc2 | ROM's Address Access Time | FAN OUT= 3, Wire length= 3mm | | | 50 | ns |

## ■DEVELOPMENT FLOW CHART

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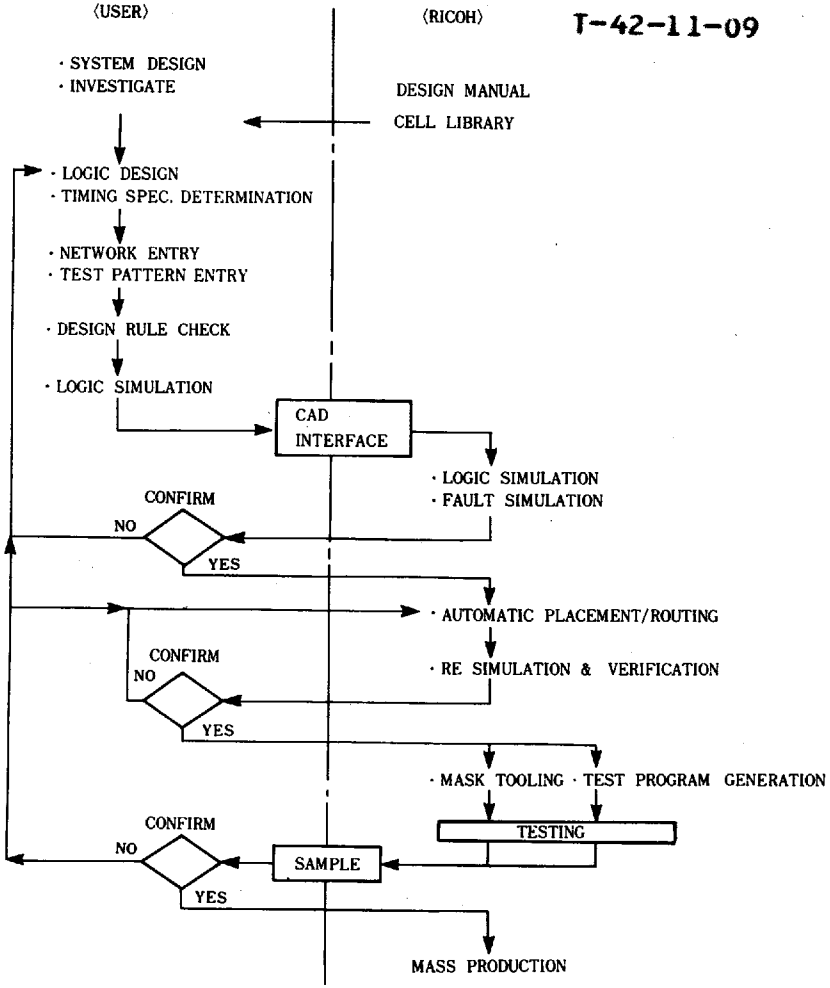
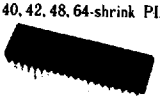
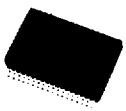



## ■PACKAGE

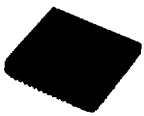
DIP 14, 16, 18, 20, 22, 24, 28, 40, 42, 48, 64-shrink PIN



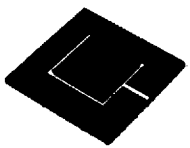
FLAT 44, 60, 80, 100 PIN



PLCC 18, 20, 28, 44, 68, 84 PIN



PGA 68, 84, 100, 120 PIN



# CMOS STANDARD CELL RSC-20 series
# CELL LIST



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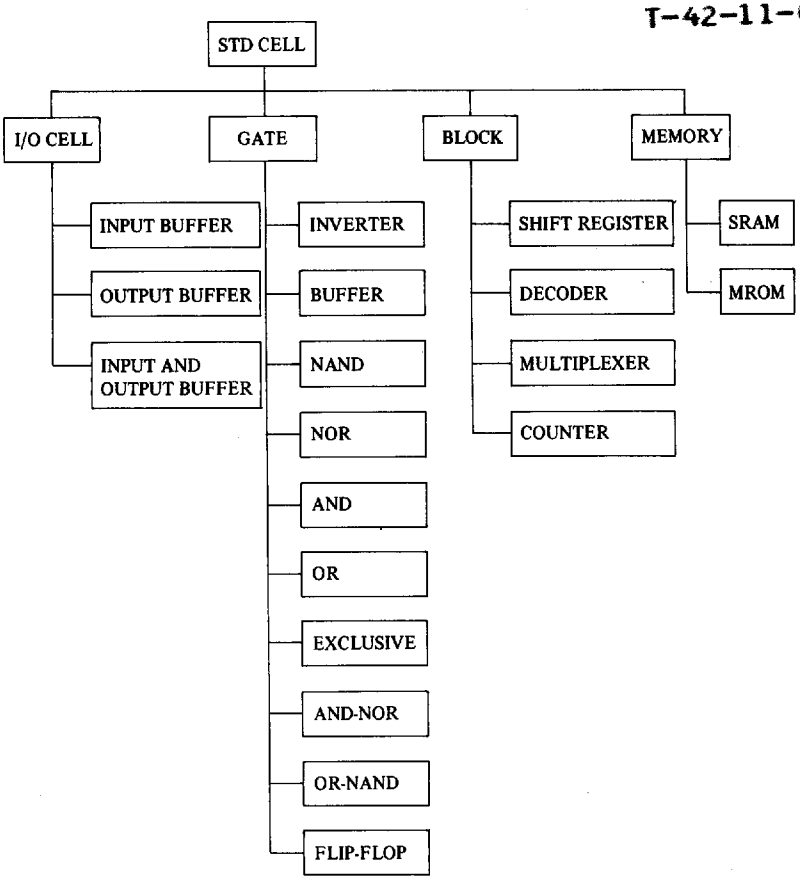

## I/O CELLS

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### INPUT BUFFER — STANDARD

| CELL | FUNCTION |
|---|---|
| INT01 | TTL Compatible Inverter |
| INT02 | TTL Buffer |

### OUTPUT BUFFER

| | |
|---|---|
| OUTTSLP | Inverter |
| OPENSLP | Open Drain Output |
| OPENSL | |
| OUTTSL | Buffer |

### OUTPUT AND INPUT BUFFER — STANDARD

| | |
|---|---|
| IOTSLP | TTL Compatible Inverter & 3-State Output |
| IOTSL | TTL Compatible Buffer & 3-State Output |

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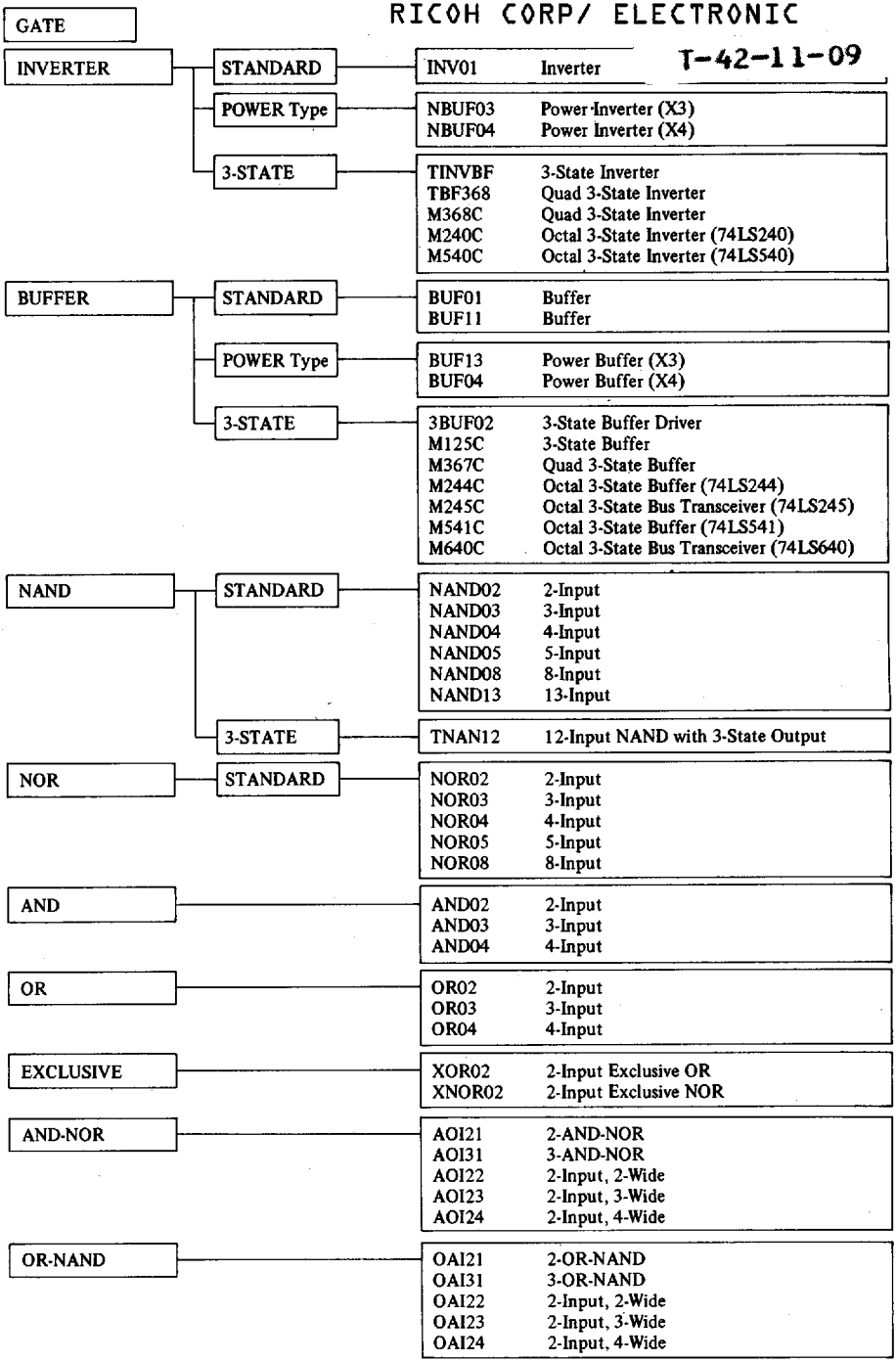

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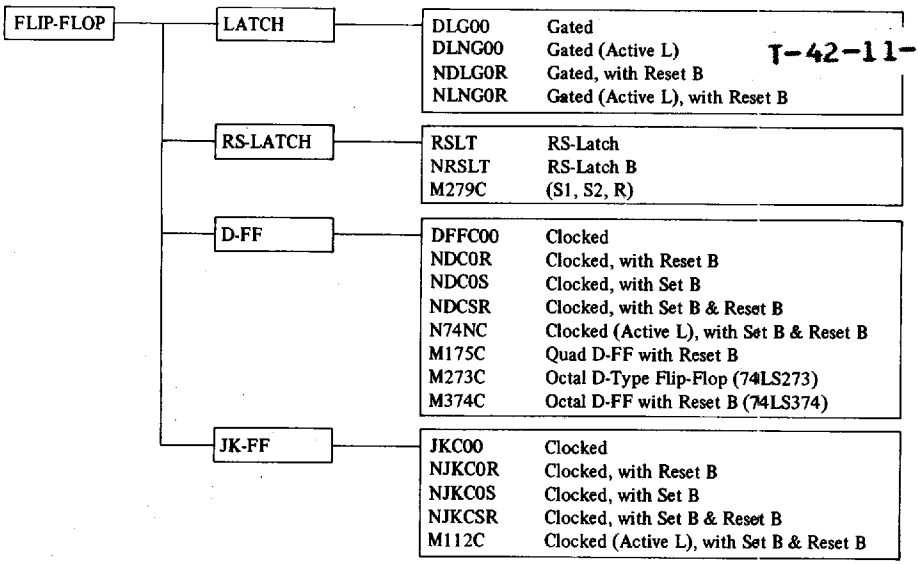
FLIP-FLOP
LATCH
DLG00 Gated
DLNG00 Gated (Active L)
NDLG0R Gated, with Reset B
NLNG0R Gated (Active L), with Reset B
RS-LATCH
RSLT RS-Latch
NRSLT RS-Latch B
M279C (S1, S2, R)
D-FF
DFFC00 Clocked
NDC0R Clocked, with Reset B
NDC0S Clocked, with Set B
NDCSR Clocked, with Set B & Reset B
N74NC Clocked (Active L), with Set B & Reset B
M175C Quad D-FF with Reset B
M273C Octal D-Type Flip-Flop (74LS273)
M374C Octal D-FF with Reset B (74LS374)
JK-FF
JKC00 Clocked
NJKC0R Clocked, with Reset B
NJKC0S Clocked, with Set B
NJKCSR Clocked, with Set B & Reset B
M112C Clocked (Active L), with Set B & Reset B

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| BLOCK | | |
|---|---|---|
| SHIFT REGISTER | M95C | 4 Bit Shift Register (74LS95) |
| | M295C | 4 Bit Shift Register with 3-State Output (74LS295) |
| | M164C | 8 Bit Parallel Output Serial Shift Register (74LS164) |
| | M165C | Parallel Load 8 Bit Shift Register (74LS165) |
| | M166C | 8 Bit Shift Register (74LS166) |
| DECODER | M139C | 2 to 4 Decoder (74LS139) |
| | M155C | Dual 2 to 4 Decoder |
| | M138C | Gated 3 to 8 Decoder (74LS138) |
| | M154C | 4 to 16 Decoder (74LS154) |
| | M42C | Bcd to Decimal Decoder (7442) |
| MULTIPLEXER | M157C | Quad 2 Bit Gated Non Inverting Mux |
| | M158C | Quad 2 Bit Gated Inverting Mux |
| | M257C | Quad 2 Bit Gated Non Inverting Mux with 3-State Output |
| | M258C | Quad 2 Bit Gated Inverting Mux with 3-State Output |
| | M153C | Dual 4 Bit Gated Non Inverting Mux |
| | M352C | Dual 4 Bit Gated Inverting Mux |
| | M353C | Dual 4 Bit Gated Inverting Mux with 3-State Output |
| | M253C | Dual 4 Bit Gated Non Inverting Mux with 3-State Output (74LS253) |
| | M251C | 8 Bit Gated Mux with 3-State Output (74LS251) |
| | M151C | 8 Bit Gated Mux |
| | M152C | 8 Bit Inverting Mux |
| | M150C | 16 Bit Gated Inverting Mux (74LS150) |
| COUNTER | SYNCHRONOUS COUNTER | M393SC Synchronous 4 Bit Binary Counter |
| | | M161D Synchronous 4 Bit Binary Counter (74LS161) |
| | | M163D Synchronous 4 Bit Binary Counter (74LS163) |
| | TTL/CMOS MSI | M393C 4 Bit Binary Counter |

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## MEMORY

### ASYNCHRONOUS SRAM

COMPILED CELL

| | | |
|---|---|---|
| Data (D) | $2 < D < 8, D = 16$ | |
| Words (W) | $32 \leqq W \leqq 1024$ | (D = 2, 3, 5, 6, 7, 16) |
| | $32 \leqq W \leqq 2048$ | (D = 8) |
| | $32 \leqq W \leqq 4096$ | (D = 4) |
| | MAX. Size | 16 K bit |

### SYNCHRONOUS SRAM *

* under development

COMPILED CELL

| | | |
|---|---|---|
| Data | 2 bit ~ 64 bit | |
| Words | 8 ~ 2048 | ($2 \leqq$ bits $\leqq 16$) |
| | 8 ~ 1024 | ($17 \leqq$ bits $\leqq 32$) |
| | 8 ~ 512 | ($33 \leqq$ bits $\leqq 64$) |
| | MAX. Size | 32 K bit |

### MROM

COMPILED CELL

| | | |
|---|---|---|
| Data | 2 ~ 16 | |
| Words | 128 ~ 32 K | |
| | MAX. Size | 64 K bit |