



## QUICKRAM ESP FAMILY

DUAL-PORT EMBEDDED RAM FOR EXTREMELY HIGH PERFORMANCE FUNCTIONS



### QUICKRAM FAMILY HIGHLIGHTS

- **High Performance** — 160MHz FIFOs, 200MHz ROM functions, 5 ns access times, 300MHz counters
- **Embedded RAM** — Multiple dual-port RAM modules (up to 25,344 bits)
- **Configurable** — four modes (64x18, 128x9, 256x4, or 512x2)
- **Synchronous/asynchronous operation** — supports FIFO/RAM/ROM functions
- **High Density** — up to 90,000 usable gates, 316 I/Os, eight clock networks

The QuickRAM™ family of Embedded Standard Products (ESPs) offers a unique combination of RAM features that are ideal for designs with extremely high-performance RAM, ROM and FIFO requirements. QuickRAM devices embed up to 25,344 bits of SRAM in an array of configurable logic, enabling RAM and ROM functions to run at speeds over 200MHz and FIFOs to run at speeds of

over 160MHz. The highly flexible 1152-bit RAM blocks can be configured in any one of four modes and can easily be cascaded to produce greater memory widths or depths. The QuickLogic development tools supporting the QuickRAM family include a "RAM Wizard" intuitive graphical user interface to further simplify the design process.

### QUICKRAM ESP FAMILY

Device	RAM Bits	RAM Blocks	Usable Gates	Logic Cells	Max. I/Os	Packages	Supply Voltage
QL4009	9,216	8	9K	160	82	68-PLCC, 84-PLCC, 100-TQFP	3.3V
QL4016	11,520	10	16K	320	118	84-PLCC, 100-TQFP, 144-TQFP	3.3V
QL4036	16,128	14	36K	672	204	144-TQFP, 208-PQFP, 256-PBGA	3.3V
QL4058	20,736	18	58K	1,008	252	208-PQFP, 240-PQFP, 456-PBGA	3.3V
QL4090	25,344	22	90K	1,584	316	208-PQFP, 240-PQFP, 456-PBGA	3.3V



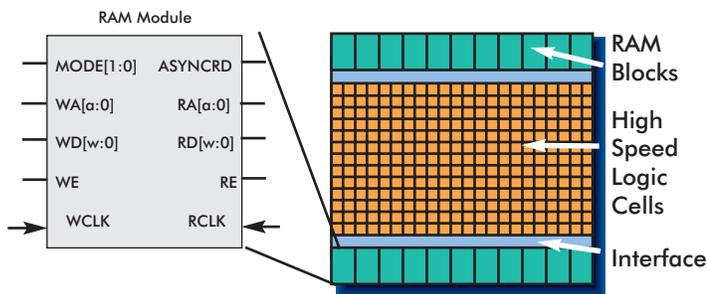
Embedded Standard Products . . . a generation ahead

## EXTREME FLEXIBILITY

Each QuickRAM device has from 10 to 22 1,152 bit RAM modules, for a total of 11,520 to 25,344 RAM bits. Separate READ and WRITE ports allow full dual-port operation and support extremely high-speed operation for dual-port functions such as FIFOs.

Using two "mode" pins, designers can configure each module into 64 (deep) x 18 (wide), 128 x 9, 256 x 4, or 512 x 2 blocks. These blocks are easily cascadable to increase their effective width or depth. The unique "by nine" architecture supports error or parity bits for bytes or words without wasting additional RAM blocks.

Each RAM module supports synchronous READ and WRITE operation, as well as asynchronous READs for ROM (look-up table) functions such as fast multipliers.



## HIGH PERFORMANCE AND HIGH DENSITY

Because QuickRAM devices are built using QuickLogic's unique ViaLink<sup>®</sup> interconnect technology and ESP architecture, they are among the largest programmable devices available. Density levels range from 16,000 to 90,000 usable gates with I/Os from 118 to 316 respectively. Even the largest devices in the family support 64x18 FIFOs at speeds of over 160MHz and 16-bit counters at over 300MHz.

## PERFECT FOR A WIDE RANGE OF HIGH-SPEED MEMORY APPLICATIONS

The high density and speed of the QuickRAM devices make them perfect for a wide range of performance-driven applications including:

- High-speed datacom and telecom functions such as ATM and SONET/SDH interfaces
- Video/imaging/graphics applications including display drivers and image processing
- PCI 0-wait state master/target interface and controller designs
- Test equipment and high-speed data acquisition

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