

General

The LL3000 series of silicon-gate HCMOS logic arrays from LSI LOGIC CORPORATION is a family of ten arrays with complexities ranging from 272 to 2550 blocks and pin counts ranging from 36 to 104. Each block is equivalent to a 2-input NAND gate. The LL3000 series uses 3.5 micron HCMOS technology with single-level metal interconnection and offers HTTL and better-than-LSTTL speeds at CMOS power consumption and noise margins.

The speeds and densities of the LL3000 series make it suitable for a variety of cost-effective applications. The smaller arrays can be used for replacement of TTL and CMOS MSI/SSI logic in medium-speed (HTTL and LSTTL) applications and for simple functions such as a priority encoder or a UART. The larger members can be used for more complex and intelligent functions such as a channel controller, a programmable vectoring interrupt controller, a display interface, etc.

Features

- Silicon-gate 3.5-micron (drawn) HCMOS technology
- Single-layer metal interconnection
- HTTL and LSTTL speeds—5 ns through a 2-input NAND gate and interconnection, $T_A = 25^\circ\text{C}$, fanout = 2, $V_{DD} = 5\text{V}$
- Optimal block structure of 2N and 2P transistors
- Complexities ranging from 272 to 2550 blocks
- Pin counts ranging up to 104
- Fully supported by LDS™ (LSI Design System)
- Extensive macrocell and macrofunction libraries
- All non-power pads configurable as inputs, outputs or bidirectional
- TTL/CMOS I/O compatibility
- Configurable output drive up to 4.8mA
- All inputs and outputs protected from over-voltage and latch-up
- Full Military capability
- Ceramic and plastic packages
- LL3110Q evaluation device available

Product Outline

Device Number	Block Complexity	Max ³ I/O	V _{DD} Pads	V _{SS} Pads	Max Pads	Gate Speed (ns) ¹	
						Typ	Max ²
49130 LL3020	272	32	1	3	36	5.0	9.0
49131 LL3030	342	36	1	3	40	5.0	9.0
49132 LL3040	420	40	1	3	44	5.0	9.0
49133 LL3060	600	48	1	3	52	5.0	9.0
49134 LL3080	812	56	1	3	60	5.0	9.0
49135 LL3110	1056	64	1	3	68	5.0	9.0
49136 LL3130	1332	72	1	3	76	5.0	9.0
49137 LL3170	1722	82	1	3	86	5.0	9.0
49138 LL3210	2162	92	1	3	96	5.0	9.0
49139 LL3250	2550	100	1	3	104	5.0	9.0

Notes: 1. 2-input NAND gate, fanout = 2, statistically necessary metal interconnection
 2. $T_A = 0$ to 70°C , $V_{DD} = 5\text{V} \pm 5\%$
 3. It may be necessary to configure additional I/O pads for V_{DD} and V_{SS} , depending on the number and drive of the output buffers. See section on 'V_{DD} and V_{SS} Requirements'.

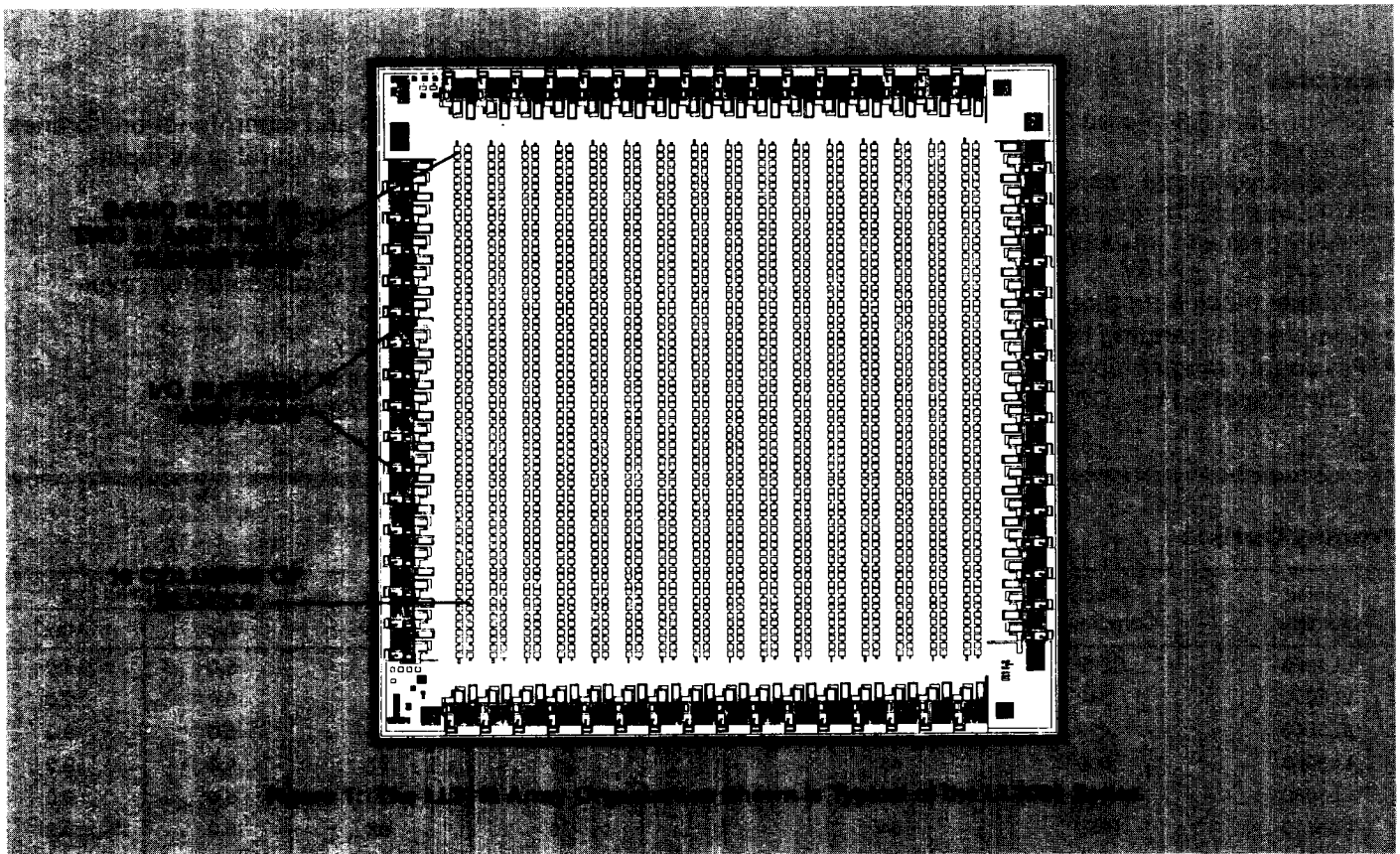
Product Description

The LL3000 series of arrays are manufactured using a proven 3.5-micron, oxide-isolated silicon-gate HCMOS fabrication process. The low parasitic capacitance of the oxide-isolated devices and their small channel geometries provide high speeds. Propagation delays through a 2-input NAND gate average 5 ns for a fanout of 2, an ambient temperature of 25° C, and 5V \pm 5% power supply voltage. A single layer of metal is used for interconnection.

Macrocells

The arrays consist of columns of blocks in the core region, I/O buffers around the periphery, and wiring channels in-between. The typical organization is shown in Figure 1. Each block consists of 2N and

2P transistors. Thus, a block can implement complete basic functions such as a 2-input NAND or 2-input NOR gate. Array complexities are stated in terms of the number of blocks, or equivalently, 2-input NAND gates. The individual N- and P-transistors in a block are not pre-connected. They can be configured into a variety of logic elements such as exclusive-OR gates or flip-flops using unique metal interconnections. These elements are called macrocells. The LL3000 series macrocell library contains over 100 macrocells with new elements being defined regularly. The 'A.C. Characteristics' section lists some of the commonly used macrocells, their propagation delays, and their complexity measured in blocks or 2-input NAND equivalent gates.



Macrocells For Level-Sensitive Scan Design

The LL3000 series macrocell libraries also contain macrocells needed to support scan testing. Scan testing simply involves the capability to serially shift the contents of all internal flip-flops off-chip in a test mode. (See LSI LOGIC Application Note A32 on

'Testing Logic Arrays' for more details). All that is required to select scan-testable storage logic elements is to add an 'S' suffix to each applicable macrocell reference, and two input entries, Test Enable and Test Source, in the netlist. See Figure 2.

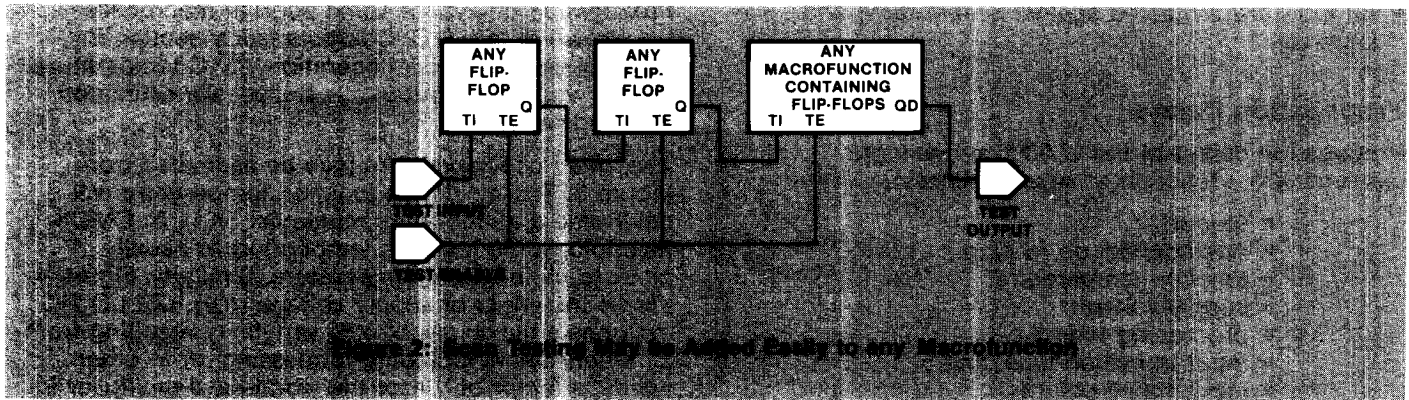


Figure 2: How Testing Pins Can Be Added Easily to any Macrofunction

Macrofunctions

Macrocells are the simplest building blocks available to the user. To specify his logic, the user builds elements of greater complexity from macrocells. These elements are called macrofunctions. Simple macrofunctions are in turn used to hierarchically build higher-level macrofunctions until the logic is completely specified.

For user convenience, a selection of macrofunctions hierarchically designed from macrocells is also available in the LL3000 series libraries. These macrofunctions implement generic functions such as counters, decoders, shift registers, etc., and are optimized for gate usage and performance characteristics. Under some circumstances, such as for upgrading existing products using 7400/4000 series MSI/SSI functions, or because of previous familiarity, designers may prefer to use 7400/4000 series functions as building blocks. LSI LOGIC also provides a selection of these elements. Overall, over two hundred macrofunctions are available in the LL3000 series library, and new ones are added regularly. Table 1 lists some representative macrofunctions. Detailed information on available macrocells and macrofunctions is provided in other LSI LOGIC publications.

I/O Buffers

Each I/O buffer around the perimeter of the chip consists of an input protection circuit and large N- and P-channel transistors for driving off-chip loads. One dedicated power pad and three dedicated ground pads are provided. All the remaining peripheral blocks can be used as input, output, bi-directional three-state, power, or ground pads. If necessary, they can even be used to buffer heavily loaded internal signals. Further flexibility is available in the use of pull-ups/pull-downs, and choice of input levels and current drive:

- All I/O pads have pull-up and pull-down resistors available (typically 50 kohm).
- Standard output drive capability is 1.6mA, (4 LSTTL or 1 standard TTL load). Additional drive may be obtained by connecting two (3.2mA) or three (4.8mA) drivers in parallel on-chip.
- Three input voltage level options are available on any input/output pin. CMOS input buffers provide standard 1.5 and 3.5 volt input levels for $V_{DD} = 5V$. In general, the input levels are $0.3V_{DD}$ and $0.7V_{DD}$. At $V_{DD} = 5V$, TTL input buffers provide standard 0.8 and 2.0 volt (2.25 volt on industrial and military devices) input levels. Schmitt trigger inputs provide 1.5 volts of hysteresis. See the 'D.C. Characteristics' section for more details.

<p>ADDERS Full adder 2-bit binary full adder similar to 7482</p> <p>COMPARATORS 4-bit magnitude comparator similar to 7485 8-bit equality comparator</p> <p>PARITY GENERATORS 8-bit odd parity detector</p> <p>REGISTERS 8-bit data latch 8-bit data register, clear direct 4-bit shift register, sync parallel load and clear 4-bit shift register, async parallel load</p>	<p>COUNTERS Binary, BCD, Gray and Johnson counters in a variety of configurations Large modulo counters</p> <p>CLOCK GENERATORS Two-phase clock generator, buffered</p> <p>DECODERS 2-to-4 decoders 3-to-8 decoders 4-to-10 decoders</p>
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Table 1: Representative Macrofunctions Available in the LL3000 Series

- All I/O's are protected against over-voltage and latch-up.

Propagation Delays

Propagation delays of the LL3000 series logic elements are a function of several factors:

- fanout,
- interconnection routing,
- junction temperature,
- supply voltage,
- processing tolerance,
- input transition time, and
- input signal polarity.

The LDS design verifier program generates the propagation delays for all networks automatically once the network has been entered into the development system. Prior to layout, these values are based on the estimated interconnections. After layout, the program is re-run and final delay values based on actual interconnections are obtained.

Prior to availability of the network in computer format, approximate delay calculations may be used. This may be done as follows:

Propagation delays for some popular macrocells are shown in the 'A.C. Characteristics' section for nominal processing, 5V operation, 25° C temperature and for various fanouts, with statistically estimated wirelengths.

The effect of temperature may be estimated from Figure 3. The maximum junction temperature will determine a temperature multiplier (K_T). In CMOS technology, the junction temperature is usually close to the ambient temperature. Similarly, Figure 4 shows the effect of supply voltage (K_V). LSI LOGIC assumes a maximum of 40% variability resulting from all other factors including processing, or in other words, a factor of 1.4 for the worst-case multiplier for all other factors (K_O).

The maximum propagation delay is:

$$T_{MAX} = K_O \cdot K_T \cdot K_V \cdot T_{TYP}$$

A simple example will illustrate the technique.

The circuit of Figure 5 must operate over 0° C to 70° C, and 4.75V to 5.25V power supply voltage. Using Figures 3 and 4 and the 1.4 K_O multiplier, we determine the worst-case maximum delay to be $1.4 \times 1.16 \times 1.07 = 1.74$ times the typical delay.

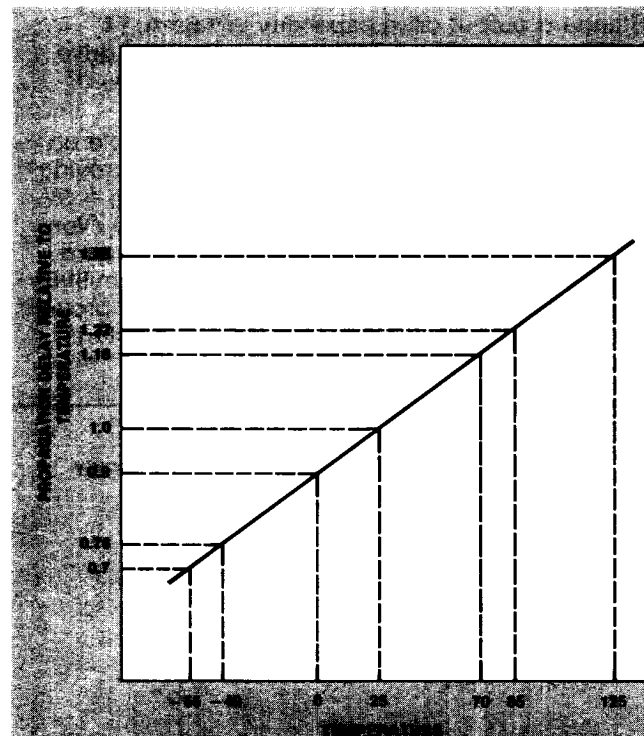


Figure 3: CMOS Propagation Delays as a Function of Temperature

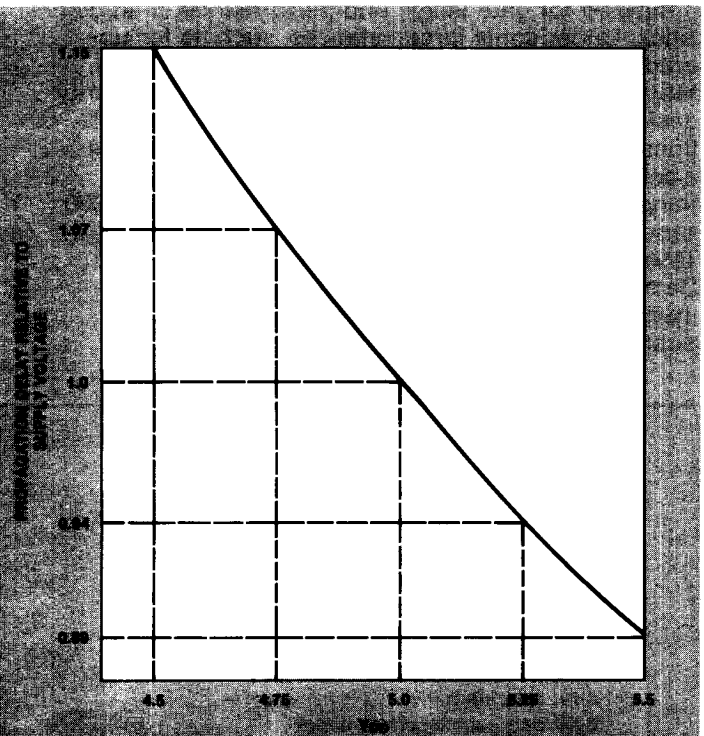


Figure 4: CMOS Propagation Delays as a Function of Supply Voltage

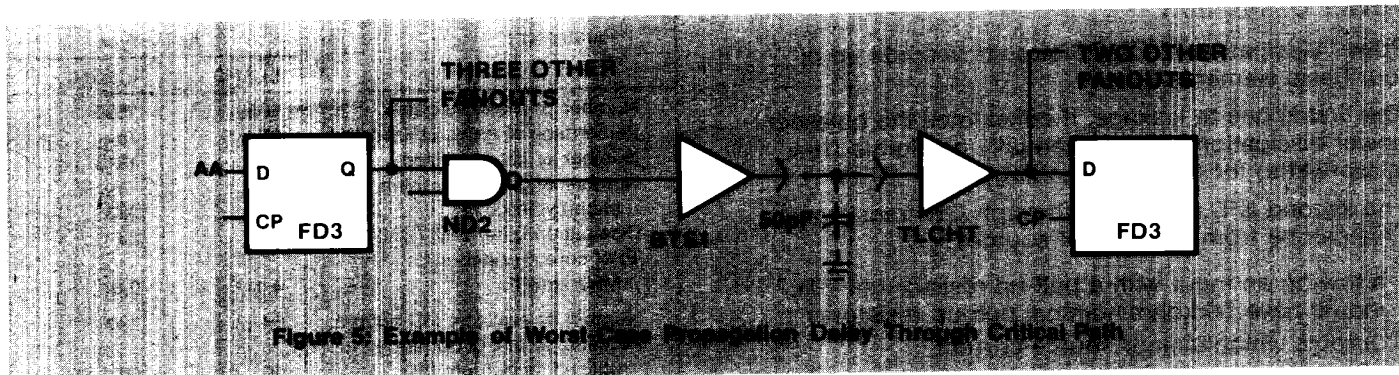


Figure 5: Example of Worst-Case Propagation Delay Through Critical Path

The FD3 flip-flop, driven by the signal AA, feeds an ND2 2-input NAND gate and three other loads. The ND2 drives a BTS1 three-state buffer directly. The BTS1 drives off-chip, through a PC board, and on to another array using a TLCHT input level shifter. The total capacitance at the output, interconnect, and input is 50pF. The TLCHT drives the D input of an FD3 D flip-flop and two other loads. The delay characteristics of all the macrocells are tabulated in Table 2. The total clock-to-clock delay is 45.2 ns typical, 78.6 ns worst-case. LDS programs are used to obtain accurate delays after the logic has been entered into the system.

- the drive capability of the buffer,
- the number of buffers switching simultaneously, and
- the location of power and ground pins relative to the outputs.

Each power and ground pad can support a maximum of 64 current units, where a current unit is the peak drive capability required for a single LS TTL load. Thus, the sum of the possible current units of all the outputs around a V_{DD} or V_{SS} pad should not exceed 64 current units. Output types can be mixed—high drive when needed, low drive when acceptable to reduce noise and power dissipation. Note that inputs are not taken into account since CMOS inputs sink and source minimal current. Table 3 summarizes the guidelines for the maximum number of output pads for a power or ground pad for each buffer type. Further, the 64 current units should be distributed as equally as possible on either side of the power or ground pad, i.e., no signal should be more than 32 current units away from a power or ground pad (see Figure 6).

Input Signal AA	FD3 FO=4	ND2 FO=1	3-state Output BTS1 C _L =50pF	TLCHT FO=3	FD3 Set-up	Typical Path Delay	W.C. Path Delay
Goes high	19.0	1.9	12.0	11.3	1.0	45.2	78.6
Goes low	10.5	3.1	19.3	6.4	1.0	40.3	70.1

Table 2: Propagation Delay Calculation

Buffer Type	Drive (LS TTL Loads)	Maximum Number of Output Pads for a V _{DD} or V _{SS} Pad
B1	4	16
B2	8	8
B3	12	5

Table 3: Maximum Number of Output Pins for Each Buffer Type

V_{DD} and V_{SS} Requirements

HCMOS is a fast technology rivaling bipolar HTTL and LSTTL speeds. High-speed operation places stringent requirements on the number of power and ground pins required to avoid current transients when the output buffers charge and discharge their output capacitance. One dedicated V_{DD} and three dedicated V_{SS} pads are provided on all members of the LL3000 series. Ordinarily, these are adequate for handling the current requirement of a design. In some cases, it may be necessary to configure additional I/O pads for V_{DD} and V_{SS} to support several high-drive outputs switching simultaneously at high speeds. For example, a transient current of 40mA can be generated when a B1 buffer switches. If twenty B1 buffers switch simultaneously, an instantaneous current of 800mA is generated through the V_{SS} bus, bonding wire, package and out to the PC board. There are therefore guidelines on the number of V_{SS} and V_{DD} pins based on three factors:

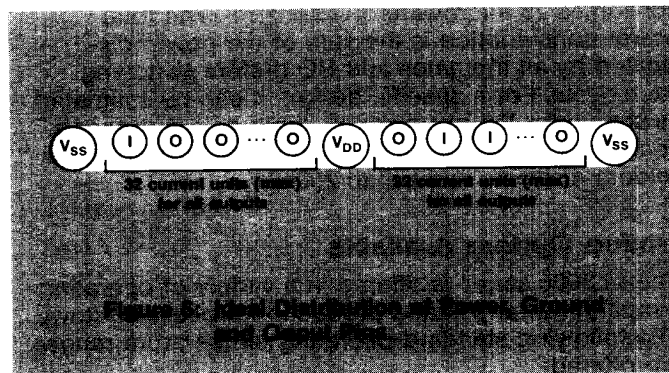


Figure 6: Pad Design of a Power, Ground, and Output

Power Dissipation

Power dissipation in CMOS circuits is made up of four basic elements.

The first is due to leakage. It constitutes the quiescent power dissipation and is essentially negligible (few micro-watts) for CMOS technology.

The second is D.C. current through ON transistors. This can be from a variety of sources:

- a low on an input with a pull-up resistor (all TTL inputs have 50 kohm nominal pull-up resistors),
- outputs which sink or source current,
- any unconnected inputs without a pull-up or pull-down,
- any internal gates whose inputs are floating (e.g., a data bus with all the lines disabled),
- inputs at worst-case levels, particularly TTL inputs at 2 volts.

Care should be exercised during logic design to make sure that there is a test condition in which all this D.C. current may be turned off, so that D.C. leakage may be easily measured.

The third source of power dissipation is due to overlap currents when the P- and N-transistors are switching from the high-to-low state or vice-versa. This contributes less than 10% of the power dissipated and occurs for the transition period when

$$V_{TH(N)} < V_{IN} < V_{DD} - V_{TH(P)}$$

The fourth and the most important factor is the charging and discharging of circuit capacitance. The charging of a capacitor C to a voltage V through a P-channel device builds up a charge CV and stores energy CV^2 . This energy is later discharged through an N-channel transistor in the CMOS P-N pair. When such switching takes place at a frequency 'f', the resulting power dissipated in the CMOS circuit is equivalent to $P = CV^2f$. This A.C. power dissipation usually contributes in excess of 90% of the total power dissipated. Thus, the power dissipation in a CMOS circuit is essentially a function of the frequency and logic configuration. Each internal gate in the LL3000 series typically consumes 23 microwatts/gate/MHz. Each I/O buffer, with its higher output capacitance and larger capacitive loads, consumes 25 microwatts/I/O/MHz/pF. The total power consumption is the sum of the power dissipated by all the gates and I/O buffers switching each cycle. For a specific design, it can be estimated as shown for the examples in Table 4. In our experience, even large arrays operating at high clock rates seldom dissipate more than 200mW.

Product Options Available

The LL3000 series is offered in a variety of operating temperature ranges and production processing flows. The following standard operating temperature ranges are offered:

Parameter	Array Type	
	LL3110	LL3250
Number of available gates	1056	2550
Percentage of gates utilized (%)	85	75
Number of gates utilized	898	1913
Number of gates switching each cycle (20%)	180	383
Dissipation/gate/MHz (μ W)	23	23
Total core dissipation/MHz (mW)	4.1	9.8
Number of available I/O buffers	64	100
Percentage of I/O buffers utilized as outputs (%)	50	50
Number of I/O buffers utilized as outputs	32	50
Number of I/O outputs switching each cycle (20%)	6.4	10.0
Dissipation/output buffer/MHz/pF (μ W)	25	25
Output Capacitive Load (pF)	50	50
Dissipation/output buffer/MHz (mW)	1.250	1.250
Total output buffer dissipation/MHz (mW)	8.0	12.5
Total dissipation/MHz (mW)	12.1	22.3
Total dissipation at 5MHz clock speed (mW)	60.5	111.5
Total dissipation at 10MHz clock speed (mW)	121.0	223.0

Table 4: Power Dissipation Calculation

- Military (-55°C to +125°C)
- Industrial (-40°C to +85°C)
- Commercial (0°C to +70°C)

Other special temperature ranges are also available.

Production flow options other than LSI LOGIC's standard commercial flow are available. The commercial flow consists of preparation of diffused wafers, metallization, wafer sort, wafer saw, optical die inspection, die attach, wire bonding, pre-seal visual inspection, seal, marking, temperature cycling, stabilization bake (plastic packages only), fine and gross leak (ceramic packages only), and final test. High-reliability processing included in the commercial flow consists of temperature cycling and stabilization bake. Burn-in and other high-reliability screening can be included to customer specifications. Full Mil 38510 qualification is available when required.

Packaging

The LL3000 series of HCMOS arrays can be packaged in a variety of plastic and ceramic dual-in line packages, leadless and leaded chip carriers, and pin grid arrays. Plastic packages are not available for the full military temperature range. The compatibility chart of Table 5 shows the packages and pin counts available for the various members of the LL3000 series.

Device Number	Max Pins	Dual-in-line Packages		Chip Carriers		Pin Grid Arrays
		Plas-tic	Cer-amic	Plas-tic	Cer-amic	
LL3020	36	16+	16+	—	28+	64
LL3030	40	16+	16+	—	28+	64
LL3040	44	16+	16+	—	28+	64
LL3060	52	16+	16+	—	28+	64
LL3080	60	22+	22+	68	28+	64
LL3110	68	22+	22+	68	28+	64+
LL3130	76	22+	22+	68	28+	64+
LL3170	86	24+	24+	68	44+	64+
LL3210	96	24+	24+	68	44+	64+
LL3250	104	40+	24+	68	44+	64+

Package families include:

- Ceramic DIPs—24, 28, 40, 42, 48 and 64 leads
- Plastic DIPs—24, 28, 40 and 48 leads
- Ceramic chip carriers—28, 44, 52, 68, 84 and 100 leads
- Plastic chip carriers—68 and 84 leads
- Ceramic Pin-grid arrays—64, 68, 84, 100 and 120 leads

Table 5: Package Selector Guide for the LL3000 Series

LL3110Q Evaluation Device

A potential user of the LL3000 series can, prior to design commencement, measure its performance under his unique system and environmental conditions. The LL3110Q contains a variety of logic functions such as 2-, 3-, or 4-input NAND gates, 2- or 4-input NOR gates, output buffers with different drive capability, a variety of different flip-flops, inverters, TTL-to-CMOS level-shifters, etc. These functions are implemented in several different test circuits. Technology parameters such as propagation delays, power consumption, input/output characteristics, etc., can be measured under different conditions of loading, supply voltage, ambient temperature, etc. See the LL3110Q data sheet for more details.

Getting Started on the Design

To get started on a logic array design, the following sequence of preliminary steps is suggested.

1. The complete system is partitioned into LSI building blocks. An effort should be made to minimize the I/O count when partitioning between user-defined VLSI. Each functional block to be implemented in a logic array is then converted to a logic schematic. The user can describe his logic using LSI LOGIC's macrofunction/macrocell libraries or 7400/4000 series functions. The use of hierarchical design techniques on the LDS design system allows design expression at these various levels. Ultimately, when the logic is compiled on LDS, it is 'flattened' into macrocells. It is advisable

to structure the complete schematic as a set of functional sub-systems such as a 16-bit ALU, a data receiver, a programmable timer or a register file, to allow comprehensible and easy hierarchical simulation.

2. The base clock frequency and the critical path timing is necessary to make the correct choice of technology. The LL3000 series can support designs operating up to 10-15MHz. The critical path timing is determined based on macrocell propagation delays (see the 'Propagation Delays' and 'A.C. Characteristics' sections). To verify the capability of a technology under the unique environmental and system conditions of a user application, an evaluation device such as the LL3110Q may be used.
3. The next step is to determine the number of I/O required and the complexity of the design. The LSI LOGIC macrocell application note actually achieves design dependments, as well as inter-block timing. For example, the LL3080 to 7 rule-of-thumb for the design, although it can be achieved.

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4. Finally, a choice of technology, package, temperature range, performance, etc., is made.

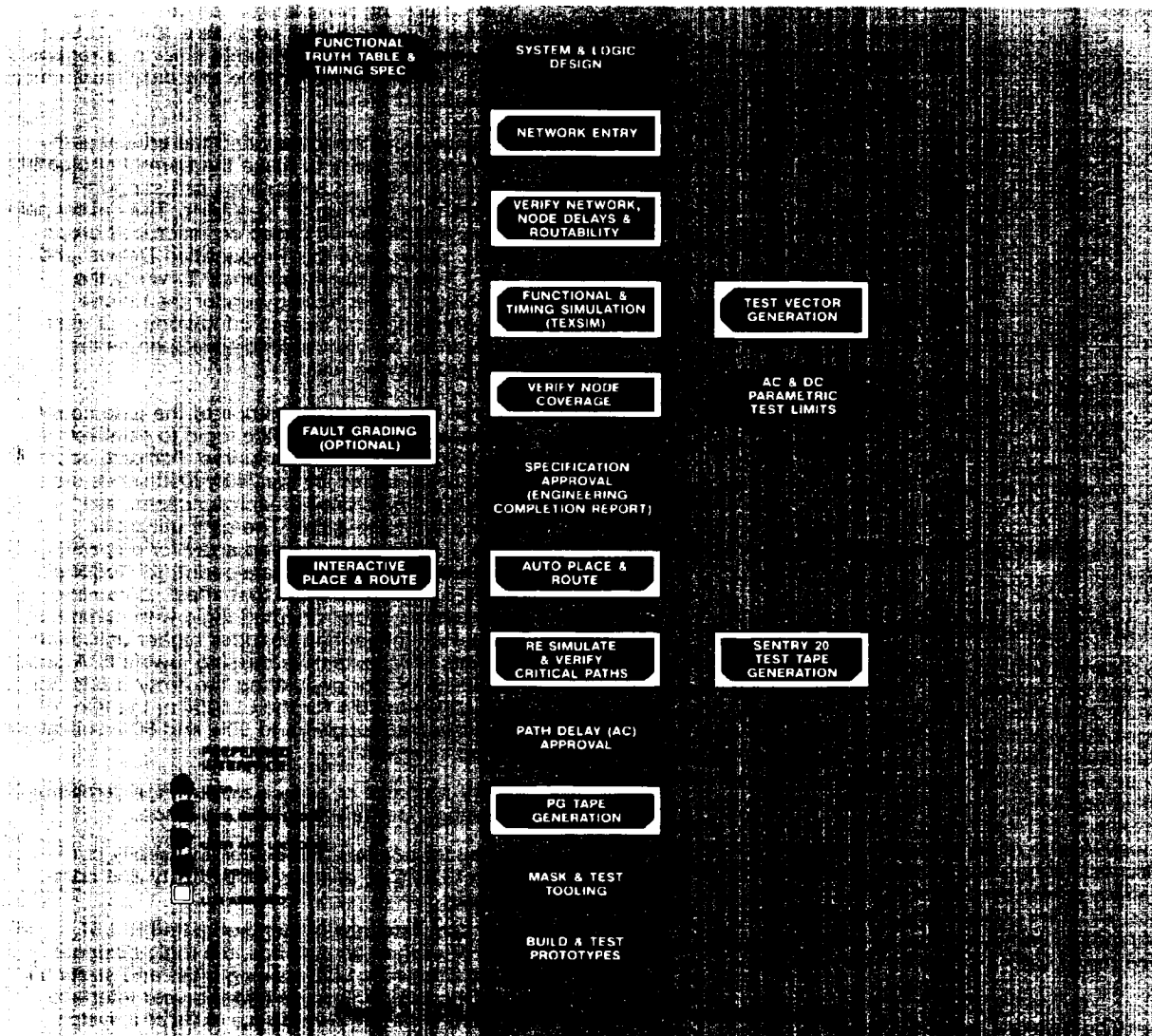
During all these steps, the customer usually consults LSI LOGIC to ensure compatibility and completeness.

A set of specifications is then submitted to LSI LOGIC. After their acceptance, the logic designer takes the one-week LDS training class and starts his design. The design process and the user interface to LDS are oriented towards the skills of a system designer rather than a semiconductor device or VLSI designer.

Alternatively, the customer can contract LSI LOGIC for a turnkey design.

Design Support and Interface

The LDS System is used for logic specification, basic network verification (gate usage, I/O pad usage, average fanout per net, estimated automatic wire-ability), logic simulation and performance analysis, automatic placement and routing, resimulation with actual wire-lengths to verify the A.C. performance, mask P.G. tape generation and test tape generation. The basic design flow is outlined in Figure 7.



Operating Characteristics

Absolute Maximum Ratings (Referenced to V_{SS})

Parameter	Symbol	Limits	Unit
DC Supply Voltage	V_{DD}	- 0.3 to + 7	V
Input Voltage	V	- 0.3 to $V_{DD} + 0.3$	V
DC Input Current	I_i	± 10	mA
Storage Temperature Range (Ceramic)	T_{STG}	- 65 to + 150	$^{\circ}C$
Storage Temperature Range (Plastic)	T_{STG}	- 40 to + 125	$^{\circ}C$

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	V_{DD}	+ 3 to + 6	V
Operating Ambient Temperature Range			
Military	T_A	- 55 to + 125	$^{\circ}C$
Industrial Range	T_A	- 40 to + 85	$^{\circ}C$
Commercial Range	T_A	0 to + 70	$^{\circ}C$

DC Characteristics

Specified at $V_{DD} = 5V \pm 5\%$ ambient temperature over the specified temperature range(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage (2)					
	TTL Inputs				0.8	V
	CMOS Levels				1.5	V
V_{IH}	High Level Input Voltage (2)					
	TTL Inputs, Commercial Temperature Range		2.0			V
	TTL Inputs, Military and Industrial Temperature Range		2.25			V
	CMOS Levels		3.5			V
V_{T+}	Schmitt-Trigger, Positive-going Threshold			3.0	4.0	V
V_{T-}	Schmitt-Trigger, Negative-going Threshold		1.0	1.5		V
ΔV	Hysteresis, Schmitt Trigger		1.0	1.5		V
						V
I_{IN}	Input Current, CMOS, TTL Inputs	$V_{IN} = V_{DD}$	-10	± 1	10	μA
	Inputs with pull-down resistors	$V_{IN} = V_{DD}$		150		μA
	CMOS inputs	$V_{IN} = V_{SS}$	-10	± 1	10	μA
	TTL Inputs & Inputs with Pull-up Resistors	$V_{IN} = V_{SS}$		-150		μA
V_{OH}	High Level Output Voltage					
	Type B1	$I_{OH} = -1.6mA$	2.4	4.5		V
	Type B2 (3)	$I_{OH} = -3.2mA$				
	Type B3 (4)	$I_{OH} = -4.8mA$				
V_{OL}	Low Level Output Voltage					
	Type B1	$I_{OL} = 1.6mA$		0.2	0.4	V
	Type B2 (3)	$I_{OL} = 3.2mA$				
	Type B3 (4)	$I_{OL} = 4.8mA$				
I_{OZ}	Three-State Output Leakage Current	$V_{OH} = V_{SS}$ or V_{DD}	-10	± 1	10	μA
I_{OS}	Output Short Circuit Current (5)	$V_{DD} = \text{Max } V_O = V_{DD}$	25		90	mA
		$V_{DD} = \text{Max}, V_O = 0V$	-7		-28	mA
I_{DD}	Quiescent Supply Current	$V_{IN} = V_{DD}$ or V_{SS}	User-Design Dependent			
C_{IN}	Input Capacitance	Any Input (6)		5		pF
C_{OUT}	Output Capacitance	Any Output (7)		7		pF

Notes:

- Military temperature range is $-55^{\circ}C$ to $+125^{\circ}C$, $\pm 10\%$ power supply (ceramic packages only); Industrial temperature range is $-40^{\circ}C$ to $+85^{\circ}C$, $\pm 5\%$ power supply; Commercial temperature range is $0^{\circ}C$ to $70^{\circ}C$, $\pm 5\%$ power supply.
- In general, for any V_{DD} between the allowable limits ($+3V$ to $+6V$), $V_{IL} = 0.3V_{DD}$ and $V_{IH} = 0.7V_{DD}$.
- Requires two output pads.
- Requires three output pads.
- Type 5LS output. Output short circuit current for other outputs will scale. Not more than one output may be shorted at a time for a maximum duration of one second.
- Not applicable to assigned bi-directional buffer (excluding package).
- Output using single buffer structure (excluding package).

AC Characteristics

$$V_{DD} = 5V, T_A = 25^{\circ}C$$

Delays through interconnects, consisting of metal and polysilicon, are included in the propagation delays. Interconnect wirelengths are assumed from statistical distributions for given fanouts. (See note next page).

Macrocell	Input Transition	Propagation Delays				Equivalent Gate Count		
		Output Load Capacitance						
		15pF	50pF	85pF	100pF			
UNIDIRECTIONAL BUFFERS								
3-state Output Buffer with 1.6mA Drive (BTS1)	tPHL	9.1	12.0	14.6	15.7	5		
	tPLH	10.9	19.3	27.7	31.3			
3-state Output Buffer with 3.2mA Drive (BTS2)	tPHL	9.0	10.8	12.3	12.8	5		
	tPLH	10.8	15.1	19.4	21.2			
3-state Output Buffer with 4.8mA Drive (BTS3)	tPHL	9.2	10.7	11.8	12.2			
	tPLH	11.7	14.7	17.6	18.8			
OUTPUT BUFFERS								
Output Buffer with 1.6mA Drive (B1)	tPHL	6.2	9.2	11.8	12.9	1		
	tPLH	6.2	14.7	23.2	26.8			
Output Buffer with 3.2mA Drive (B2)	tPHL	5.2	7.2	8.7	9.2	2		
	tPLH	4.3	8.6	12.9	14.7			
		Fanout						
		1	2	3	4	8		
INPUT RECEIVERS								
Input Buffer with CMOS Inputs (IBUF)	tPHL	5.4	6.3	7.9	10.1	21.3	0	
	tPLH	5.7	7.2	9.5	12.6	32.1		
Inverting Input Buffer with CMOS Inputs (IBUFN)	tPHL	4.1	5.2	6.7	8.9	23.5	3	
	tPLH	4.7	6.1	8.1	11.0	27.3		
Input Buffer with TTL Inputs (TLCHT)	tPHL	8.6	9.6	11.3	13.5	25.0	3	
	tPLH	3.2	4.4	6.4	9.3	28.2		
INTERNAL BUFFERS								
Single Inverter (IVD)	tPHL	1.2	2.2	3.9	6.0	21.4	1	
	tPLH	2.4	4.5	7.2	10.2	29.9		
Power Inverter (IVP)	tPHL	1.0	2.0	3.5	5.9	20.7	1-2	
	tPLH	1.8	3.2	5.6	8.8	27.1		
LOGIC GATES								
2-input NAND (ND2)	tPHL	1.9	3.1	5.1	7.6	23.3	1-2	
	tPLH	3.1	5.3	8.2	11.5	30.4		
2-input NOR (NR2)	tPHL	1.3	2.3	3.9	6.3	21.4	1-2	
	tPLH	4.5	8.1	12.1	16.4	36.9		
3-input NAND (ND3)	tPHL	2.8	4.4	6.6	9.3	25.6	2	
	tPLH	3.6	5.9	8.6	12.3	32.2		
3-input NOR (NR3)	tPHL	1.4	2.5	4.2	6.5	21.7	2	
	tPLH	8.9	13.8	19.1	24.6	47.8		
FLIP-FLOPS								
D Flip-flop with Set Direct, Clear Direct (FD3)	Q	tPHL	7.0	8.5	10.0	10.5	29.0	7
		tPLH	8.5	11.0	15.0	19.0	38.5	
	QN	tPHL	10.0	11.8	14.0	16.5	31.0	
		tPLH	10.5	13.0	16.5	18.0	41.0	
		t _s	1.0	1.0	1.0	1.0	1.0	
		t _h	1.0	1.0	1.0	1.0	1.0	

Note: Higher performance can be achieved through careful minimization of polysilicon in a selected number of nets during layout and routing. The user can specify up to fifteen very critical nets and thirty fanout critical nets during logic specification. The propagation speeds can be significantly improved in most cases, particularly for high fanouts.

NOTES