Ordering number : EN4412A

CMOS IC

LC7442, 7442E

PIP Controller

Overview

The LC7442 and LC7442E are memory controller for PIP (picture-in-picture) systems for TV sets and VCRs. Since this IC includes 3 built-in D/A converter circuits on chip, a component-type PIP system can be constructed by combining this product with memory and an A/D converter such as the LC7480.

Features

- Horizontal resolution: 600 TV lines*1
- Three built-in D/A converter provided on-chip in the PIP memory controller block
- High image quality display provided by vertical filter function frame display*2
- Built-in even/odd field determination circuit
- Built-in PLL circuit (requires external LPF)
- Handles NTSC/PAL, TV/VCR, and multi-mode systems (NTSC-PAL)*3
- Sub-screen specifications
  - — Display modes: 2-screen, 3-screen, and 4-screen*2
  - — Display on/off and frame on/off/color switching, wipe function
  - — Supports switching between fixed (4 corners) and arbitrary (8-bit specification of vertical and horizontal position) display positions
  - — The size of the display area can be either variable or 1/9 of the main picture area, i.e 1/3 of the vertical and 1/3 of the horizontal dimensions of the screen
  - — Horizontal resolution of about 250 dots (Y signal)
  - — Gradations (quantization): 64 (6 bits)
- Operating power supply voltage: 5 V ±10%
- Package: QIP64E, DIP64S

Notes 1.When aspect correction is not performed

	D/A clock
Y	15.00 MHz
R-Y	3.75 MHz
B-Y	3.75 MHz

2. The specifications vary with the external memory as listed in the table below.

Display \ Memory	256 k	1 M
1 screen	Δ	O
2 screens	×	O
3 screens	×	Δ
4 screens	×	Δ

Single-screen display consists of displaying only one screen in 2-screen mode.

O: Both dynamic and static images can be frame displayed
Δ: Only dynamic images can be frame displayed
×: Not possible

3. Multi-mode is only supported when 1M of external memory is provided.

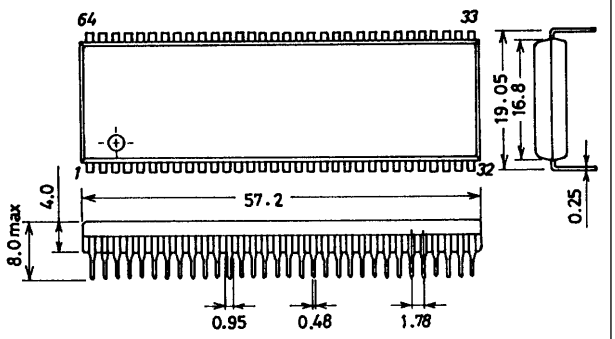
4. See the separate “APPLICATION NOTE” document for details.

Package Dimensions

unit: mm

3071-DIP64S

[LC7442]

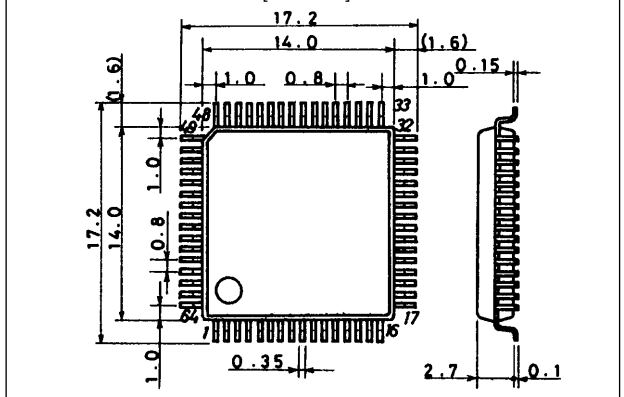


SANYO: DIP64S

unit: mm

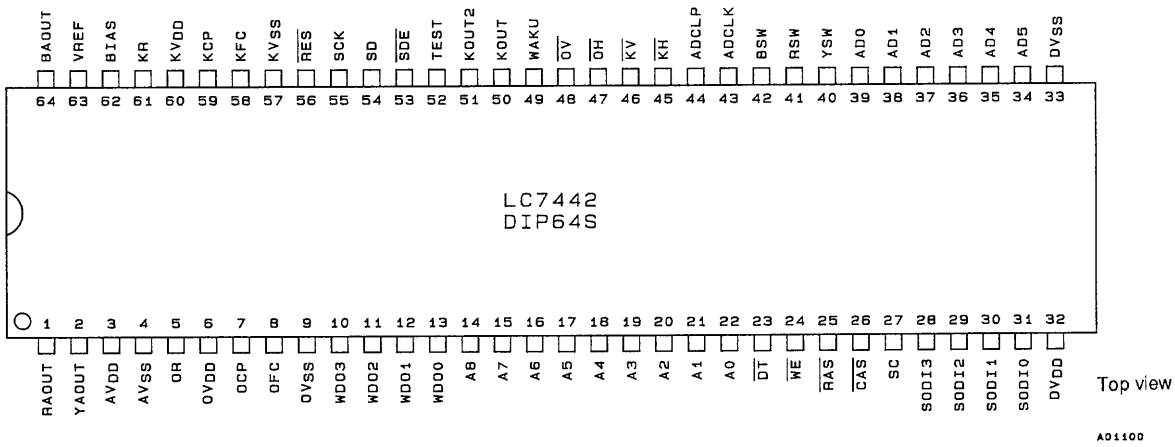
3159-QFP64E

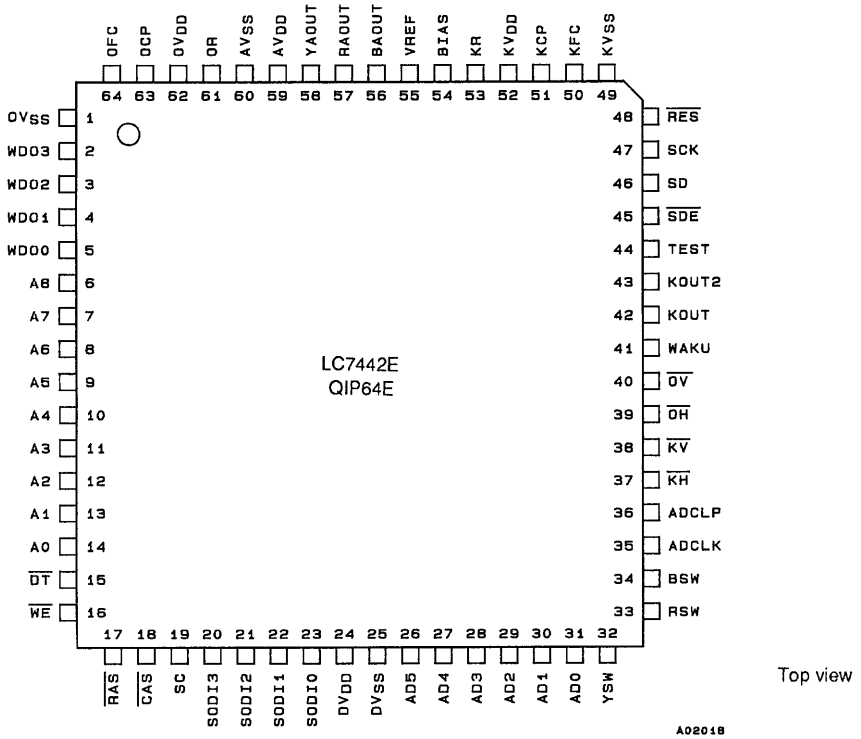
[LC7442E]



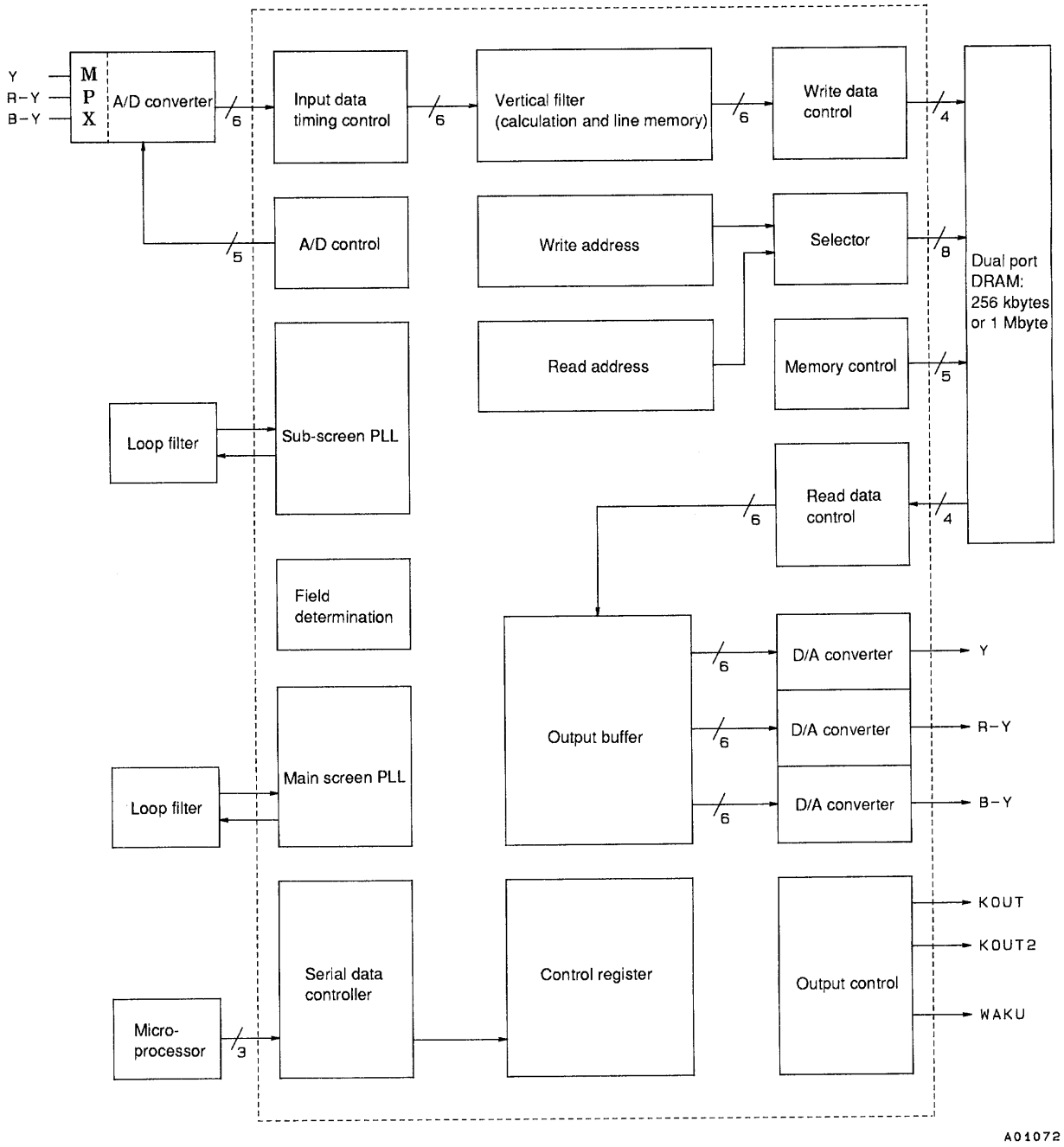
SANYO: QIP64E

Pin Assignments

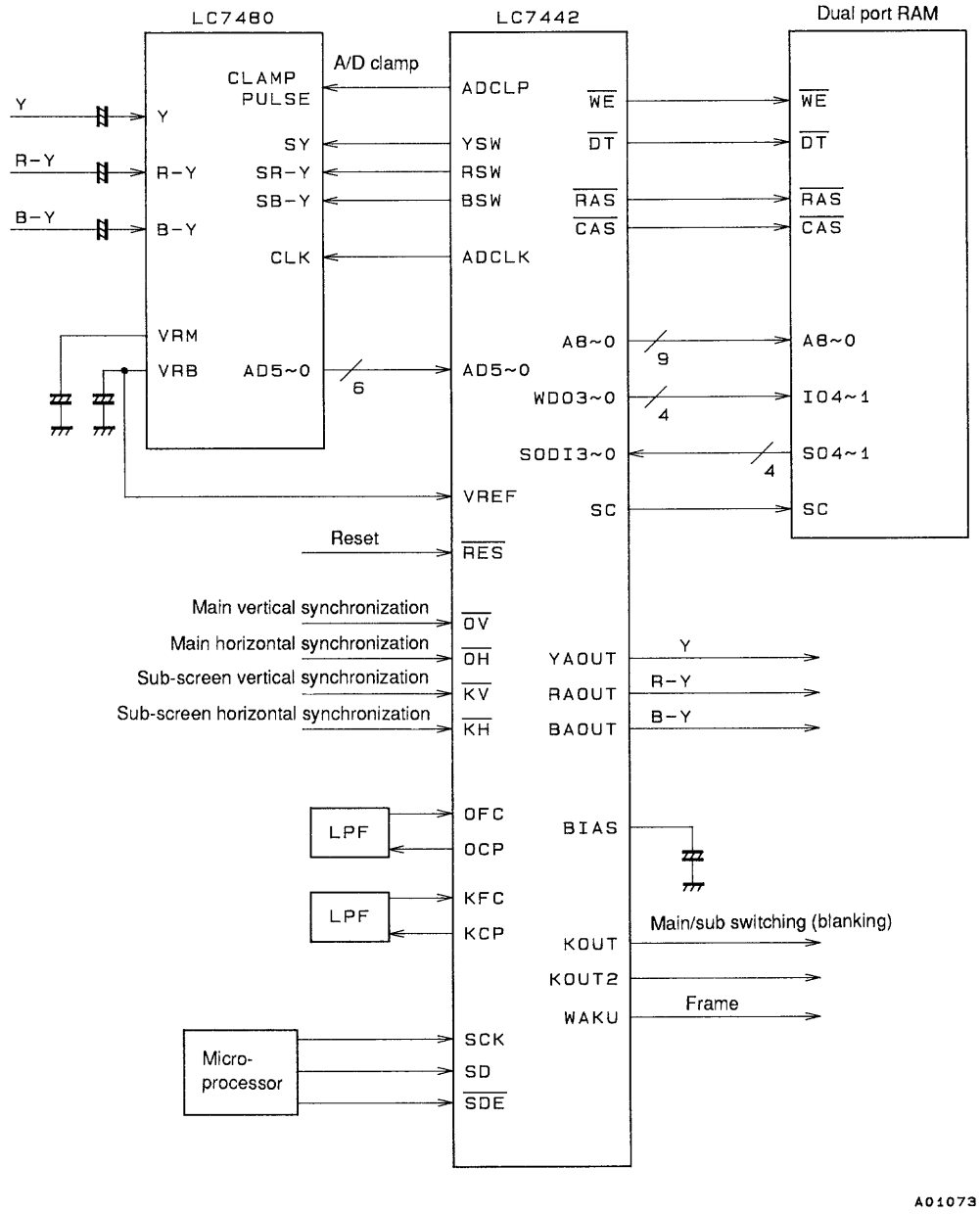




Block Diagram



Component-Type PIP System Structural Diagram (using the LC7442 and LC7480)



Note: See the separate “APPLICATION NOTE” document for details on applications.

Internal Control Registers

All functions are operated by inputting control register settings as serial port data.

Bit / Address	MSB 7	6	5	4	3	2	1	LSB 0	Functions
01H	SBY	STL	N/P	MUL	VDFS1	VDFS0	MOD1	MOD0	Operating mode
02H	FLD-B	FLD-A	MVS1	MVS0	KOUT-B	KOUT-A	FVP	FHP	Display mode
03H	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	Display position (V)
04H	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Display position (H)
05H	WK-B	WK-A	WKVR-B	WKVR-A	YWK5	YWK4	YWK3	YWK2	Frame color (Y), control
06H	PLL6	PLL5	PLL4	PLL3	RWK5	RWK4	RWK3	RWK2	PLL, frame color (R-Y)
07H	VWIPE	HWIPE	DWIPE	WPMOD	BWK5	BWK4	BWK3	BWK2	Wipe, frame color (B-Y)
08H	WVAJ1	WVAJ0	WHAJ1	WHAJ0	RVAJ1	RVAJ0	RHAJ1	RHAJ0	Display adjustment 1
09H	CLPAJ1	CLPAJ0	YCAJ1	YCAJ0	WKAJ1	WKAJ0	L	L	Display adjustment 2
0AH	$\overline{PP}$	BSE-A	BS5	BS4	BS3	BS2	BS1	BS0	Display area

Note: L: Enter data values of 0.

Operating Modes

Mode	[MOD1]	[MOD0]	Number of sub-screens	Display	Description
Two-screen frame	0	0	2 (A, B)	Frame	Has screens A and B
Two-screen field	0	1	2 (A, B)	Field	Has screens A and B
Three-screen field	1	0	3 (B)	Field	Uses screen B for 3 screens as a single block
Four-screen field	1	1	4 (B)	Field	Uses screen B for 4 screens as a single block

Notes: Field: The dynamic image is framed.
A and B screen overlapped display is not allowed (including horizontal overlap).

Screens A and B

Screen A: The sub-screen displayed at the location of its 4 corners. (specified by FVP and FHP)
Screen B: Sub-screen displayed at the location according to register data (specified by VP0 to VP7 and HP0 to HP7)

Function	Screen B	Screen A
Display on/off	o	o
Dynamic/static	Δ	Δ
Frame on/off	o	o
Frame color, fixed/data	o	o
Wipe*5	o	×
Display area*5	o	Δ*4

o : Can be controlled independently.
Δ : Can be controlled jointly.
× : Not supported.
Notes: 4: Controlled jointly with the B screen when BSE-A = 1.
5: Wipe and display area cannot be used at the same time.
6: An operation evaluation must be performed if the wipe function or the display area function is to be used.

Register Data Functions o: On, ×: Off

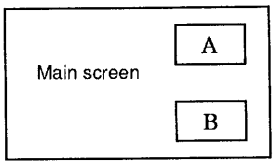
Address	Register	Data		Notes
		H	L	
01H	SBY	o	×	Standby mode (PLL circuits stopped)
	STL	o	×	Static screen (all writing stopped)
	N/P	NTSC	PAL	Mode selection
	MUL	o	×	Multi-mode specification*
	VDFS1, VDFS0	—	—	Vertical filter coefficient selection*
	MOD1,MOD0	—	—	Operating mode specification
02H	FLD–B, FLD–A	—	—	Field memory specification (in 2-screen field mode)
	MVS1, MVS0	—	—	Dynamic image specification (write field selection)
	KOUT–B, KOUT–A	o	×	Screen B/A display
	FVP, FHP	—	—	Four-corner fixed position specification
03H	VP7 to VP0	—	—	Screen B vertical position data
04H	HP7 to HP0	—	—	Screen B horizontal position data
05H	WK–B, WK–A	o	×	D/A converter frame for screens B and A
	WKVR–B, WKVR–A	Register data	Fixed data	D/A converter frame color selection for screens B and A
	YWK5 to YWK2	—	—	D/A converter frame color Y data
06H	PLL6 to PLL3	—	—	PLL divisor specification (aspect correction function)*
	RWK5 to RWK2	—	—	D/A converter frame color R-Y data
07H	V, H, D, WIPE	o	×	Wipe type selection
	WPMOD	Wipe	Display area	Wipe circuit function selection
	BWK5 to BWK2	—	—	D/A converter frame color B-Y data
08H	WVAJ1, WVAJ0	—	—	Write vertical adjustment
	WHAJ1, WHAJ0	—	—	Write horizontal adjustment
	RVAJ1, RVAJ0	—	—	Display vertical adjustment
	RHAJ1, RHAJ0	—	—	Display horizontal adjustment
09H	CLPAJ1, CLPAJ0	—	—	A/D clamp position adjustment
	YCAJ1, YCAJ0	—	—	Phase adjustment for C (R-Y, B-Y) with respect to Y*
	WKAJ1, WKAJ0	—	—	D/A converter frame position adjustment*
0AH	$\overline{PP}$	—	—	Passing processing (normally set to H: see the APPLICATION NOTE)*
	BSE-A	o	×	The A screen is linked to the B screen display area
	BS5 to BS0	—	—	Display area (blanking) size specification

Note: Usage notes may apply for certain setting values. See the separate “APPLICATION NOTE” document for details.

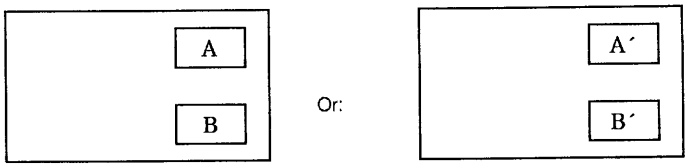
Function Descriptions

This section describes the functions supported when 1 Mbyte of external memory is used.

• 2-screen frame mode*7, *9

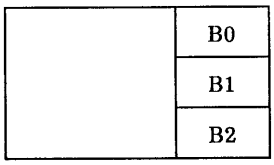


• 2-screen field mode*8, *9



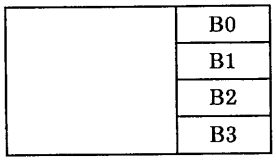
Switching between A and A' and between B and B' can be performed independently.

• 3-screen field mode*8, *9



The 3 screens are handled as a single block, and the functions are the same as those for the B screen.

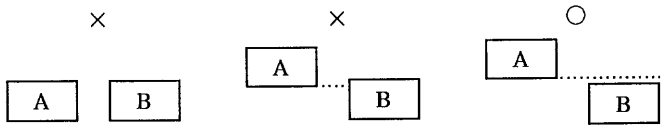
• 4-screen field mode*8, *9, *10



The 4 screens are handled as a single block, and the functions are the same as those for the B screen.

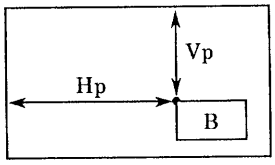
Notes: 7: Frame display
8: Frame display for dynamic images only (However, an overrun phenomenon occurs.)
9: Two sub-screens cannot be displayed so that they share a scan line.

Examples:



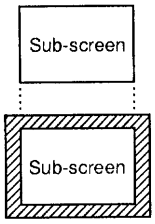
10: The maximum vertical direction for the display area is 75%.

• Display position of the B screen



Vp: Data in register VP0 to VP7
Hp: Data in register HP0 to HP7

• Frame control



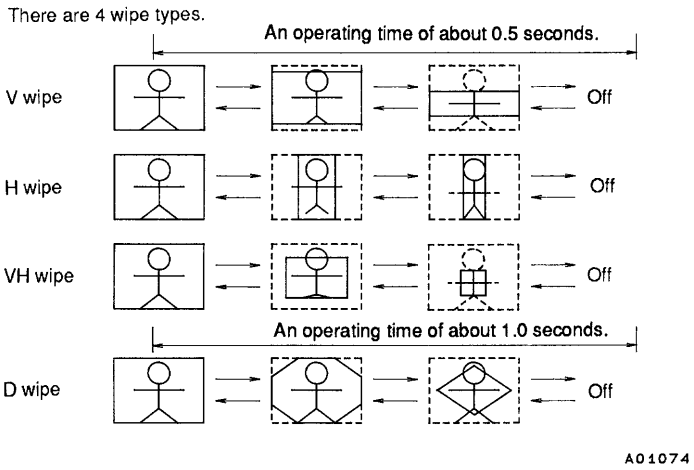
Frame on/off: Registers WK-B and WK-A

Frame color: Registers WKVR-B and WKVR-A
Fixed color: white

Arbitrary color: Specified by register data

[YWK5 to YWK2]
[RWK5 to RWK2]
[BWK5 to BWK2]

• Wipe function



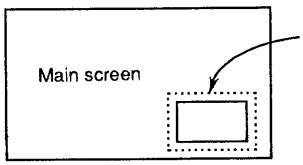
Note: The wipe function can only be used on the B screen.

• Display area

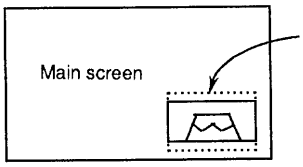
This function allows display in an intermediate state of the wipe operation.

<Application Example>

— Reducing the size of the sub-screen to reduce the disruption of the main screen



— Aspect conversion

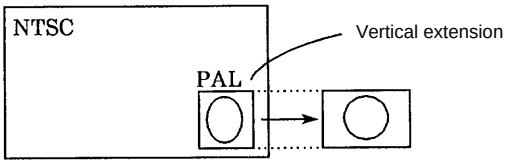


• Aspect correction

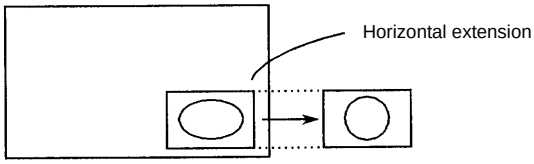
Horizontal direction compression or expansion is effected by changing the PLL oscillator frequency. There are limitations on the values of this setting, so be sure to refer to the separate “APPLICATION NOTE” document for details.

<Application Example>

— When multi-mode is used



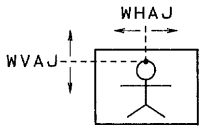
— 16:9 aspect ratio tube



• Fine adjustment of setting values

This function allows the number of external components (such as delay circuits) to be reduced.

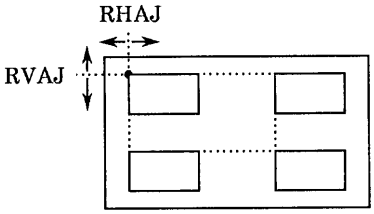
— Position of the image within the sub-screen



WVAJ: 4 steps in 1H increments
WHAJ: 4 steps in 267 ns increments

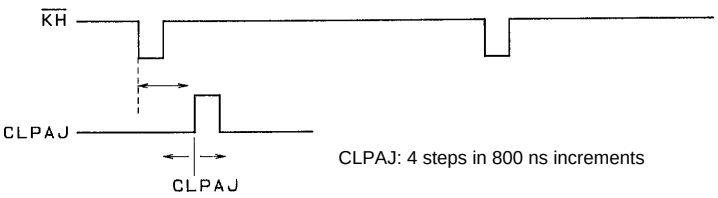
A01075

— Display position



RVAJ: 4 steps in 2H increments
RHAJ: 4 steps in 246 ns increments

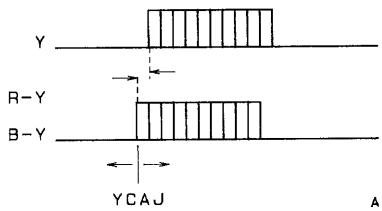
— Clamp pulse position



CLPAJ: 4 steps in 800 ns increments

A01076

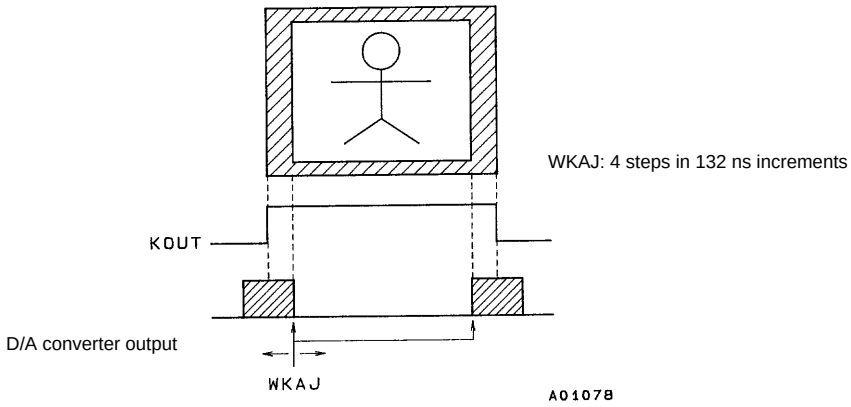
— Phase difference between the Y and R-Y/B-Y D/A converter outputs



YCAJ: 4 steps in 267 ns increments

A01077

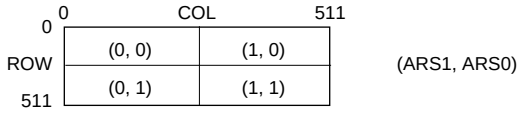
— Vertical frame horizontal thickness



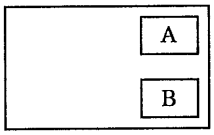
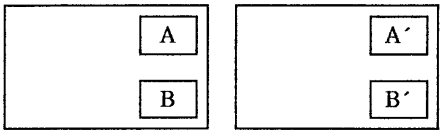
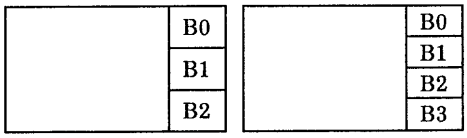
Note: When [YCAJ1,0] = 00, use care when setting [WKAJ1,0] to values other than 00, since incorrect color data may appear at the right edge.

Memory Map

The 1 Mbyte VRAM is divided into 4 fields.



Read Selection

Mode		ARS1	ARS0	Screen state
2-screen frame		Automatic switching by the field determination circuit	Automatic switching based on the position of the A and B screens	
2-screen field		A screen = FLD-A B screen = FLD-B	As above	
3-, 4-screen field (automatic switching)	B0*	0	0	
	B1*	0	1	
	B2*	1	0	
	B3*	1	1	

* The order B0 to B3 is fixed.

Write Selection

Dynamic image display is controlled by setting MVS0 and MVS1.

Mode	ARS1	ARS0
2-screen frame	Automatic switching by the field determination circuit	[MVS0]
2-, 3-, 4-screen field	[MVS1]	[MVS0]

Limitations when a 256 kbit Memory is Used

- 1-screen display

  The following control registers have fixed values.

[MOD1] = L
[MOD0] = H
} 2-screen filed mode

[FLD-B] = L
[FLD-A] = L

KOUT-B and KOUT-A cannot be high at the same time (only 1 screen can be displayed)

- Dynamic image display

  The following control registers are taken as the display setting.

[KOUT-B]	[KOUT-A]	[MVS1]	[MVS0]	Description
L	L			No sub-screen
L	H	L	L	Screen A is displayed
H	L	L	H	Screen B is displayed
H	H			Illegal combination

- Control register table

  Control register table for 256 kbyte systems.

Address \ Bit	MSB 7	6	5	4	3	2	1	LSB 0	Description
01H	SBY	STL	N/P	L	VDFS1	VDFS0	L	H	Active mode
02H	L	L	L	MVS0	KOUT-B	KOUT-A	FVP	FHP	Display mode

See item “Dynamic image display” above.

  Registers starting at address 03H function the same as when 1 Mbit of memory is used.

- Multi-mode systems

  The multi-mode function cannot be used with 256 kbit VRAM since V-dancing occurs in dynamic images.

Notes on multi-mode (NTSC-PAL)

- External memory

  Multi-mode can only be used when 1M of external memory is provided.

- Operating mode

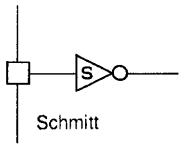
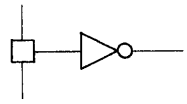
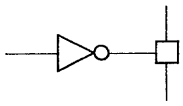
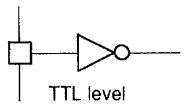
  Since vertical dancing occurs in moving images in modes other than two-screen frame mode, this can only be used with static images.

  When the main screen is NTSC and the subscreen is PAL, images will be expanded vertically. As a result, images may go offscreen in the 3 and 4 screen field modes.

- Vertical compression ratio

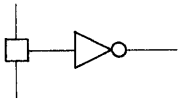
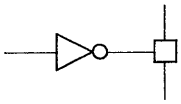
  Since the number of scan lines in NTSC and PAL differ, the ratios differ by 1/3 in accordance with the ratio of the number of scan lines.

Pin Functions

Pin No. QIP	Pin No. DIP	Signal	I/O	Connection	Function	Circuit type
40	48	$\overline{OV}$	I	LA7403 or a sync separator IC	Main screen vertical sync signal (negative polarity)	
39	47	$\overline{OH}$	I		Main screen horizontal sync signal (negative polarity)	
38	46	$\overline{KV}$	I		Sub-screen vertical sync signal (negative polarity)	
37	45	$\overline{KH}$	I		Sub-screen horizontal sync signal (negative polarity)	
47	55	SCK	I	Microprocessor	Serial clock (Serial control)	
46	54	SD	I		Serial data (Serial control)	
45	53	$\overline{SDE}$	I		Enable (Serial control)	
48	56	$\overline{RES}$	I	Initialization circuit	Reset	
44	52	TEST	I	V_{SS}	Test (Connect to V_{SS} in normal operation)	
2	10	WDO3	O	Memory	Memory write data output	
3	11	WDO2	O	Memory		
4	12	WDO1	O	Memory		
5	13	WDO0	O	Memory		
6	14	A8	O	Memory	MSB — Address (A8 is left open when a 256 kbyte memory is used)	
7	15	A7	O	Memory		
8	16	A6	O	Memory		
9	17	A5	O	Memory		
10	18	A4	O	Memory		
11	19	A3	O	Memory		
12	20	A2	O	Memory		
13	21	A1	O	Memory		
14	22	A0	O	Memory	LSB	
15	23	$\overline{DT}$	O	Memory	Control signals	
16	24	$\overline{WE}$	O	Memory		
17	25	$\overline{RAS}$	O	Memory		
18	26	$\overline{CAS}$	O	Memory		
19	27	SC	O	Memory		
20	28	SODI3	I	Memory	Memory read data	
21	29	SODI2	I	Memory		
22	30	SODI1	I	Memory		
23	31	SODI0	I	Memory		

Continued on next page.

Continued from preceding page.

Pin No. QIP	Pin No. DIP	Signal	I/O	Connection	Function	Circuit type
26	34	AD5	I	LC7480	MSB — Input of A-to-D converted digital data	 A01080
27	35	AD4	I	LC7480		
28	36	AD3	I	LC7480		
29	37	AD2	I	LC7480		
30	38	AD1	I	LC7480		
31	39	AD0	I	LC7480	LSB	
32	40	YSW	O	LC7480	Y signal selection — MPX switching signals	 A01081
33	41	RSW	O	LC7480	R-Y signal selection	
34	42	BSW	O	LC7480	B-Y signal selection	
35	43	ADCLK	O	LC7480	Sampling clock	
36	44	ADCLP	O	LC7480	Clamp pulse	
41	49	WAKU	O	LA7403	Frame pulse output	
42	50	KOUT	O	LA7403	Main/sub switching signal (blanking)	
43	51	KOUT2	O	—	Control signal	
24	32	DV_{DD}			Digital power supply (for logic circuits and the line memory)	
25	33	DV_{SS}				
58	2	YAOUT	O	LA7403	Y signal — D/A output	
57	1	RAOUT	O	LA7403	R-Y signal	
56	64	BAOUT	O	LA7403	B-Y signal	
55	63	VREF	I	LC7480	D/A connection	
54	62	BIAS	—	Capacitor		
59	3	AV_{DD}			D/A analog power supply	
60	4	AV_{SS}				
63	7	OCP	O	LPF	Charge pump output — Main screen synchronization VCO	
64	8	OFC	I	LPF	Oscillator control voltage input	
61	5	OR	—	Resistor	Oscillator range resistor	
62	6	OV_{DD}			Power supply	
1	9	OV_{SS}				
51	59	KCP	O	LPF	Charge pump output — Sub-screen synchronization VCO	
50	58	KFC	I	LPF	Oscillator control voltage input	
53	61	KR	—	Resistor	Oscillator range resistor	
52	60	KV_{DD}			Power supply	
49	57	KV_{SS}				

Specifications

Absolute Maximum Ratings at Ta = 25 ±2°C, V_{SS} = 0 V

Paramater	Symbol	Ratings	Unit
Maximum supply voltage	V_{DD} max	–0.3 to +7.0	V
Maximum input voltage	V_{IN} max	–0.3 to V_{DD} + 0.3	V
Maximum output voltage	V_{OUT} max	–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd_1 max (DIP version)	500	mW
	Pd_2 max (QFP version)	350	mW
Operating temperature	Topr	–10 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Allowable Operating Ranges at Ta = –10 to +70°C, V_{SS} = 0 V

Paramater	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply voltage	V_{DD}		4.5	5.0	5.5	V
Input high level voltage	V_{IH1}	CMOS levels	0.7 V_{DD}			V
	V_{IH2}	TTL levels	2.2			V
Input low level voltage	V_{IL1}	CMOS levels			0.3 V_{DD}	V
	V_{IL2}	TTL levels			0.8	V
Reference voltage	V_{REF}	V_{REF} pin	3.4	0.8 V_{DD}	V_{DD}	V

Electrical Characteristics at Ta = 25 ±2°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

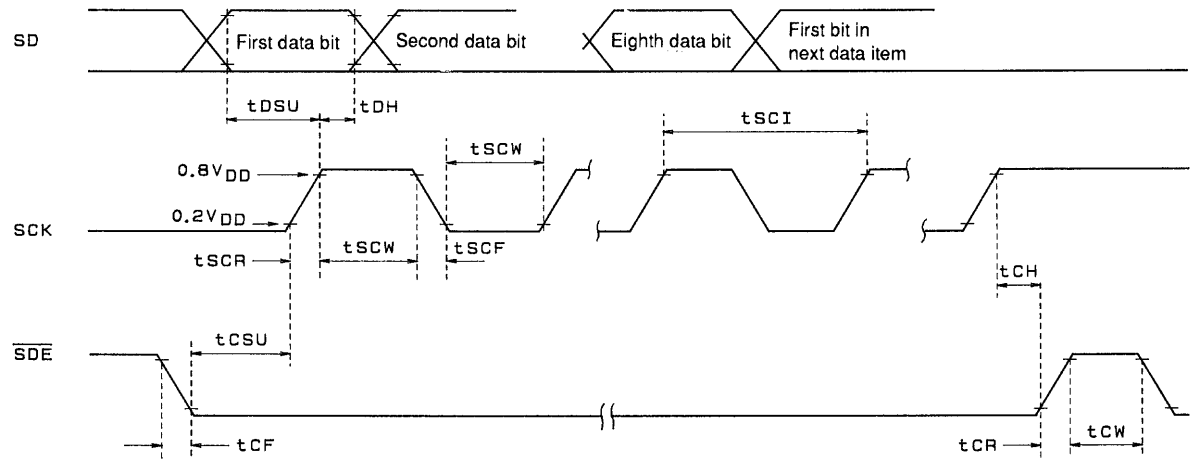
Paramater	Symbol	Conditions		Ratings			Unit
				min	typ	max	
Output high level voltage	V_{OH1}	I_{OH} = –1 mA; Pins KCP and OCP		V_{DD} – 1			V
	V_{OH2}	I_{OH} = –1 mA; Pins other than KCP and OCP		V_{DD} – 1			V
Output low level voltage	V_{OL1}	I_{OL} = 1 mA; Pins KCP and OCP				1.0	V
	V_{OL2}	I_{OL} = 2 mA; Pins other than KCP and OCP				0.4	V
Operating current dissipation	$I_{DD}D$	$\overline{RES}$: H	The DV_{SS} pin		20		mA
	$I_{DD}A$	$\overline{OV}$, $\overline{KV}$: 60 Hz	The AV_{SS} pin		21		mA
	$I_{DD}O$	$\overline{OH}$, $\overline{KH}$: 15 kHz	The OV_{SS} pin		2		mA
	$I_{DD}K$	A/D data: 1010 Output unloaded	The KV_{SS} pin		2		mA
Static current dissipation	$I_{DD}S$	$\overline{RES}$: L, Input pin DC, output unloaded				10	µA
Input leakage current	I_{LK}	V_I = V_{DD}, V_{SS}		–1		1	µA
Output leakage current	I_{OZ}	V_I = V_{DD}, V_{SS}; Pins KCP and OCP		–1		1	µA
D/A output resistance	R_{DA}				150		Ω

Note: There are 4 power supply pin systems.
The power supplies are DV_{DD}, AV_{DD}, OV_{DD}, and KV_{DD}, and they must be identical. Descriptions are for V_{DD}.
The grounds are DV_{SS}, AV_{SS}, OV_{SS} and KV_{SS}, and they must be identical. Descriptions are for V_{SS}.

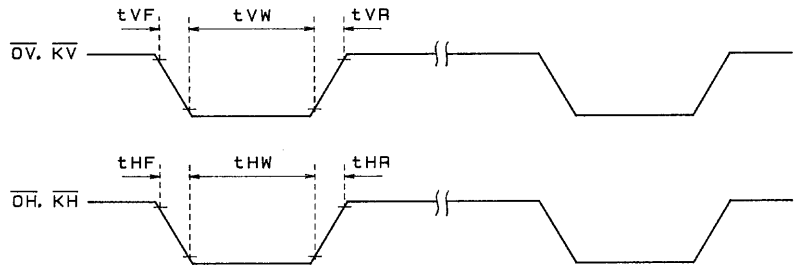
Switching Characteristics at Ta = 25 ±2°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Paramater			Symbol	Ratings			Unit
				min	typ	max	
Vertical sync signals		Pulse width	t_{VW}	1			µs
		Rise time	t_{VR}			50	ns
		Fall time	t_{VF}			50	ns
Horizontal sync signals		Pulse width	t_{HW}	1			µs
		Rise time	t_{HR}			50	ns
		Fall time	t_{HF}			50	ns
Serial data interface	Serial clock	Pulse width	t_{SCW}	200			ns
		Rise time	t_{SCR}	50			ns
		Fall time	t_{SCF}	50			ns
		Data setup	t_{DSU}	100			ns
		Data hold	t_{DH}	30			ns
		Interval	t_{SCI}	2			µs
	Control	Pulse width	t_{CW}	200			ns
		Rise time	t_{CR}	50			ns
		Fall time	t_{CF}	50			ns
		Setup	t_{CSU}	200			ns
		Hold	t_{CH}	200			ns

Serial Data



Synchonization Signals



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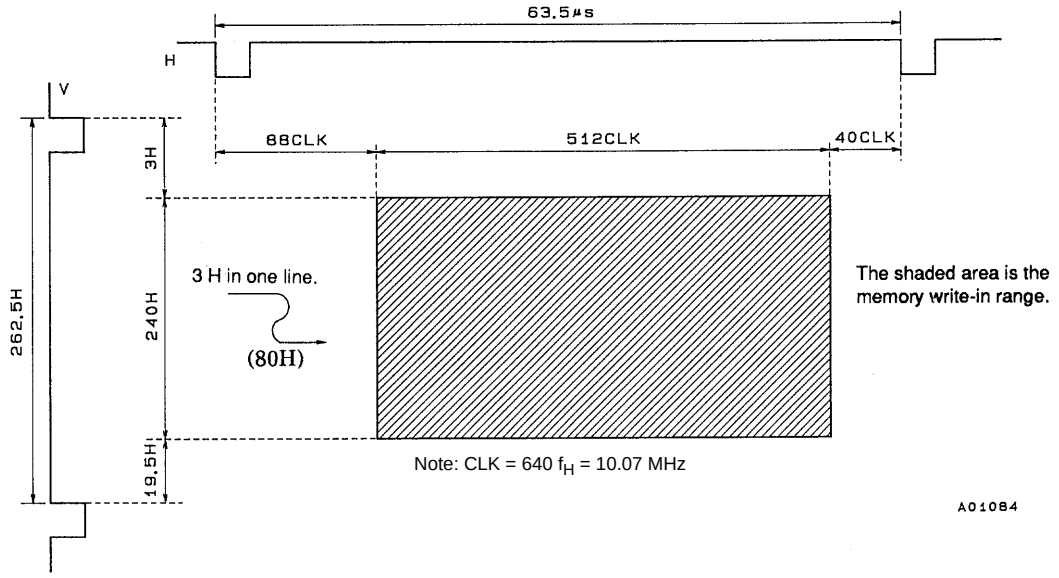
Sub-Screen Digital Processing Specifications

Parameter			NTSC (f_H = 15734 Hz)	PAL (f_H = 15625 Hz)
Sampling	Order		Y, R - Y, Y, B - Y, Y, -, Y -, · · · · ·	
	Frequency	f_T (MHz)	640 f_H	
			10.070	10.000
		Only Y	320 f_H	
		f_{TY}	5.035	5.000
		Only R-Y	80 f_H	
		f_{TR}	1.258	1.250
		Only B-Y	80 f_H	
		f_{TB}	1.258	1.250
Number of quantization bits			6 bits	
D/A converter clock (MHz)		Y signal	960 f_H	
		f_{CY}	15.105	15.000
		R-Y signal	240 f_H	
		f_{CR}	3.776	3.750
		B-Y signal	240 f_H	
		f_{CB}	3.776	3.750
Write	Number of dots (horizontal)		384	
		Only Y	256	
		Only R-Y	64	
		Only B-Y	64	
	Vertical H count		80	84
Read display	Number of dots (horizontal)		370	
		Only Y	250	
		Only R-Y	60	
		Only B-Y	60	
	Vertical H count		75	83

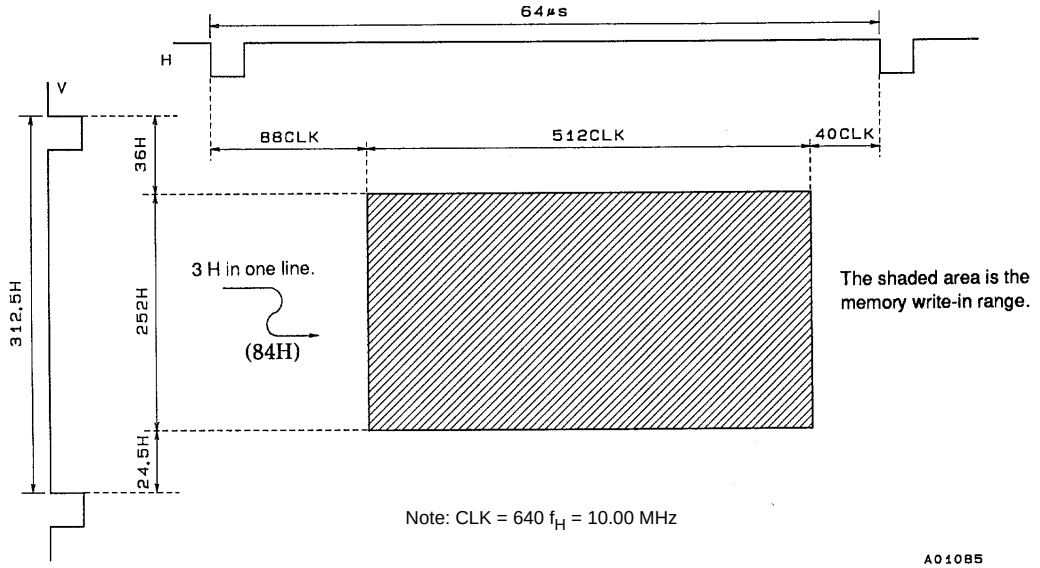
Memory Write Range

When the display fine adjustment register (WVAJ1, 0, WHAJ1, 0) is 0000.

<NTSC>



<PAL>

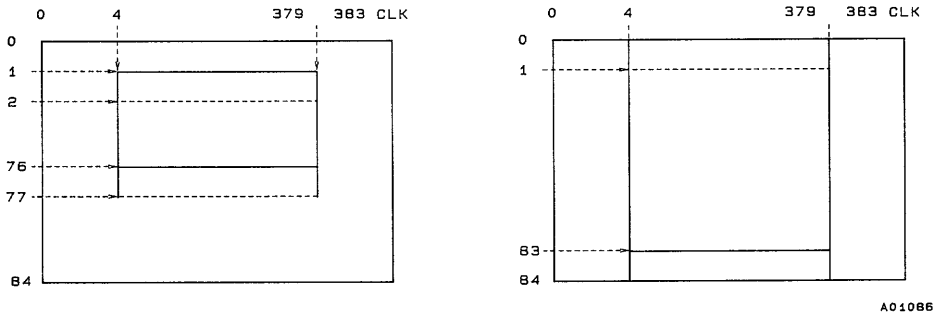


Memory Read Range

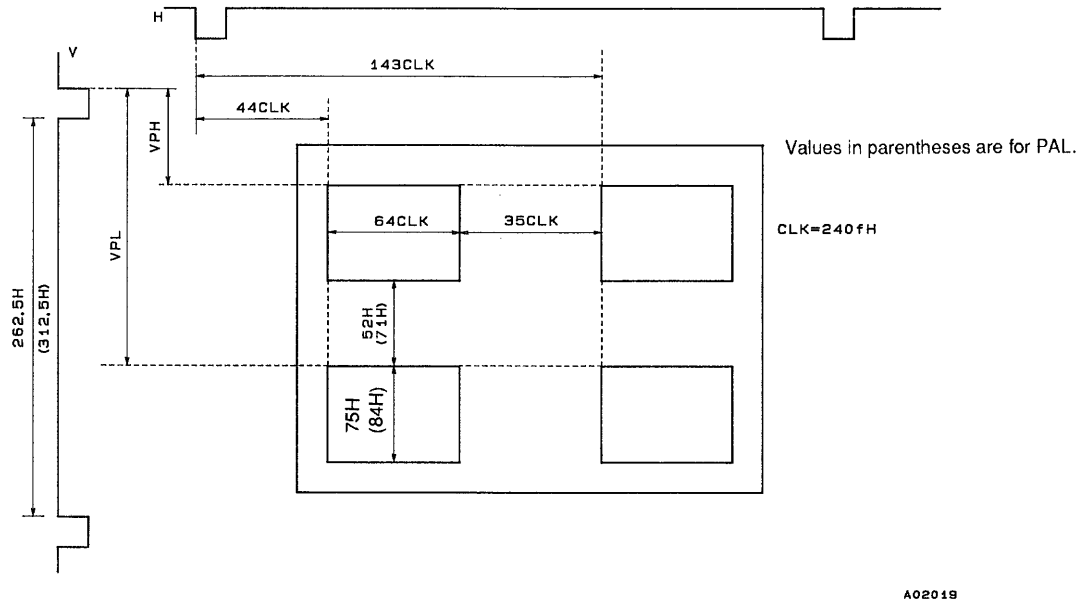
Sub-Screen Display Position (for 4 corner display)

<NTSC>

<PAL>



When the display fine adjustment register (RVAJ1, 0, RHAJ1, 0) is 0000.

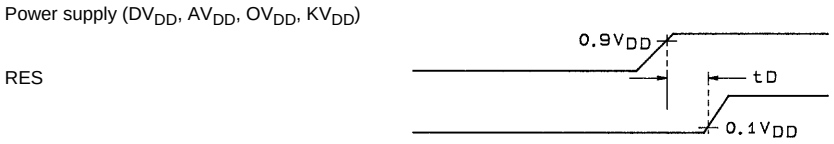


		VPH		VPL	
N/P register		H	L	H	L
MUL register	H	48H	43H	198H	158H
	L	43H	48H	158H	198H

Initial Settings

- $\overline{\text{RES}}$ pin: reset

  This pin must be held low when power is first applied.



t_D: At least a few microseconds.

- Internal control registers

  The table below lists the states of the registers following a reset.

Register	State
SBY	H
KOUT–A, KOUT–B	L
PLL6	L
PLL5	L
PLL4	H
PLL3	H

Notes: H: V_{DD} level
L: V_{SS} level

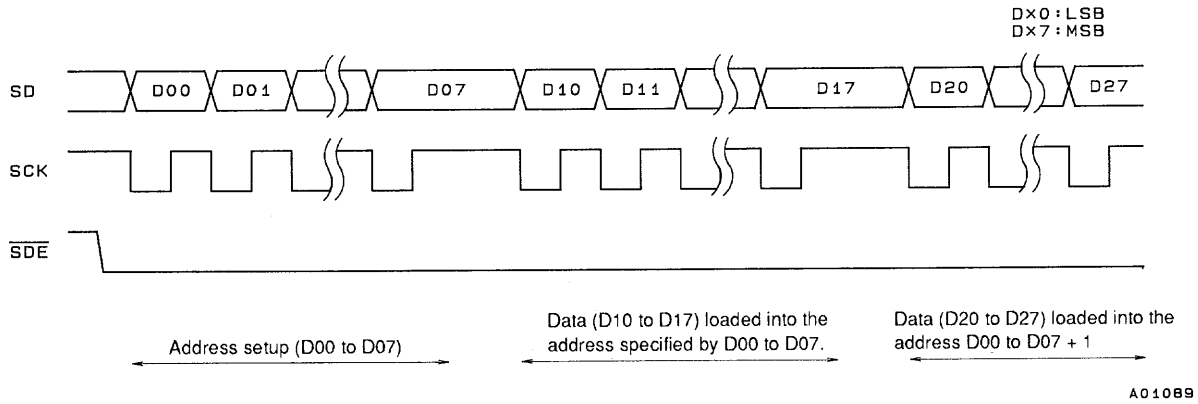
These states are set even if SBY = H.

Since all system operations are stopped at this time, the data held in external memory cannot be retained.

Registers other than the above are not initialized by a reset.

Serial Data Interface

- Serial input format



The first 8 bits of data following $\overline{\text{SDE}}$ going low specify an address, and the next 8 bits are register data for that address. The last 8 bits of data are transferred to the incremented address.

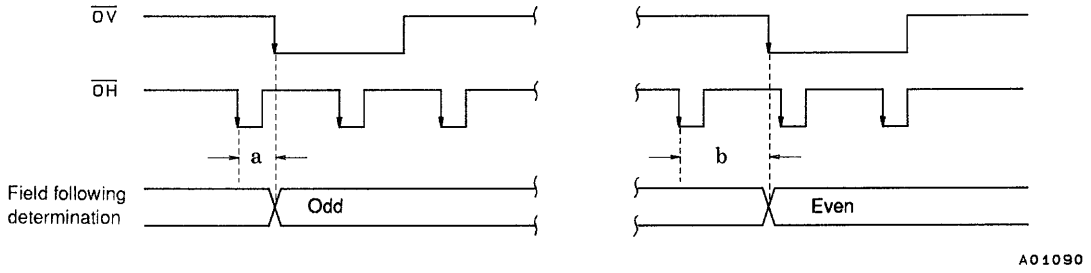
The address can be re-specified after switching $\overline{\text{SDE}}$ from low to high to low again (⌐¬).

Since the PLL clock is not used for serial data transfer, data transfers can be performed when SBY is high. However, data cannot be transferred to registers that are initialized by a reset.

Since there is no way to confirm that the transferred data was latched correctly, we recommend refreshing this data periodically.

Even/Odd Field Determination Circuit

Since this determination is based on the phase difference between the falling edges of OV and OH, these must be input with the following timing.



Note: $\overline{KV}$ and $\overline{KH}$ are similar to the above.

a = 0.02 to 0.40 H

b = 0.60 to 0.98 H

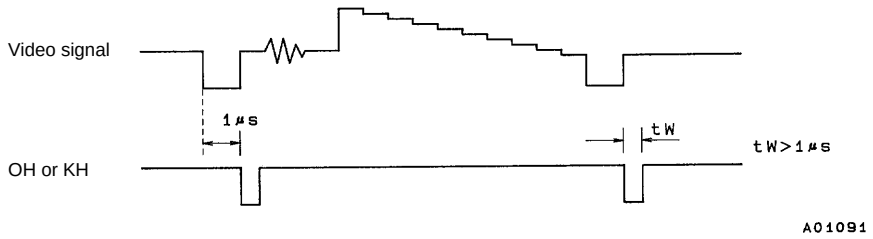
However, if the PLL aspect correction function is used, these values will differ.

See the separate “APPLICATION NOTE” document for details.

The horizontal synchronization signal equalizing pulse must be removed.

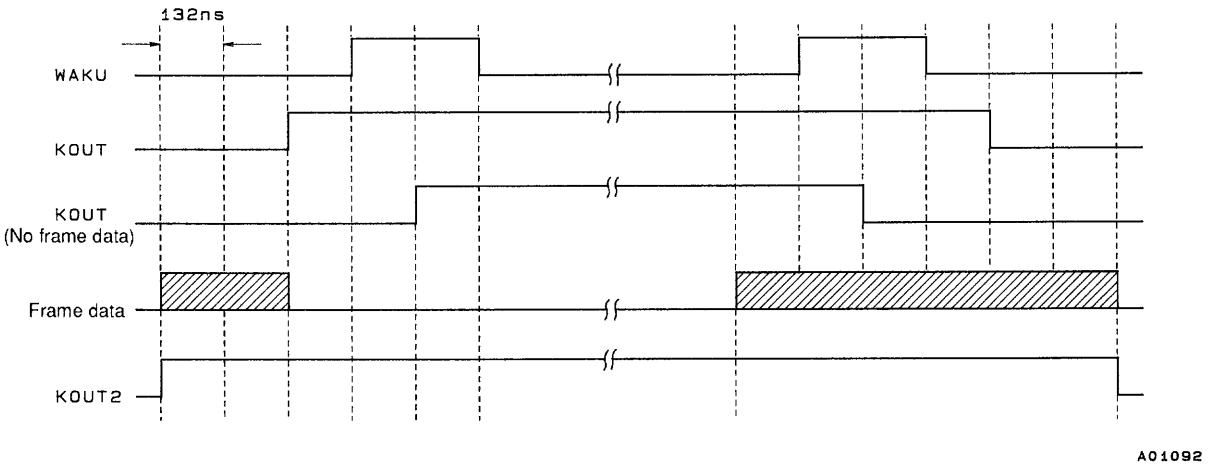
Synchronization Signals

- The LC7442 $\overline{OH}$ and $\overline{KH}$ pin inputs are set assuming that $\overline{OH}$ (and $\overline{KH}$) are delayed 1 µs from the video signal horizontal synchronization signal.



- Since noise on the synchronization signal input pins ($\overline{KV}$, $\overline{KH}$, $\overline{OV}$ and $\overline{OH}$) results in image distortion, care must be used in wiring these signals.
- Since the sub-screen will be distorted if the synchronization signals are unstable, we recommend turning off display in such cases.

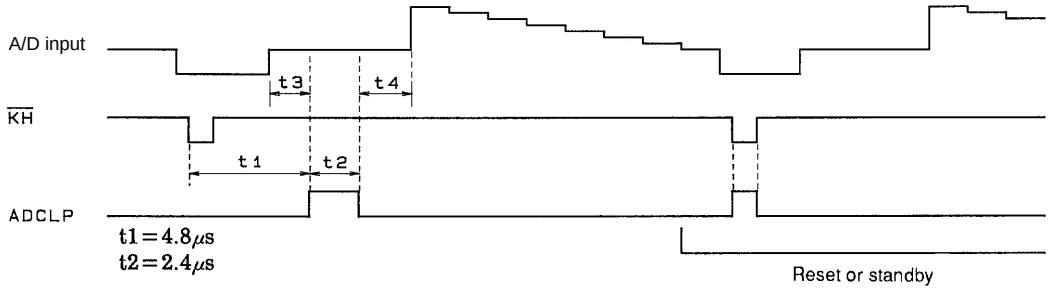
Sub-Screen Output Timing



Notes: a: The frame data position shown here is for the timing when registers WKAJ0 and 1 are 00.
b: Whether frame data is present or not is switched by the size of the KOUT pulse.

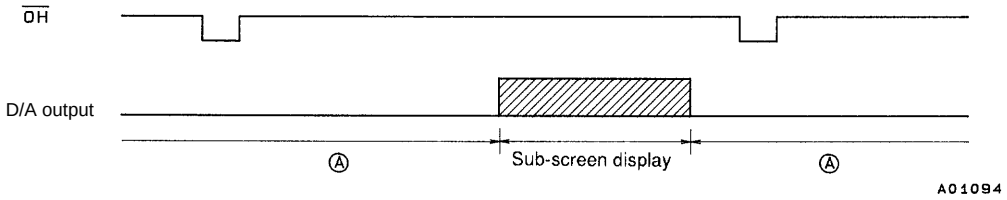
Clamp Pulse

- A/D converter clamp
  Since clamp pulses are output with the timing shown in the figure below, it is setup to fall within the pedestal range. On reset and during standby, the $\overline{KH}$ signal goes to a positive polarity, and is output as such.



Notes: 1: The conditions t3 > 0 µs and t4 > 0.5 µs must be met.
2: The value of 4.8 µs for t1 is the value when registers CLPAJ0 and 1 are 00.

- D/A converter clamp



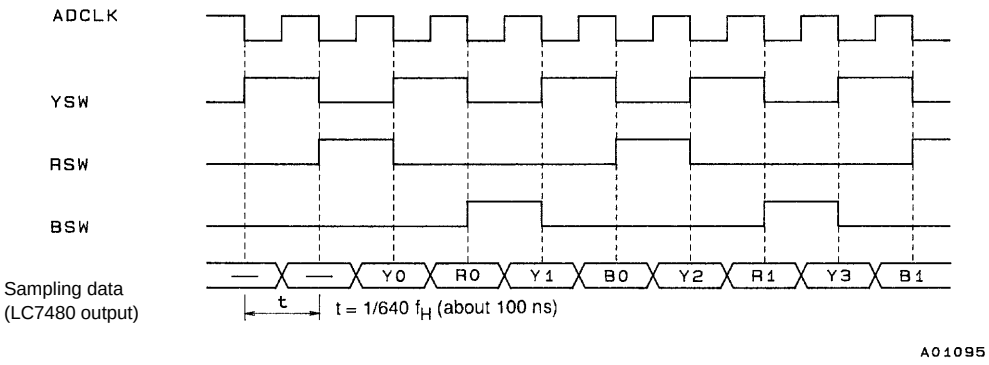
Digital data in the A region:

	MSB					LSB
Y D/A:	0	0	0	0	0	0
R-Y D/A:	1	0	0	0	0	0
B-Y D/A:	1	0	0	0	0	0

Clamping is applied by the main screen horizontal synchronization signal.

External Control Output Timing

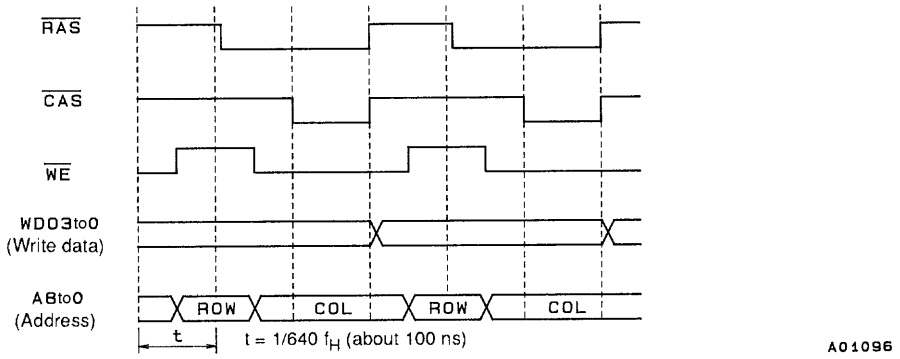
- Relationship with the LC7480 A/D converter



Note: Since this circuit operates at the high speeds shown in this figure, care is required to keep leads as short as possible in the wiring used in this circuit.

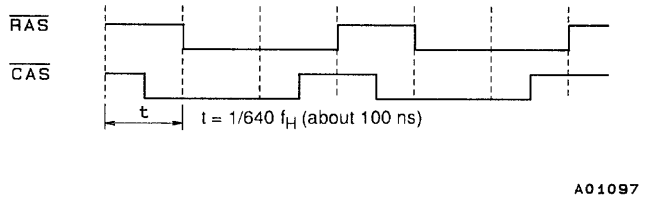
- Video memory relationships
  This value of t is for situations when aspect correction is not applied.

— Data write

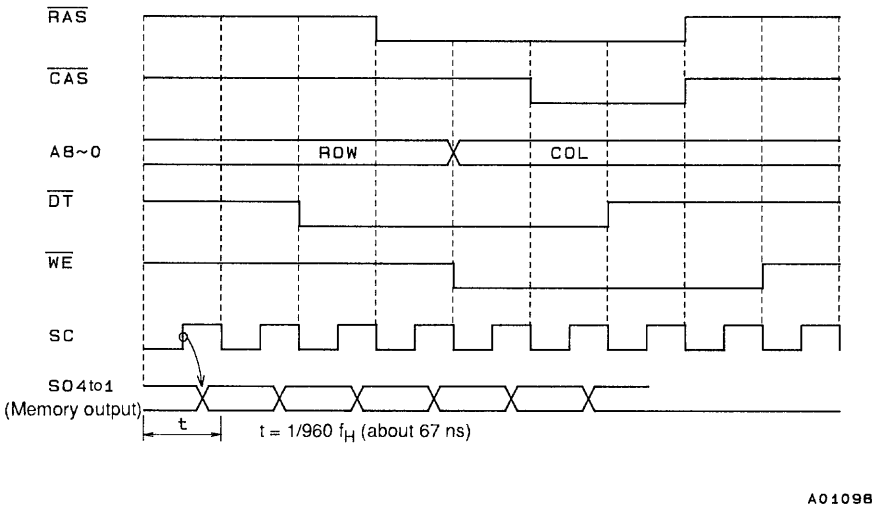


Note: Since this circuit operates at the high speeds shown in this figure, care is required to keep leads as short as possible in the wiring used in this circuit.

— Refresh
A $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle is used.



— Data transfer → serial read



Note: Since this function operates at the high speeds shown in the figure, care is required to keep the leads as short as possible in the circuit wiring.
Caution: Contact your Sanyo representative before determining the memory to be used.

P. 3 Block Diagram

1 A/D converter
2 Loop filter
3 Loop filter
4 Micro-processor
5 Input data timing control
6 A/D control
7 Sub-screen PLL
8 Field determination
9 Main screen PLL
10 Serial data controller
11 Vertical filter (calculation and line memory)
12 Write address
13 Read address
14 Output buffer
15 Control register
16 Write data control
17 Selector
18 Memory control
19 Read data control
20,21,22
D/A converter D/A converter D/A converter
23 Output control
24 Dual port DRAM: 256 kbytes or 1 Mbyte

P. 4 Component-Type PIP System Structural Diagram

1 A/D clamp
2 Reset
3 Main vertical synchronization
4 Main horizontal synchronization
5 Sub-screen vertical synchronization
6 Sub-screen horizontal synchronization
7 Micro-processor
8 Dual port RAM
9 Main/sub switching (blanking)
10 Frame

P. 7 Function Descriptions

(1) Main screen
(2) Or:

P. 8 Frame control

(6) 1 Sub-screen Sub-screen
(7) 1 There are 4 wipe types.
2 An operating time of about 1.0 seconds.
3 V wipe
4 H wipe
5 VH wipe
6 D wipe
7 Off Off Off Off