622 MHz 4:32 Demultiplexer GD16333

Preliminary

General Description

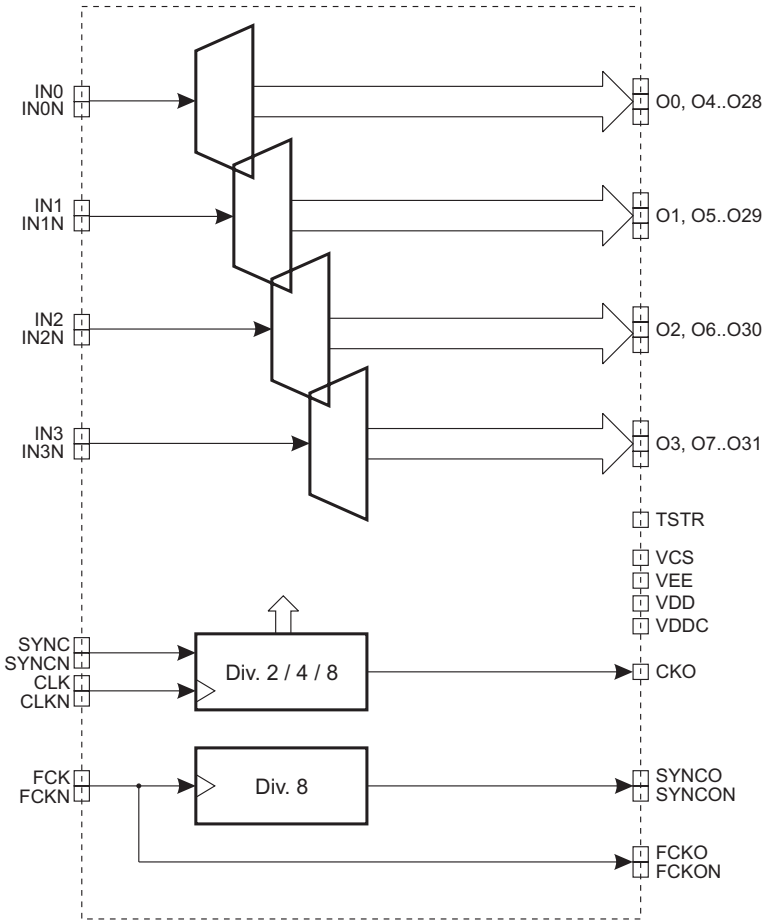
The GD16333 is 4:32 Demultiplexer, intended for use with GD16544, an STM-64 receiver and 1:16 Demultiplexer or in DSP applications with fast ADC's.

The GD16333 consists of:
- four 1:8 demultiplexers
- a clock generator circuit
- a synchronisation circuit.

The synchronisation circuit enables a parallel coupling of several devices. This is done with a master clock divider, which distributes a synchronisation signal to the parallel devices.

The GD16333 is provided in a 100 pin power enhanced plastic package.

The chip is designed for operation between -5 °C and +85 °C (case temperature).



Features

- Clock frequency to 622 MHz.
- 4:32 DeMUX obtained by four 1:8 DeMUX.
- High-speed differential inputs, CML/PECL level.
- Data outputs are CMOS level.
- 100 pin QFP (14 x 20 mm) power enhanced plastic package.
- Power consumption: 1 W typical.
- Synchronisation of parallel devices for wider bus widths.
- 5 V single supply operation.

Applications

- Tele Communication:
  - STM-64
    STM-16
  - OC-192
    OC-48
- DSP
  - High speed ADC interface

Functional Details

Synchronisation

The GD16333 provides a synchronisation block that allows parallel expansion of devices for wider data width. When this is required only one synchronisation block is used as a master controller, which drives the synchronisation input of all parallel DeMUX devices.

The synchronisation block provides a clock output (FCKO) and a SYNCO signal (which is a 1/8 clock signal) timed by the FCKO output. These signals are then daisy-chained to the CLK and SYNC inputs of all the DeMUX devices. This solution provides a fully synchronised parallel demultiplexer structure, where all DeMUX data ports samples data in the same clock cycle.

The data inputs (FCK, CLK and SYNC) allow for either CML or PECL termination. Termination resistors must be provided externally (i.e. 50 Ω to V_{DD} if CML or 50 Ω to V_{DD} -2 V if PECL). The FCKO and SYNCO outputs are both open drain outputs accommodating the CLK and SYNC inputs in CML configuration.

There are two ways to connect the master clock, provided at the input to the GD16333's from the upstream device, with different timing constrains. Using the clock output (FCKO) from the synchronisation block, will give a good timing condition for the SYNC signal path, with respect to the clock. But it will put constrains on the timing at the data inputs, since the synchronisation block will add a delay to the master clock, with respect to the data coming from the upstream device (refer to Figure 1).

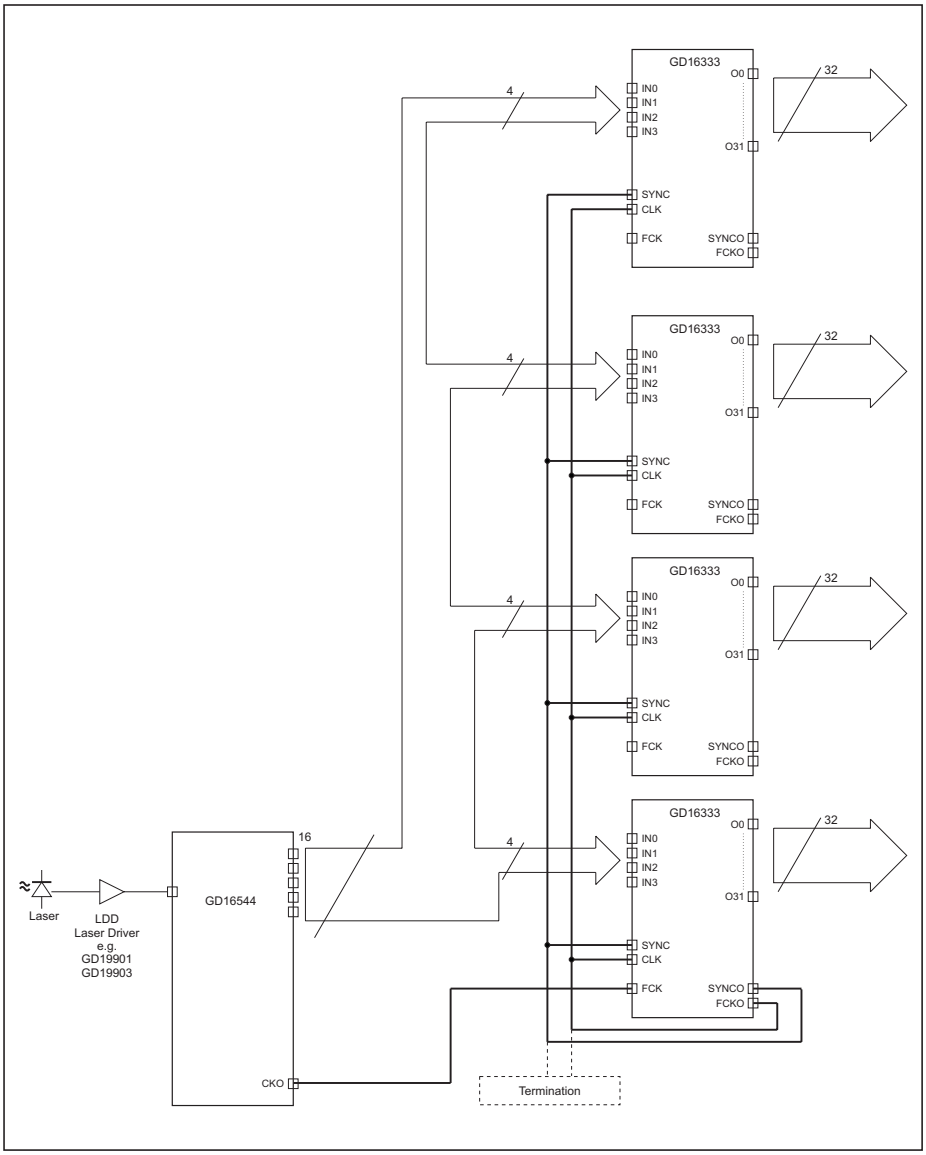


Figure 1. *GD16544: 10 Gbit/s, STM-64 receiver application.*

Another approach is to feed the input clock directly to the CLK input of the DeMUX'es, maintaining the data/clock relations as given by the upstream device (refer to Figure 2). This will however put constrains on the timing of the SYNC signal path. Depending on actual timing of the upstream device and actual board layout, both approaches may prove useful.

In either case, to compensate for board delays use the near-end device as clock master such that the clock propagating to the following slave devices outcompensates data propagating from the GD16544.

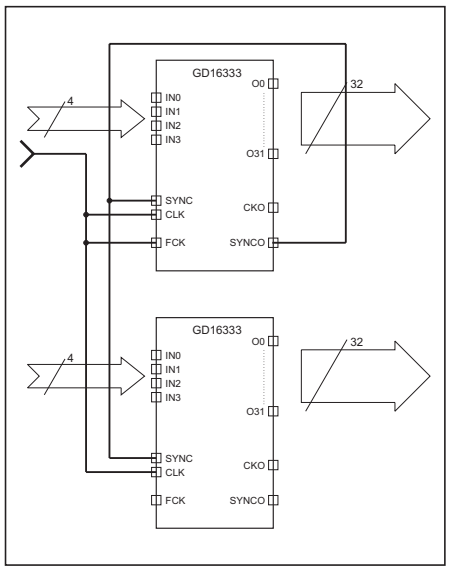


Figure 2. *Maintaining fast clock < - > data relations*

Practical Considerations

The SYNC and CLK control signals are differential high-speed control signals. Care should be taken to design the routing of these signals as transmission lines, i.e. as coplanar wave guides, or as strip lines. The signals should be routed without branches from the signal source with shortest possible distance to the first load, then onwards to the next load, and finally terminating in a resistor matching the transmission line impedance, normally 50 Ω. The transmission line should not have any branches in order to minimise stub effects (reflections).

Pin List

Mnemonic:	Pin No.:	Pin Type:	Description:
IN0, IN0N IN1, IN1N IN2, IN2N IN3, IN3N	8, 9 72, 71 58, 59 23, 22	CML/PECL IN	622 MHz differential data input.
CLK, CLKN	61, 62	CML/PECL IN	622 MHz differential clock input.
SYNC, SYNCN	63, 64	CML/PECL IN	78 MHz differential synchronization input.
O0, O4, O8, O12, O16, O20, O24, O28	6, 5, 4, 3, 98, 97, 96, 95	CMOS OUT	78 MHz DeMUXed IN0.
O1, O5, O9, O13, O17, O21, O25, O29	74, 75, 76, 77, 83, 84, 85, 86	CMOS OUT	78 MHz DeMUXed IN1.
O2, O6, O10, O14, O18, O22, O26, O30	56, 55, 54, 53, 48, 47, 46, 45	CMOS OUT	78 MHz DeMUXed IN2.
O3, O7, O11, O15, O19, O23, O27, O31	25, 26, 27, 28, 33, 34, 35, 36	CMOS OUT	78 MHz DeMUXed IN3.
CKO	68	CMOS OUT	78 MHz clock output.
FCK, FCKN	15, 16	CML/PECL IN	622 MHz differential input to clock divider.
FCKO, FCKON	19, 20	CML OUT	622 MHz differential clock output.
SYNCO, SYNCON	17, 18	CML OUT	78 MHz differential synchronisation output, timing identical to FCKO, for synchronisation.
TSTR	14	Sing. PECL IN	Reset to clock divider. For normal operation, connect with 1 kΩ to VEE. Only for test purpose.
VCS	12	Sense	Internal control voltage sense, leave open.
VEE	7, 11, 13, 24, 31, 32, 38, 37, 43, 44, 49, 50, 57, 66, 69, 73, 81, 82, 87, 88, 93, 94, 99, 100	GND	0 V.
VDDC	1, 30, 39, 42, 51, 67, 80, 89, 92	PWR	5 V, power supply to CMOS output drivers.
VDD	10, 21, 40, 41, 60, 65, 70, 90, 91	PWR	5 V.
NC	2, 29, 52, 78, 79		Not Connected.
Heat sink			Connect to VEE

Package Pinout

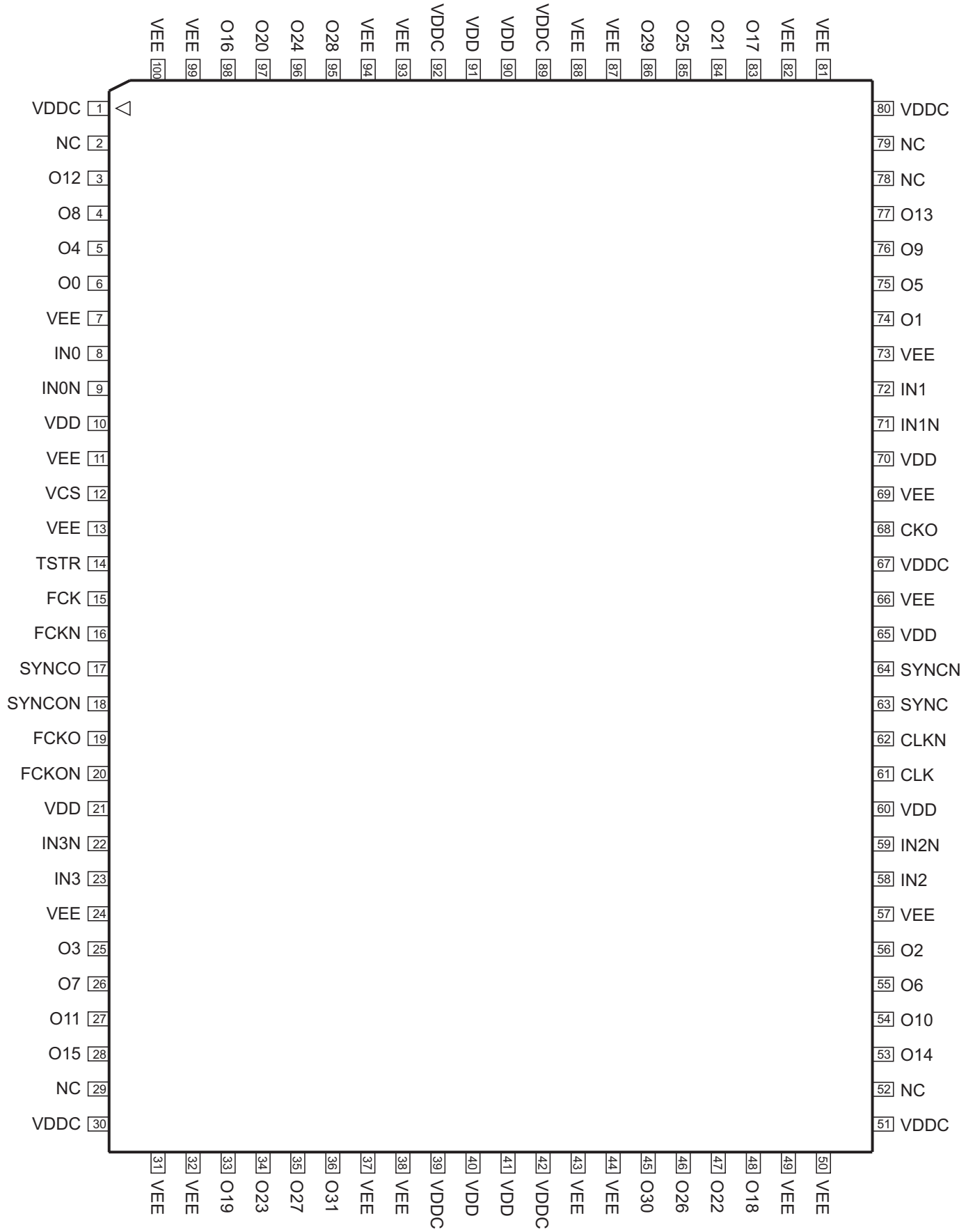


Figure 3. *Package 100 pin QFP, Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in table are referred to VEE.
All currents are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{DD}	Positive Supply	rel. to *VEE*	0		6	V
V_O *max*	Output Voltage	PECL	-0.5		V_{DD} +0.5	V
I_O *max*	Output Current	CML	-15		0	mA
I_O *max*	Output Current	CMOS Data	-15		15	mA
I_O *max*	Output Current	CMOS CKO	-30		30	mA
V_I *max*	Input Voltage	PECL	-0.5		V_{DD} +0.5	V
I_I *max*	Input Current	PECL	-1.0		1.0	mA
T_S	Operating Temperature	Junction	-55		+150	°C
T_O	Storage Temperature		-65		+175	°C

Thermal Characteristics

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
$\theta_{j\text{-}c}$	Thermal resistance, junction to case			11.7		°C/W
$\theta_{j\text{-}a}$	Thermal resistance, junction to ambient	Still air, Horizontal mounting		42		°C/W
T_o	Operating Temperature	Case	-5		85	°C

Thermal Considerations

A heat-conducting slug is placed at the bottom of the package allowing heat dissipation out of the bottom of the IC package to the PCB. The heat slug can be soldered to a conducting plane (VEE) on the PCB using solder paste, or a thermally conducting foil can be placed under the package. If the thermal foil method is preferred, a 0.25 mm thick foil may be used.

Via holes for heat transfer to the other side of the PCB should be made and a heat sink can be attached on the opposite side of the PCB if required.

DC Characteristics

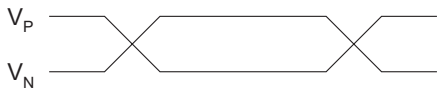
All voltages in table are referred to VEE.
All currents are defined positive out of the pin.
T_{CASE} = -5°C to 85°C.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{DD}	Supply Voltage		4.75	5.00	5.40	V
I_{DD}	Supply Current	Note 1		220		mA
$V_{CM,CML/PECL}$	CML/PECL Input Common Mode Voltage	Note 2	V_{DD} - 2		V_{DD} - 0.2	V
$V_{diff,CML/PECL}$	CML/PECL Input Differential Swing	Note 3	100		1400	mV
$I_{IH,PECL}$	CML/PECL Input HI Current	V_{IH} *max*			100	µA
$I_{IL,PECL}$	CML/PECL Input LO Current	V_{IL} *max*	-100			µA
$V_{Ipp,CML}$	CML Differential Input V p-p		100			mV
$V_{Opp,CML}$	CML Differential Output V p-p		200			mV
$V_{OH,CMOS}$	CMOS Output HI Voltage		4			V
$V_{OL,CMOS}$	CMOS Output LO Voltage				0.4	V
$I_{OH,CMOS}$	CMOS Output HI Current Data				4	mA
$I_{OH,CMOS}$	CMOS Output HI Current CKO				16	mA
$I_{OL,CMOS}$	CMOS Output LO Current Data		-4			mA
$I_{OL,CMOS}$	CMOS Output LO Current CKO		-16			mA

Note 1: Measured at DC, no signal on CMOS outputs.

Note 2: $V_{CM} = \frac{V_P + V_N}{2}$

Note 3: $V_{diff} = |V_P - V_N|$



AC Characteristics

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
Tpd,fcko	Delay from FCK to FCKO			900		ps
Tpd,synco	Delay from FCK to SYNCO			1300		ps
Ts,in	Input set-up time before CLK			250		ps
Th,in	Input hold time after CLK			-100		ps
Ts,sync	SYNC set-up time before CLK			-500		ps
Th,sync	SYNC hold time after CLK			700		ps
Tpd	CKO to output delay			3200		ps

Note: All timing data are based on one prototype measurement.

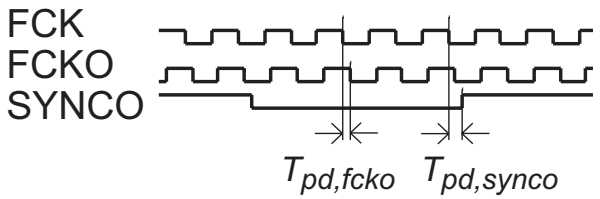


Figure 4. *Fast Clock Divider*

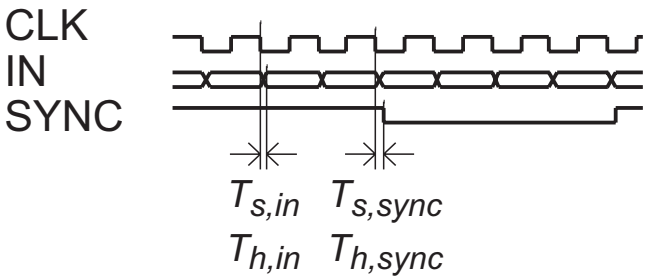


Figure 5. *Input*

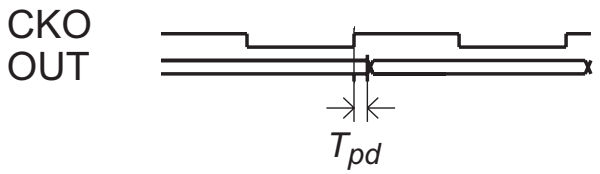


Figure 6. *Output*

Note: When SYNC is sampled low, after a high sample, the internal clock divider is reset, giving a low CKO and data output two CLK samples after SYNC is sampled low.

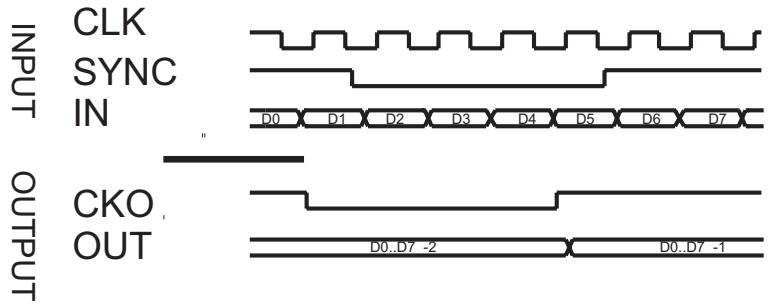
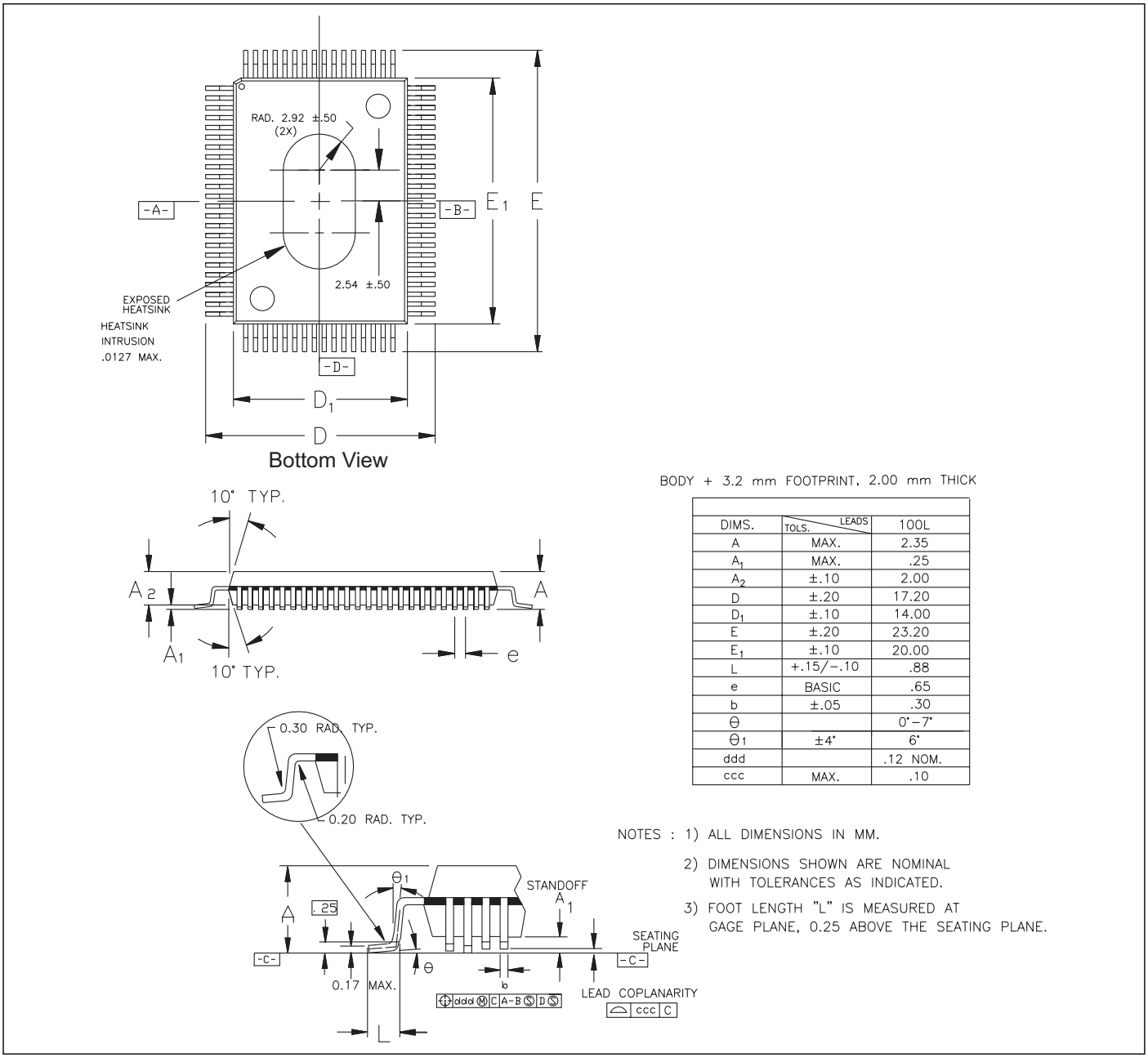


Figure 7. *Input/Output Relations*

Package Outline



BODY + 3.2 mm FOOTPRINT, 2.00 mm THICK

DIMS.	TOLS. \ LEADS	100L
A	MAX.	2.35
A_1	MAX.	.25
A_2	±.10	2.00
D	±.20	17.20
D_1	±.10	14.00
E	±.20	23.20
E_1	±.10	20.00
L	+.15/−.10	.88
e	BASIC	.65
b	±.05	.30
θ		0°−7°
θ_1	±4°	6°
ddd		.12 NOM.
ccc	MAX.	.10

NOTES : 1) ALL DIMENSIONS IN MM.

2) DIMENSIONS SHOWN ARE NOMINAL WITH TOLERANCES AS INDICATED.

3) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, 0.25 ABOVE THE SEATING PLANE.

Figure 8. *Package 100 pin QFP, Power Enhanced.*

Device Marking

GD16333
<MaskID>
<Assembly Lot #> <YYWW>

Figure 9. *Device Marking - Top View*

Ordering Information

To order, please specify as shown below:

Product Name:	Package Type:	Case Temperature Range:	Options:
GD16333 - QFP100	100 pin QFP, EDQUAD	-5 °C..+85 °C	

Mileparken 22, DK-2740 Skovlunde
Denmark
Phone : +45 7010 1062
Fax : +45 7010 1063
E-mail : sales@giga.dk
Web site : http://www.giga.dk

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