

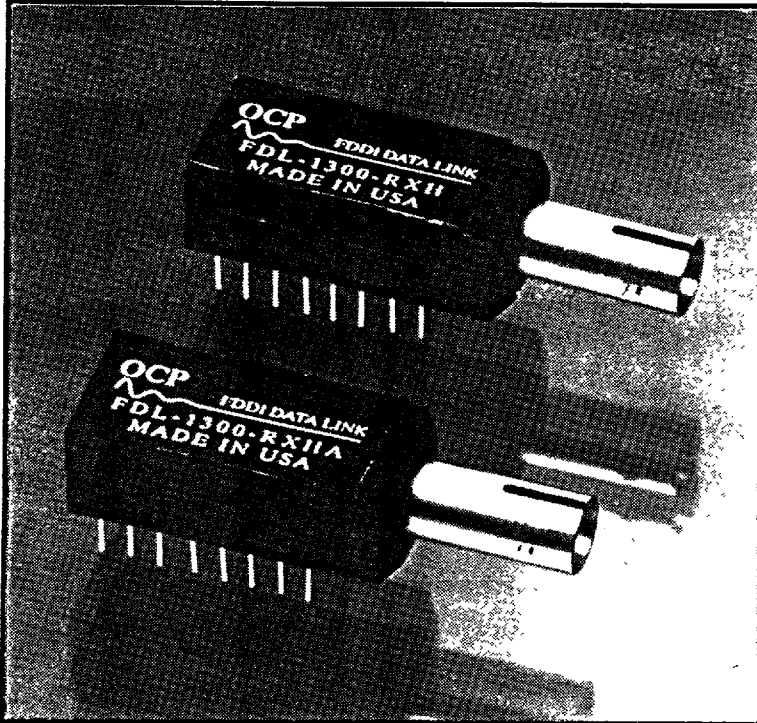
OCP

T-41-91

Preliminary

FDL-1300-RX-H & FDL-1300-RX-HA**High Sensitivity & Wide Dynamic Range Receivers****Features**

- Compliant with SONET OC-1 & OC-3 Standard
- Meets or Exceeds FDDI Standard Requirements
- Wide Dynamic Range with Internal AGC
- Signal Detect Status Output
- Single Supply Voltage (+5 V or -5.2 V)
- Integral ST™ Optical Connector
- 16-pin Dual-in-Line Conductive Plastic Package
- 40°C to +85°C Operation

**Description**

The FDL-1300-RX-H & FDL-1300-RX-HA receivers are designed to be used where both a high receiver sensitivity and a wide dynamic range are required. It incorporates an advanced InGaAs PIN photodiode, an ultra low noise GaAs MESFET IC transimpedance amplifier and a post amplifier-regenerator IC. The transimpedance amplifier IC incorporates an internal automatic-gain-control (AGC) circuitry so that a very wide dynamic range can be achieved for easy system configuration. The post amplifier-regenerator IC generates differential ECL data outputs as well as a Signal Detect Status Output Flag.

The FDL-1300-RX-H & FDL-1300-RX-HA receivers are compliant with the OC-1 and OC-3 data rates

of the SONET (SDH) standard. They also exceed the FDDI sensitivity and dynamic range requirements. They can also be used for any fiber optic receiver operating between 5 Mb/s to 160 Mb/s.

The FDL-1300-RX-H/HA receivers are housed in a cost-effective 16-pin dual-in-line conductive plastic package with integral ST™ connector and operate on standard +5 volt or -5.2 volt power supply.

The FDL-1300-RX-H receiver is pin compatible with the DTL-1300 and LDL-1300 Receiver Modules from Optical Communication Products, Inc. The FDL-1300-HA receiver is pin compatible with the ODL-125 Data Link Modules from AT&T.

Optical Communication Products, Inc.

ST is a trademark of AT&T

Receiver Operation

The receiver converts the incident optical power to a photocurrent using a high performance PIN photodiode. The photocurrent is converted to an analog voltage by a transimpedance amplifier. This analog signal is then amplified by additional gain stages and processed through a shaping filter and a comparator to generate the differential ECL output signals. Both outputs (DATA and $\overline{\text{DATA}}$) are open emitters requiring termination to $V_{CC} - 2$ volts with 50Ω or to V_{EE} with 510Ω . For optimum performance both outputs should be terminated identically, even if only one output is used.

The Signal Detect circuit monitors the level of incoming optical signal and generates a logic LOW signal when insufficient photocurrent is produced to ensure proper operation. The Signal Detect can be used to control an external squelch circuit to gate off spurious outputs generated by the receiver when no optical input is available. The outputs are open emitter ECL requiring termination (510Ω to V_{EE} is recommended).

PCB Layout Considerations

The differential outputs from the receiver are high speed emitter coupled logic signals. Printed circuit board interconnections should be configured in accordance with ECL design rules. The *MECL System Design Handbook* from Motorola, Inc. is an excellent reference. Board layouts created by CAD autorouting techniques should be reviewed carefully. Special care should be taken with the

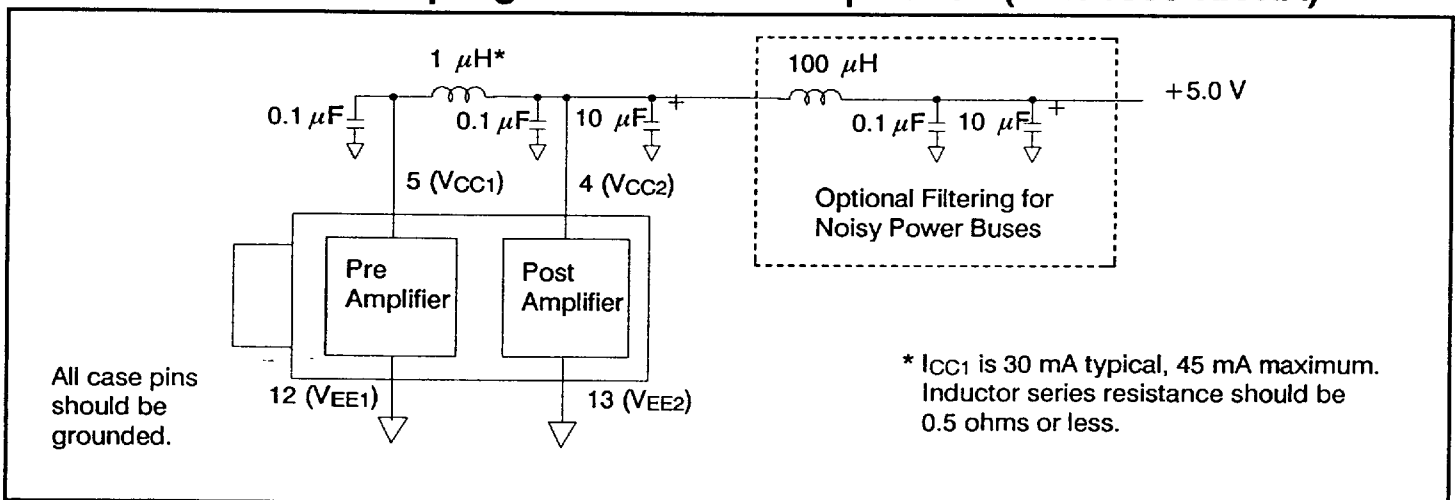
receiver, since it is a very sensitive analog device. If the receiver outputs drive long traces or multiple loads, the use of an ECL buffer gate to isolate the receiver from transmission line reflections is recommended. A solid ground plane and low impedance power supply traces are highly recommended.

EMI Susceptibility

The receiver power supply leads should be bypassed with RF quality capacitors (0.1 microfarad) close to the package. The receiver circuit contains sensitive analog circuitry and is

housed in a conductive plastic package. While shielding is provided, it is recommended that the receiver be located away from strong sources of radiated EMI.

Recommended De-Coupling Circuit for +5 V Operation (FDL-1300-RX-HA)



Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	- 55	+ 100	°C
Operating Temperature	- 40	+ 85	°C
Supply Voltage	0	+ 6.0	V
Input Voltage	0	+ 6.0	V
Lead Soldering	-	240 °C, 10 sec	-

Receiver Electrical Interface

Parameter	Symbol	Minimum	Typical	Maximum	Units	
Supply Voltage	+ 5 V	V _{CC}	4.5	5.0	5.5	V
	- 5.2 V	V _{EE}	- 5.5	- 5.2	- 4.5	V
Supply Current	I	-	80	100	mA	
Power Dissipation	P	-	400	550	mW	
Output HIGH Voltage	V _{OH}	V _{CC} - 1.035	-	V _{CC} - 0.88	V	
Output LOW Voltage	V _{OL}	V _{CC} - 1.83	-	V _{CC} - 1.62	V	

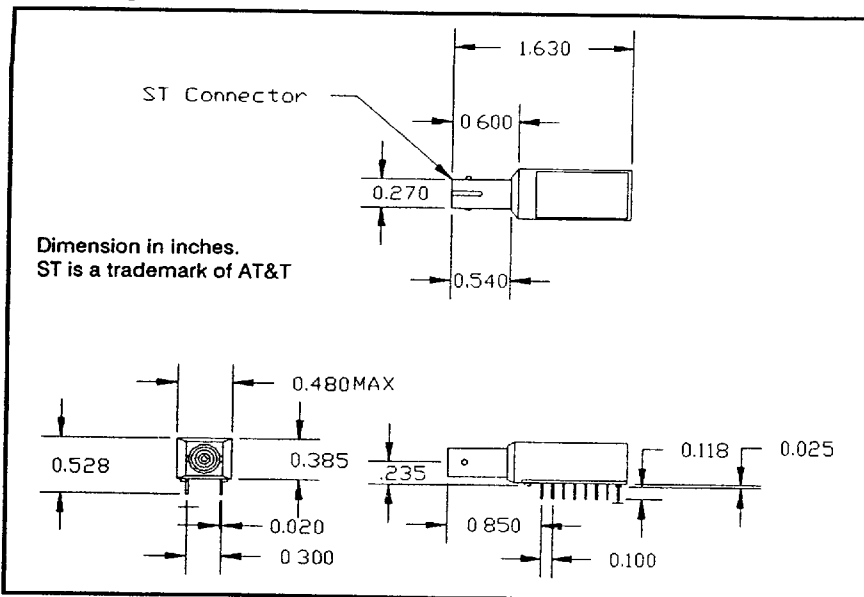
Receiver Performance (Over Operating Temperature Range -40°C to +85°C)

Parameter	Symbol	Minimum	Typical	Maximum	Units	
Data Rate	B	5	125	160	Mb/s	
Optical Input Power (BER = 10 ⁻¹⁰)	OC-1 ¹	\bar{P}_{in}	- 40.0	-	- 7.0	dBm
	OC-3 ¹		- 36.0	-		
	FDDI ^{1,2}		- 36.0	-		
Signal Detect Thresholds	OC-1	P _{sd}	- 50.0	-	- 40.0	dBm
	OC-3 & FDDI		- 45.0	-	- 36.0	
Signal Detect Hysteresis			1.5	-	-	dB
Signal Detect Timing	Assertion	T _{sd}	-	-	100	μs
	Deassertion		-	-	350	
Wavelength of Operation	λ	1100	1320	1600	nm	

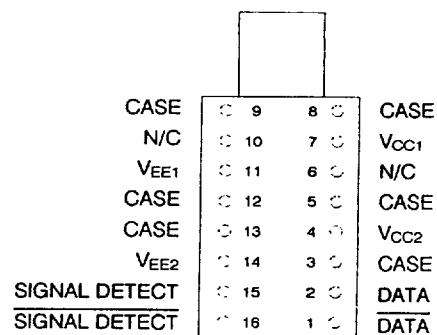
¹ When tested with an optical rise/fall time of 2.5 nsec at 1300 nm wavelength and optimum sampling point with 2²³-1 PRBS at 52 Mb/s for OC-1, 155 Mb/s for OC-3 and 125 Mb/s for FDDI.

² With worst case FDDI Test Conditions, the minimum sensitivity is -34.0 dBm.

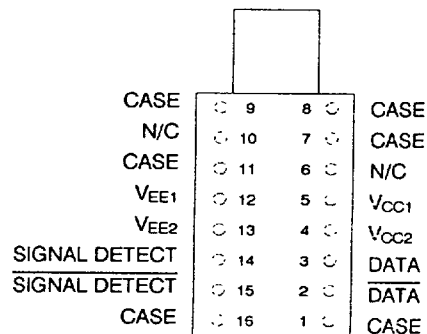
Package Outline



Pin Assignments (Top View)



FDL-1300-RX-H



FDL-1300-RX-HA

N/C — No internal connection

Ordering Information

FDL - 1300 - RX - XX - XX

Type

Bit rate

HA: AT&T ODL-125 pinout
H : OCP DTL & LDL pinout

01: OC1 (52 Mb/s)
02: FDDI (125 Mb/s)
03: OC3 (155 Mb/s)

HANDLING PRECAUTIONS

Normal handling precautions for electrostatic sensitive devices should be observed.

Optical Communication Products

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