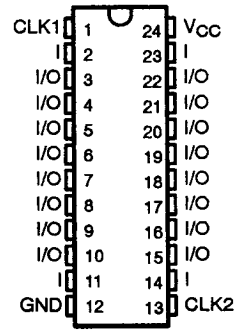
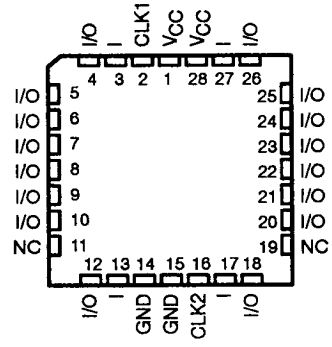
- Programmable Replacement for Conventional TTL and 74HC Devices
- Virtually Zero Standby Current
  Typ 20 μA
- Low Operating Current:
  I_{CC} max (turbo bit on) . . . 90 mA
  I_{CC} max (turbo bit off) . . . 10 mA
- High Performance CMOS Process Allows:
  Maximum t_{pd}: - 15C . . . 15 ns
  - 20C . . . 20ns
  - 25I . . . 25 ns
- Asynchronous Clocking of All Registers or Banked Register Operation From 2 Synchronous Clocks
- Sixteen Macrocells With Configurable I/O Architecture Allowing for up to 20 Inputs and 16 Outputs
- User-Programmable Output Logic Macrocells Provide Flexibility in Output Types with:
  Selectable for Registered or Combinational Operation
  Output Polarity Control
  Independently User Programmable Feedback Path
- Programmable Design Security Bit Prevents Copying of Logic Stored in Device
- Third-Party Advanced Software Support Featuring Schematic Capture, Interactive Netlist, Boolean Equations, and State Machine Design Entry

NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

AVAILABLE OPTIONS

T_A RANGE	PACKAGE TYPE	
	PLASTIC DUAL-IN-LINE PACKAGE (PDIP)	PLASTIC CHIP CARRIER PACKAGE (PLCC)
0°C to 70°C	EP630-15CNT	EP630-15CFN
	EP630-20CNT	EP630-20CFN
–40°C to 85°C	EP630-25INT	EP630-25IFN

description

general

The Texas Instruments EP630 is capable of implementing over 600 equivalent gates of SSI and MSI logic functions all in plastic and ceramic space-saving 24-pin, 300-mil dual-in-line (DIP) packages and 28-pin chip-carrier packages. It uses the familiar sum-of-products logic, providing a programmable AND with a fixed OR structure. The device accommodates both combinational and sequential (registered) logic functions with up to 20 inputs and 16 outputs. The EP630 has a user programmable output logic macrocell that allows each output to be configured as a combinational or registered output and feedback signals active high or active low.

A unique feature of the EP630 is the ability to program D, T, SR, or JK flip-flop operation individually for each output without sacrificing product terms. In addition, each register can be individually clocked from any of the input or feedback paths available in the AND array. These features allow a variety of logic functions to be simultaneously implemented.

The CMOS EPROM technology reduces the power consumption to less than 55% of equivalent bipolar devices without sacrificing speed performance. Erasable EPROM bits allow for enhanced factory testing.

Programming the EP630 is made easy by the availability of extensive third-party support for design entry, design processing and device programming.

The EP630-15C and EP630-20C devices are characterized for operation from 0°C to 70°C. The EP630-25I is characterized for operation from −40°C to 85°C.

functional

The EP630 uses a CMOS EPROM technology to implement logic designs in a programmable AND logic array. The device contains a revolutionary programmable I/O architecture that provides advanced functional capability for user programmable logic.

Externally, the EP630 provides 4 dedicated data inputs and 16 I/O pins, which may be configured for input, output, or bidirectional operation. Figure 1 shows the EP630 basic logic array macrocell. The internal architecture is organized with familiar sum-of-products (AND-OR) structure. Inputs to the programmable AND array come from true and complement signals from the 4 dedicated data inputs and the 16 I/O architecture-control blocks. The 40-input AND array encompasses 160 product terms, which are distributed among 16 available macrocells. Each EP630 product term represents a 40-input AND gate.

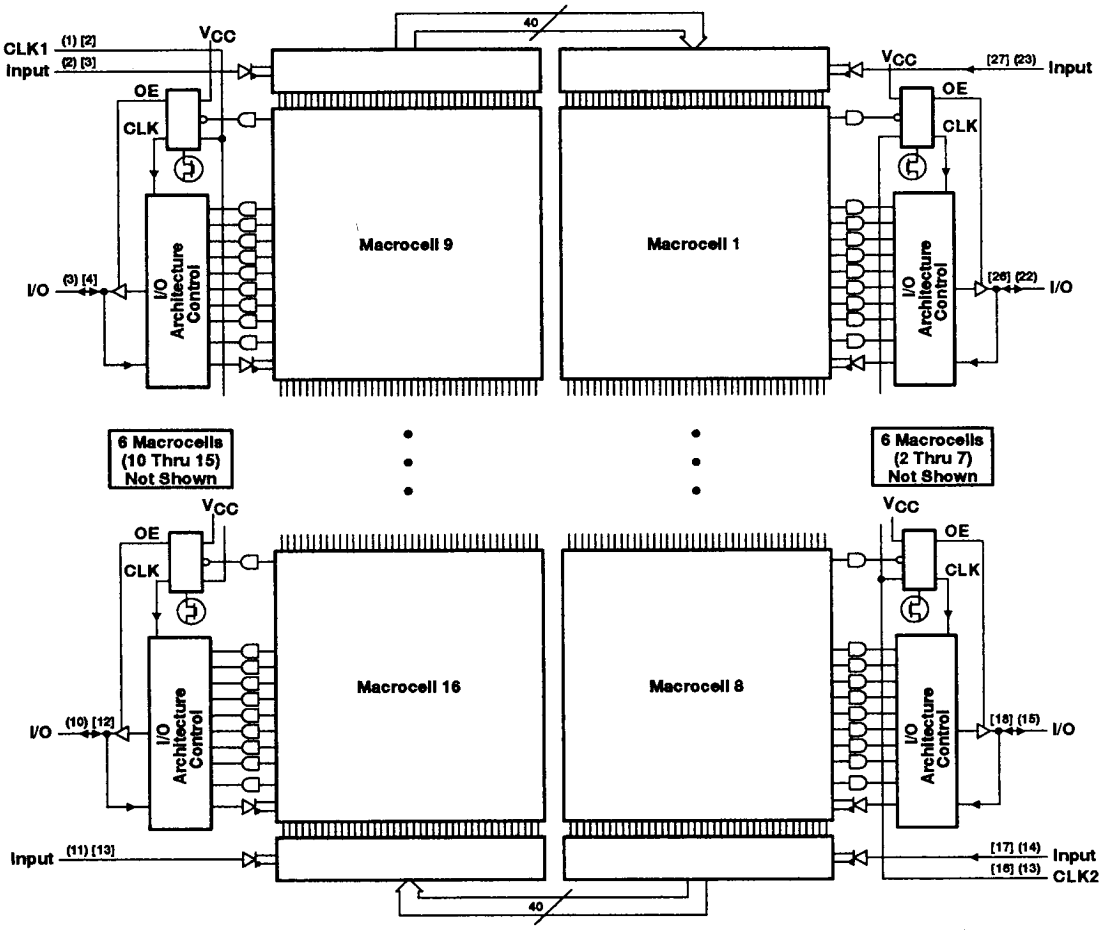
Each macrocell contains 10 product terms, 8 of which are dedicated for logic implementation. One product term is used for clear control of the macrocell internal register. The remaining product term is used for output enable/asynchronous clock implementation.

There is an EPROM connection at the intersection point of each input signal and each product term. In the erased state, all connections are made. This means both the true and complement forms of all inputs are connected to each product term. Connections are opened during the programming process. Therefore, any product term may be connected to the true or complement form of any array input signal.

When both the true and complement forms of any signal are left intact, a logical false state results on the output of the AND gate. If both the true and complement connections are open, then a logical "don't care" applies for that input. If all inputs for the product term are programmed open, then a logical true state results on the output of the AND gate.

Two dedicated clock inputs provide synchronous clock signals to the EP630 internal registers. Each of the clock signals controls a bank of 8 registers. CLK1 controls registers associated with macrocells 9-16, and CLK2 controls registers associated with macrocells 1-8. The EP630 advanced I/O architecture allows the number of synchronous registers to be user defined, from one to sixteen. Both dedicated clock inputs are positive-edge-triggered.

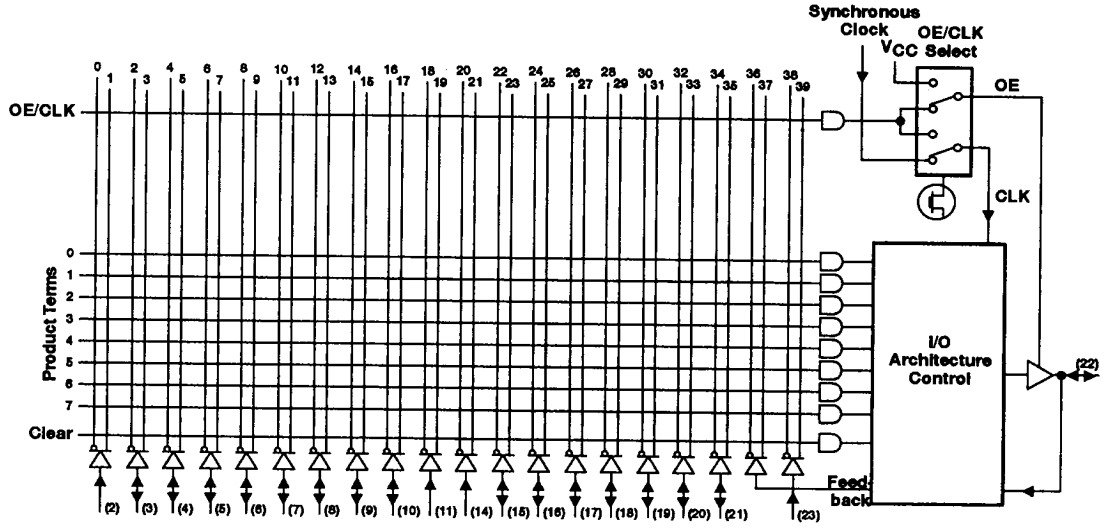
functional block diagram



Pin numbers in ( ) are for DIP packages; pin numbers in [ ] are for the chip-carrier package.

I/O architecture

The EP630 input/output architecture provides each macrocell with over 50 possible I/O configurations. Each I/O can be configured for combinational or registered output, with programmable output polarity. Four different types of registers (D, T, JK, and SR) can be implemented into every I/O without any additional logic requirements. I/O feedback selection can also be programmed for registered or input (pin) feedback. Another benefit of the EP630 I/O architecture is its ability to individually clock each internal register from asynchronous clock signals.



Pin numbers are for the NT package.

Figure 1. Logic Array Macrocell (Macrocell 1 Illustrated)

OE/CLK selection

Figure 2 shows the two modes of operation that are provided by the OE/CLK select multiplexer. The operation of this multiplexer is controlled by a single EPROM bit and may be individually configured for each EP630 I/O pin. In Mode 0, the 3-state output buffer is controlled by a single product term. If the output of the AND gate is true, the output buffer is enabled. If the output of the AND gate is false, the output buffer is in the high-impedance state. In this mode, the macrocell flip-flop may be clocked by its respective synchronous clock input. After erasure, the OE/CLK select multiplexer is configured in Mode 0.

In Mode 1, the output-enable buffer is always enabled. The macrocell flip-flop may now be triggered from an asynchronous clock signal generated by the OE/CLK multiplexable product term. This mode allows individual clocking of flip-flops from any available signal in the AND array. Because both true and complement signals reside in the AND array, the flip-flop may be configured for positive- or negative-edge-triggered operation. With the clock now controlled by a product term, gated clock structures are also possible.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

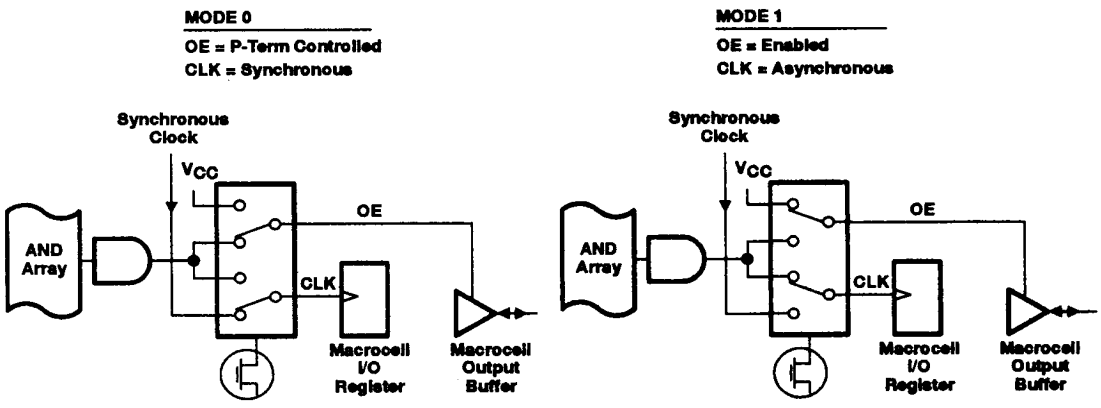


Figure 2. OE/CLK Select Multiplexer

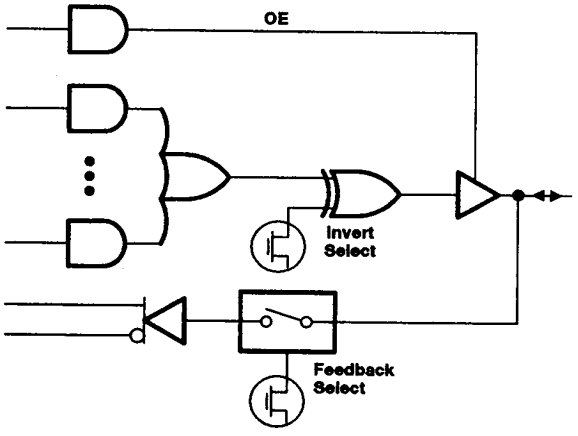
output/feedback selection

Figure 3 shows the EP630 basic output configurations. Along with combinational output, four register types are available. Each macrocell I/O may be independently configured. All registers have individual asynchronous clear control from a dedicated product term. When the product term is asserted, the macrocell register will immediately be loaded with a zero independent of the clock. On power-up, The EP630 performs the clear function automatically.

When the D or T register is selected, eight product terms are ORed together and made available to the register input. The invert select EPROM bit determines output polarity. The feedback-select multiplexer enables register, I/O (pin), or no feedback to the AND array.

If the JK or SR registers are selected, the eight product terms are shared between two OR gates. The invert select EPROM bit configures output polarity. The feedback-select multiplexer enables registered or no feedback to the AND array.

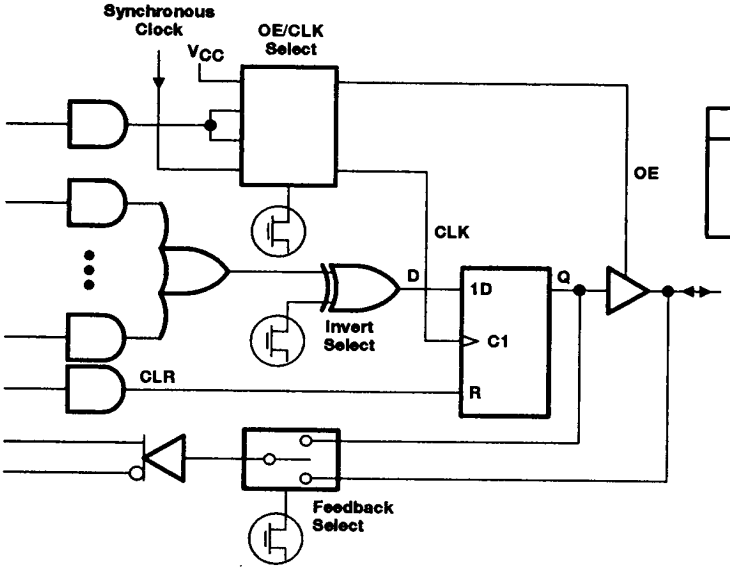
Any I/O pin may be configured as a dedicated input by selecting no output and pin feedback. No output is obtained by disabling the macrocell output buffer. In the erased state, each I/O is configured for combinational active-low output with input (pin) feedback.



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinational/high	Pin, None
Combinational/low	Pin, None
None	Pin

(a) COMBINATIONAL



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
D Register/high	D Register, Pin, None
D Register/low	D Register, Pin, None
None	D Register
None	Pin

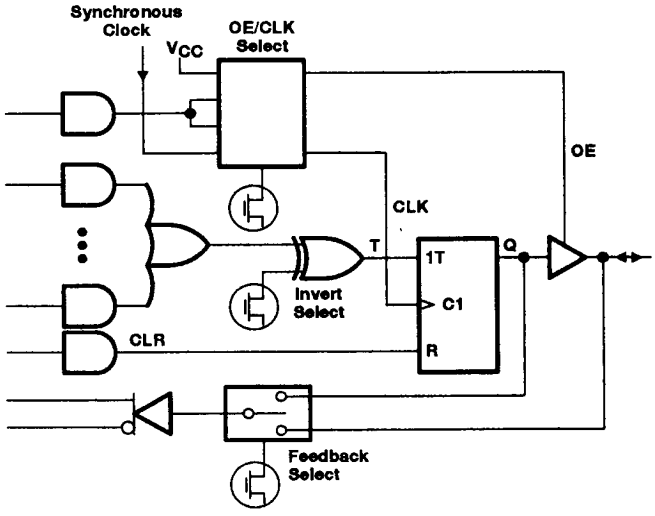
FUNCTION TABLE

INPUTS			OUTPUT
CLR	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q_O
H	X	X	L

(b) D-TYPE FLIP-FLOP

Figure 3. I/O Configurations

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265



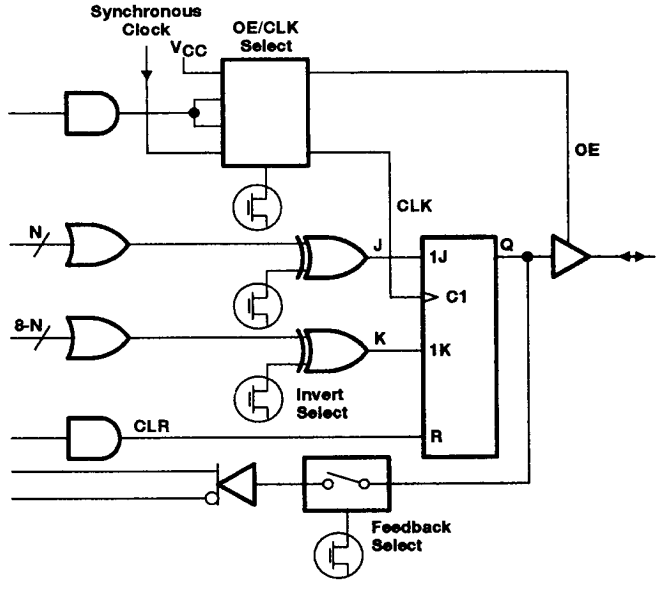
I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
T Register/high	T Register, Pin, None
T Register/low	T Register, Pin, None
None	T Register
None	Pin

FUNCTION TABLE

INPUTS			OUTPUT
CLR	CLK	T	Q
L	↑	L	Q_O
L	↑	H	$\overline{Q}_O$
L	L	X	Q_O
H	X	X	L

(c) TOGGLE FLIP-FLOP



I/O SELECTION

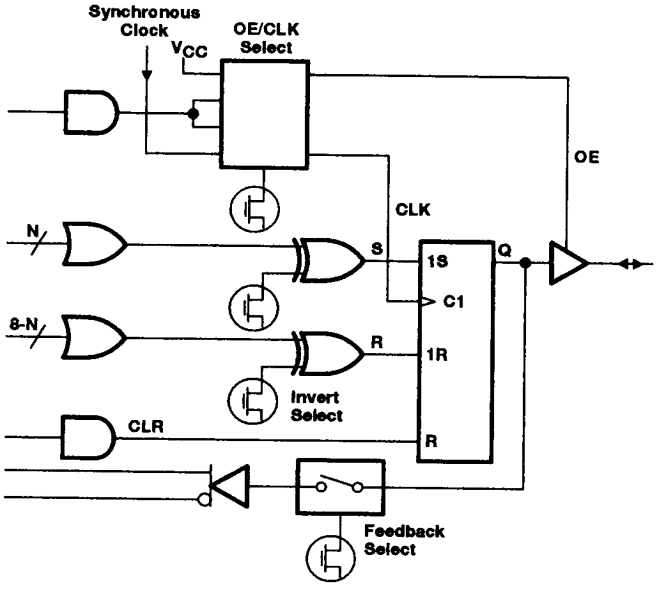
OUTPUT/POLARITY	FEEDBACK
JK Register/high	JK Register, None
JK Register/low	JK Register, None
None	JK Register

FUNCTION TABLE

INPUTS				OUTPUT
CLR	CLK	J	K	Q
L	↑	L	L	Q_O
L	↑	L	H	L
L	↑	H	L	H
L	↑	H	H	$\overline{Q}_O$
L	L	X	X	Q_O
H	X	X	X	L

(d) J-K FLIP-FLOP

Figure 3. I/O Configurations (Continued)



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
SR Register/high	SR Register, None
SR Register/low	SR Register, None
None	SR Register

FUNCTION TABLE

INPUTS				OUTPUT
CLR	CLK	S	R	Q
L	↑	L	L	Q_O
L	↑	L	H	L
L	↑	H	L	H
L	↑	H	H	Undefined
L	L	X	X	Q_O
H	X	X	X	L

(e) S-R FLIP-FLOP

Figure 3. I/O Configurations (Continued)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Instantaneous supply voltage range, V_{CC} ($t \leq 20$ ns) ..... −2 V to 7 V
Programming supply voltage range, V_{pp} ..... −0.3 V to 14 V
Instantaneous programming supply voltage range, V_{pp} ($t \leq 20$ ns) ..... −2 V to 14 V
Input voltage range, V_I ..... −0.3 V to 7 V
Instantaneous input voltage range, V_I ($t \leq 20$ ns) ..... −2 V to 7 V
V_{CC} or GND current range ..... −175 mA to 175 mA
Operating free-air temperature range, T_A ..... −65°C to 135°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: All voltage values are with respect to GND terminal.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_{IH}	High-level input voltage		2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 2)		−0.3	0.8	V
V_O	Output voltage		0	V_{CC}	V
t_r	Rise time	CLK input		20	ns
		Other inputs		40	
t_f	Fall time	CLK input		20	ns
		Other inputs		40	
T_A	Operating free-air temperature		0	70	°C

NOTE 2: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL	V_{CC} = 4.75 V,	I_{OH} = −4 mA	2.4		V
		CMOS	V_{CC} = 4.75 V,	I_{OH} = −2 mA	3.84		
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 4 mA		0.45	V
I_I	Input current		V_{CC} = 5.25 V,	V_I = V_{CC} or GND		±10	µA
I_{OZ}	Off-state output current		V_{CC} = 5.25 V,	V_O = V_{CC} or GND		±10	µA
I_{CC}	Supply current	Standby	V_{CC} = 5.25 V,	See Note 3		150	µA
		Nonturbo	V_I = V_{CC} or GND,	See Note 4		10	mA
		Turbo	No load	See Note 4		90	
C_i	Input capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C		10	pF
C_o	Output capacitance		V_O = 0, f = 1 MHz,	T_A = 25°C		12	pF
C_{clk}	Clock capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C		20	pF

NOTES: 3. When in nonturbo, the device automatically goes into the standby mode approximately 100 ns after the last transition.
4. These parameters are measured with the device programmed as a 16-bit counter and f = 1 MHz.

switching characteristics over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

combinational mode, turbo bit on

PARAMETER†		TEST CONDITIONS		EP630-15C		EP630-20C		UNIT
				MIN	MAX	MIN	MAX	
t_{pd1}	Input to nonregistered output delay	C_L = 35 pF			15		20	ns
t_{pd2}	I/O input to nonregistered output delay				17		22	ns
t_{PZX}	Output enable time	C_L = 35 pF	See Note 5		15		20	ns
t_{PXZ}	Output disable time	C_L = 5 pF			15		20	ns
t_{io}	I/O input buffer delay				2		2	ns

combinational mode, turbo bit off

PARAMETER†		TEST CONDITIONS		EP630-15C		EP630-20C		UNIT
				MIN	MAX	MIN	MAX	
t_{pd1}	Input to nonregistered output delay	C_L = 35 pF			35		40	ns
t_{pd2}	I/O input to nonregistered output delay				37		42	ns
t_{PZX}	Output enable time	C_L = 35 pF	See Note 5		35		40	ns
t_{PXZ}	Output disable time	C_L = 5 pF			35		40	ns
t_{io}	I/O input buffer delay				2		2	ns

synchronous clock mode, mode 0

PARAMETER†			TEST CONDITIONS	EP630-15C		EP630-20C		UNIT
				MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency‡	No feedback		83.3		62.5		MHz
		Internal feedback		83.3		62.5		
		External feedback§		50		41.6		
t_{co1}	Clock to output delay time				11		13	ns
t_{cnt}	Minimum clock period (register feedback to register output)		See Note 6		12		16	ns
t_{clr}	Asynchronous output clear time	Turbo bit on	C_L = 35 pF		15		20	ns
		Turbo bit off			35		40	

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

‡ f_{max} with no feedback = $\frac{1}{t_{ch} + t_{cl}}$

f_{max} with internal feedback = $\frac{1}{t_{cnt}}$

f_{max} with external feedback = $\frac{1}{t_{su} + t_{co1}}$

§ f_{max} with internal feedback is programmed as a 16-bit counter.
Use t_{su} and t_{co1} for a device programmed with the turbo bit on.

NOTES: 5. This is for an output voltage change of 500 mV.
6. These parameters are measured with device programmed as a 16-bit counter.

switching characteristics over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

asynchronous clock mode, mode 1

PARAMETER†			TEST CONDITIONS	EP630-15C		EP630-20C		UNIT
				MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency‡	No feedback		71.4		55.5		MHz
		Internal feedback		71.4		55.5		
		External feedback§		47.6		35.7		
t_{aco1}	Clock to output delay time	Turbo bit on			15		20	ns
		Turbo bit off			35		40	
t_{acnt}	Minimum clock period (register feedback to register output)				14		18	ns
t_{clr}	Asynchronous output clear time	Turbo bit on	C_L = 35 pF		15		20	ns
		Turbo bit off			35		40	

timing requirements over recommended ranges of supply voltage and free-air temperature

synchronous clock mode, mode 0

PARAMETER†			EP630-15C		EP630-20C		UNIT
			MIN	MAX	MIN	MAX	
t_{su}	Input setup time	Turbo bit on	9		11		ns
		Turbo bit off	29		31		
t_h	Input hold time		0		0		ns
t_{ch}	Clock high pulse duration		6		8		ns
t_{cl}	Clock low pulse duration		6		8		ns

asynchronous clock mode, mode 1

PARAMETER†			EP630-15C		EP630-20C		UNIT
			MIN	MAX	MIN	MAX	
t_{asu}	Input setup time	Turbo bit on	6		8		ns
		Turbo bit off	26		28		
t_{ah}	Input hold time		6		8		ns
t_{ach}	Clock high pulse duration		7		9		ns
t_{acl}	Clock low pulse duration		7		9		ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

‡ f_{max} with no feedback = $\frac{1}{t_{ach} + t_{acl}}$

f_{max} with internal feedback = $\frac{1}{t_{acnt}}$

f_{max} with external feedback = $\frac{1}{t_{asu} + t_{aco1}}$

f_{max} with internal feedback is programmed as a 16-bit counter.

§ Use t_{su} and t_{co1} for a device programmed with the turbo bit on.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_I	Input voltage		0	V_{CC}	V
V_{IH}	High-level input voltage		2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 2)		−0.3	0.8	V
V_O	Output voltage		0	V_{CC}	V
t_r	Rise time	CLK input		20	ns
		Other inputs		40	
t_f	Fall time	CLK input		20	ns
		Other inputs		40	
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL	V_{CC} = 4.5 V,	I_{OH} = −4 mA	2.4		V
		CMOS	V_{CC} = 4.5 V,	I_{OH} = −2 mA	3.84		
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.45	V
I_I	Input current		V_{CC} = 5.5 V,	V_I = V_{CC} or GND		±10	µA
I_{OZ}	Off-state output current		V_{CC} = 5.5 V,	V_O = V_{CC} or GND		±10	µA
I_{CC}	Supply current	Standby	V_{CC} = 5.5 V,	See Note 3		150	µA
		Nonturbo	V_I = V_{CC} or GND,	See Note 4		15	mA
		Turbo	No load	See Note 4		150	
C_i	Input capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C		10	pF
C_o	Output capacitance		V_O = 0, f = 1 MHz,	T_A = 25°C		12	pF
C_{clk}	Clock capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C		20	pF

NOTES: 3. When in nonturbo, the device automatically goes into the standby mode approximately 100 ns after the last transition.
4. These parameters are measured with the device programmed as a 16-bit counter and f = 1 MHz.

switching characteristics over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

combinational mode, turbo bit on

PARAMETER†		TEST CONDITIONS		MIN	MAX	UNIT
t_{pd1}	Input to nonregistered output delay	C_L = 35 pF			25	ns
t_{pd2}	I/O input to nonregistered output delay				27	ns
t_{PZX}	Output enable time	C_L = 35 pF	See Note 5		25	ns
t_{PXZ}	Output disable time	C_L = 5 pF			25	ns
t_{io}	I/O input buffer delay				2	ns

combinational mode, turbo bit off

PARAMETER†		TEST CONDITIONS		MIN	MAX	UNIT
t_{pd1}	Input to nonregistered output delay	C_L = 35 pF			45	ns
t_{pd2}	I/O input to nonregistered output delay				47	ns
t_{PZX}	Output enable time	C_L = 35 pF	See Note 5		45	ns
t_{PXZ}	Output disable time	C_L = 5 pF			45	ns
t_{io}	I/O input buffer delay				2	ns

synchronous clock mode, mode 0

PARAMETER†			TEST CONDITIONS	MIN	MAX	UNIT
f_{max}	Maximum frequency‡	No feedback		50		MHz
		Internal feedback		50		
		External feedback§		33.3		
t_{co1}	Clock to output delay time				15	ns
t_{cnt}	Minimum clock period (register feedback to register output)		See Note 6		25	ns
t_{clr}	Asynchronous output clear time	Turbo bit on	C_L = 35 pF		27	ns
		Turbo bit off			47	

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

‡ f_{max} with no feedback = $\frac{1}{t_{ch} + t_{cl}}$

f_{max} with internal feedback = $\frac{1}{t_{cnt}}$

f_{max} with external feedback = $\frac{1}{t_{su} + t_{co1}}$

§ f_{max} with internal feedback is programmed as a 16-bit counter.
Use t_{su} and t_{co1} for a device programmed with the turbo bit on.

NOTES: 5. This is for an output voltage change of 500 mV.
6. These parameters are measured with device programmed as a 16-bit counter.

switching characteristics over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

asynchronous clock mode, mode 1

PARAMETER†			TEST CONDITIONS	MIN	MAX	UNIT
f_{max}	Maximum frequency‡	No feedback		50		MHz
		Internal feedback		50		
		External feedback§		28.6		
t_{aco1}	Clock to output delay time	Turbo bit on			27	ns
		Turbo bit off			47	
t_{acnt}	Minimum clock period (register feedback to register output)				35	ns
t_{clr}	Asynchronous output clear time	Turbo bit on	C_L = 35 pF		27	ns
		Turbo bit off			47	

timing requirements over recommended ranges of supply voltage and free-air temperature

synchronous clock mode, mode 0

PARAMETER†			MIN	MAX	UNIT
t_{su}	Input setup time	Turbo bit on	15		ns
		Turbo bit off	35		
t_h	Input hold time		0		ns
t_{ch}	Clock high pulse duration		10		ns
t_{cl}	Clock low pulse duration		10		ns

asynchronous clock mode, mode 1

PARAMETER†			MIN	MAX	UNIT
t_{asu}	Input setup time	Turbo bit on	8		ns
		Turbo bit off	28		
t_{ah}	Input hold time		12		ns
t_{ach}	Clock high pulse duration		10		ns
t_{acl}	Clock low pulse duration		10		ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

‡ f_{max} with no feedback = $\frac{1}{t_{ach} + t_{acl}}$

f_{max} with internal feedback = $\frac{1}{t_{acnt}}$

f_{max} with external feedback = $\frac{1}{t_{asu} + t_{aco1}}$

f_{max} with internal feedback is programmed as a 16-bit counter.

§ Use t_{su} and t_{co1} for a device programmed with the turbo bit on.

functional testing

The EP630 is functionally tested through complete testing of each programmable EPROM bit and all internal logic elements, thus ensuring 100% programming yield. As a result, traditional problems associated with fuse programmed circuits are eliminated.

design security

The EP630 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied nor retrieved. A very high level of design control is thus achieved since programmed data within EPROM cells is invisible.

turbo bit

This family of EPLDs contains a programmable option to control the automatic power-down feature that enables the low-standby-power mode of the device. This option is controlled by a turbo bit that can be set by the design software. When the turbo bit is on, the low-standby-power mode is disabled. This renders the circuit less sensitive to V_{CC} noise transients created by the power-up/power-down cycle when operating in the low-power mode. The typical I_{CC} versus frequency data for both the turbo-bit-on mode and the turbo-bit-off (low-power) mode is shown in Figure 5. All dynamic parameters are tested with the turbo bit on.

latch-up

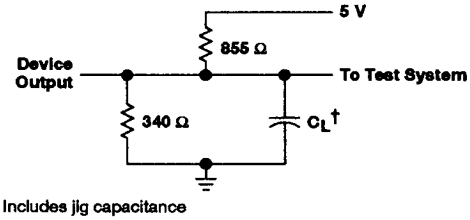
The EP630 input, I/O, and clock pins have been carefully designed to resist latch-up which is inherent in CMOS structures. None of the EP630 pins will latch up for input voltages between –1 V to V_{CC} + 1 V with currents up to 250 mA. During transitions, the inputs may undershoot to –2 V for periods of less than 20 ns.

Although the programming pin (pin 11) is designed to resist latch-up to the 14 V device limit during positive current latch-up testing, the verify mode (pin 1) and program mode (pin 11) can be inadvertently entered into thereby causing current flow in the pins. This should not be construed as latch-up.

device programming

The EP630 can be programmed using certified third-party programming equipment. Please contact Texas Instruments applications department at (214) 997-5666 for current status of third-party programming support.

PARAMETER MEASUREMENT INFORMATION



† Includes jig capacitance
Equivalent loads may be used for testing

This figure shows the test circuit and the conditions under which dynamic measurements are made. Because power supply transients can affect dynamic measurements, simultaneous transitions of multiple outputs should be avoided to ensure accurate measurement. The performance of threshold tests under dynamic conditions should not be attempted. Large-amplitude fast ground-current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground terminal and the test-system ground can create significant reductions in the observable input noise immunity.

Figure 4. Dynamic Test Circuit

TYPICAL CHARACTERISTICS

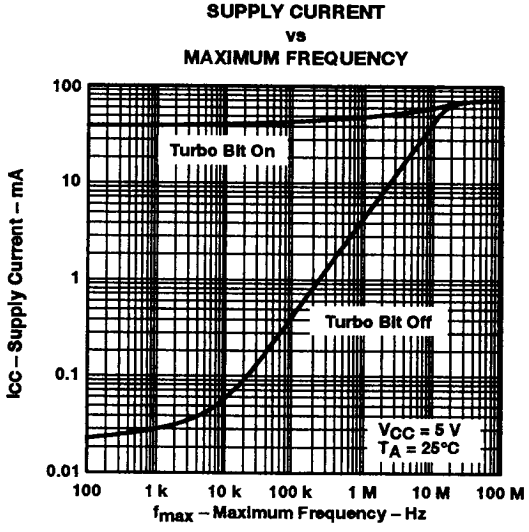


Figure 5

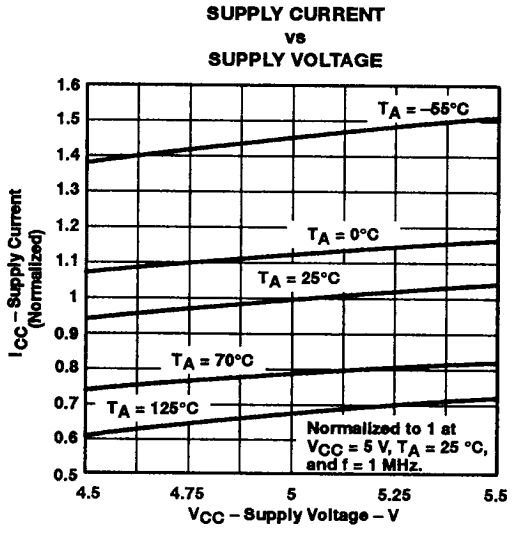


Figure 6

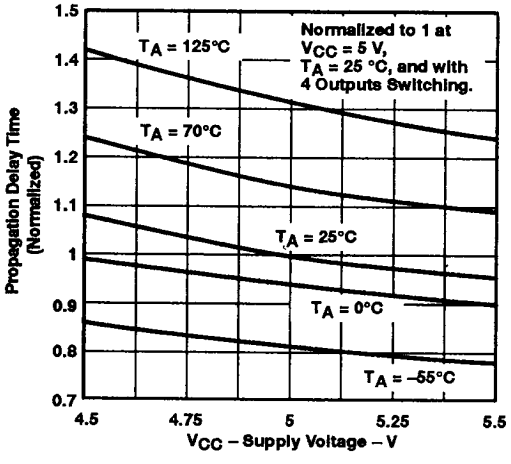


Figure 7

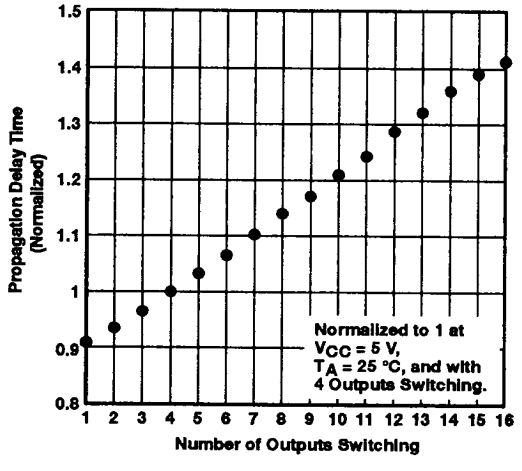
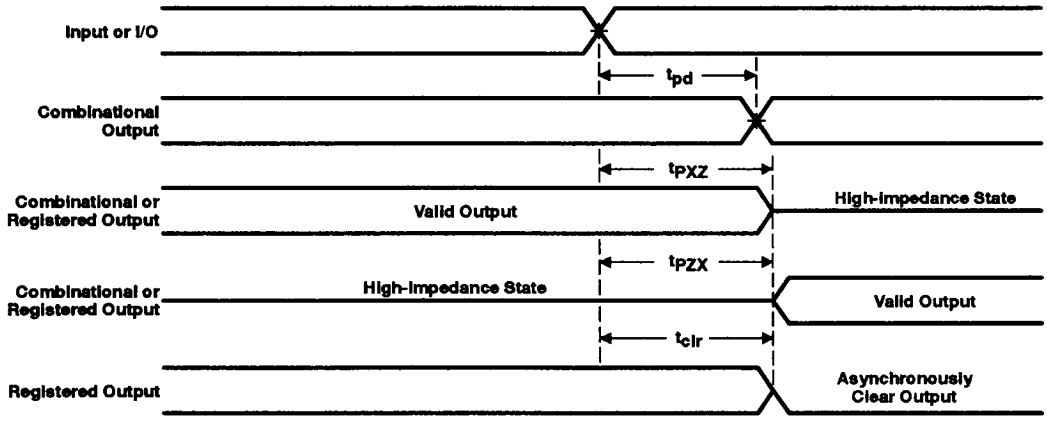
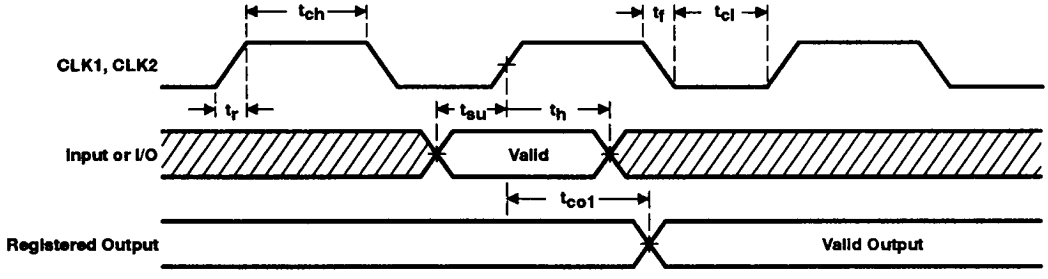


Figure 8

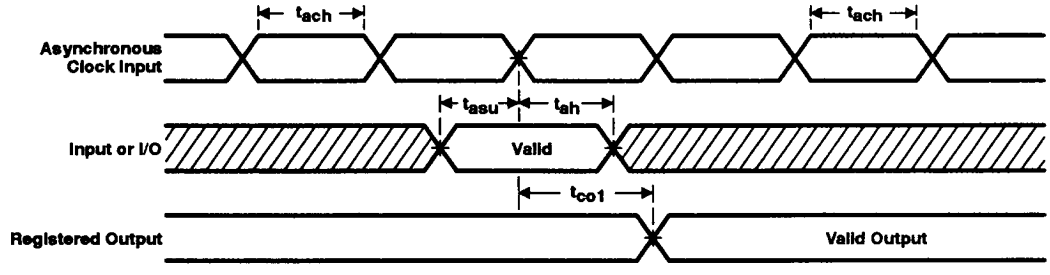
PARAMETER MEASSUREMENT INFORMATION



(a) COMBINATIONAL MODE



(b) SYNCHRONOUS CLOCK MODE



(c) ASYNCHRONOUS CLOCK MODE

NOTES: A. Input and I/O pulse levels are 0 to 3 V and $t_r = t_f \leq 2$ ns.
B. All measurements are made at 1.5 V except t_{cl} and t_{ch} are measured at 0.3 V and 2.7 V respectively and t_{PZX} and t_{PXZ} are measured for an output voltage change of 500 mV.

Figure 9. Switching Waveforms