

SONY CXK584000TM/YM/M/P -55L/70L/85L/10L -55LL/70LL/85LL/10LL

524288-word × 8-bit High Speed CMOS Static RAM

Preliminary

Description

CXK584000TM/YM/M/P is a 4,194,304 bits high speed CMOS static RAM organized as 524,288 words by 8-bits. Polysilicon TFT cell technology realized extremely low stand-by current and higher data retention stability. Operating on a single 2.7 to 5.5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

Features

- Wide supply voltage range: 2.7 to 5.5V
- Fast access time: 5V operation/3V operation

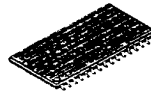
-55L/55LL	55ns/110ns (Max.)
-70L/70LL	70ns/140ns (Max.)
-85L/85LL	85ns/170ns (Max.)
-10L/10LL	100ns/200ns (Max.)
- Low stand-by current:

-55L/70L/85L/10L	100 μ A (Max.)
-55LL/70LL/85LL/10LL	50 μ A (Max.)
- Low data retention current:

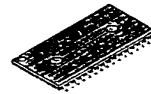
-55L/70L/85L/10L	15 μ A (Max.) Ta=0 to +40 °C
-55LL/70LL/85LL/10LL	3 μ A (Max.) Ta=0 to +40 °C
- Low voltage data retention: 2.0V (Min.)
- Package line-up

CXK584000TM/YM	400mil 32 pin TSOP (Type II)
CXK584000M	525mil 32 pin SOP
CXK584000P	600mil 32 pin DIP

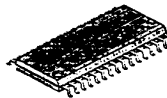
CXK584000TM
32 pin TSOP (Plastic)



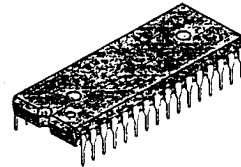
CXK584000YM
32 pin TSOP (Plastic)



CXK584000M
32 pin SOP (Plastic)



CXK584000P
32 pin DIP (Plastic)



Function

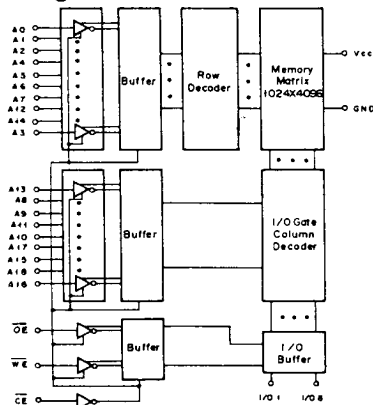
524288-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

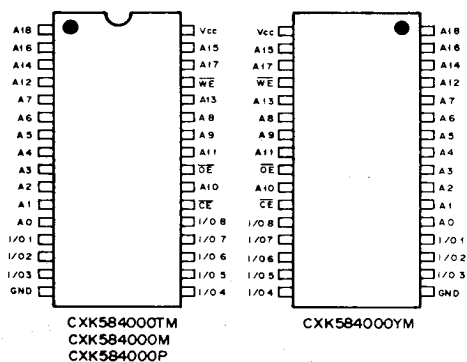
5

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A18	Address input
I/O1 to I/O8	Data input/output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	Power supply
GND	Ground

Absolute Maximum Ratings

(Ta=25 °C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to Vcc+0.5	V
Input and output voltage	V _{I/O}	-0.5 * to Vcc+0.5	V
Allowable power dissipation	P _d	CXK584000TM/YM/M	0.7
		CXK584000P	1.0
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	CXK584000TM/YM	235 • 10
		CXK584000M/P	260 • 10

* V_{IN}, V_{I/O} = -3.0V Min. for pulse width less than 50ns.

Truth Table

CE	OE	WE	Mode	I/O pin	Vcc current
H	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output disable	High Z	I _{CC1} , I _{CC2} , I _{CC3}
L	L	H	Read	Data out	I _{CC1} , I _{CC2} , I _{CC3}
L	x	L	Write	Data in	I _{CC1} , I _{CC2} , I _{CC3}

x : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70 °C, GND=0V)

Item	Symbol	Vcc=5V ± 10%			Vcc=2.7 to 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	Vcc	4.5	—	5.5	2.7	—	5.5	V
Input high voltage	V _{IH}	2.2	—	Vcc+0.3	2.2	—	Vcc+0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	-0.3 *	—	0.4	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics

(GND=0V, Ta=0 to +70 °C)

Item	Symbol	Test conditions		Vcc=5V ± 10%			Vcc=3V ± 10%			Unit	
				Min.	Typ. * 1	Max.	Min.	Typ. * 2	Max.		
Input leakage current	I _{LI}	V _{IN} =GND to Vcc		-1	—	1	-1	—	1	μA	
Output leakage current	I _{LO}	CE=V _{IH} or OE=V _{IH} or WE=V _{IL} V _{IO} =GND to Vcc		-1	—	1	-1	—	1	μA	
Operating power supply current	I _{CC1}	CE=V _{IL} , V _{IN} =V _{IH} or V _{IL} I _{OUT} =0mA		—	6	15	—	0.4	0.8	mA	
Average operating current	I _{CC2}	Min. cycle Duty=100% I _{OUT} =0mA		—	60	100	—	20	35	mA	
	I _{CC3}	Cycle time 1 μs Duty=100% I _{OUT} =0mA CE ≤ 0.2V, V _{IL} ≤ 0.2V, V _{IH} ≥ Vcc-0.2V		—	10	20	—	5	10	mA	
Standby current	I _{SB1}	CE ≥ Vcc-0.2V	L * 3	0 to +70 °C	—	—	100	—	—	74	μA
				0 to +40 °C	—	—	35	—	—	24	
				+25 °C	—	2	—	—	1	—	
			LL * 4	0 to +70 °C	—	—	50	—	—	22	
				0 to +40 °C	—	—	18	—	—	4.5	
				+25 °C	—	2	—	—	0.5	—	
	I _{SB2}	CE=V _{IH}	—	0.3	3	—	0.06	0.3	mA		
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	—	—	2.2	—	—	V		
Output low voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	—	—	0.4	V		

*1 Vcc=5V, Ta=25 °C

*2 Vcc=3V, Ta=25 °C

*3 Guaranteed for L-version (-55L/70L/85L/10L)

*4 Guaranteed for LL-version (-55LL/70LL/85LL/10LL)

I/O Capacitance

(Ta=25 °C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	8	pF

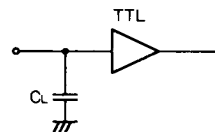
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

● AC test conditions

(V_{CC}=2.7 to 5.5V, Ta=0 to +70 °C)

Item		Conditions	
		V _{CC} =5V	V _{CC} =3V
Input pulse high level		V _{IH} =2.2V	V _{IH} =2.2V
Input pulse low level		V _{IL} =0.8V	V _{IL} =0.4V
Input rise time		tr=5ns	tr=5ns
Input fall time		tf=5ns	tf=5ns
Input and output reference level		1.5V	1.5V
Output load conditions	-70L/70LL -85L/85LL -10L/10LL	C _L * =100pF, 1TTL	C _L * =100pF, 1TTL
	-55L/55LL	C _L * =30pF, 1TTL	C _L * =30pF, 1TTL



* C_L includes scope and jig capacitances.

• Read cycle

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70 °C)

Item	Symbol	– 55L/55LL		– 70L/70LL		– 85L/85LL		– 10L/10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	trc	55	—	70	—	85	—	100	—	ns
Address access time	tAA	—	55	—	70	—	85	—	100	ns
Chip enable access time	tco	—	55	—	70	—	85	—	100	ns
Output enable to output valid	toE	—	30	—	40	—	45	—	50	ns
Output hold from address change	toH	10	—	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE}$)	tlz	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	tolz	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE}$)	thz *	0	20	0	25	0	30	0	35	ns
Output disable to output in high Z ($\overline{OE}$)	tohz *	0	20	0	25	0	30	0	35	ns

* thz and tohz are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• Write cycle

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70 °C)

Item	Symbol	– 55L/55LL		– 70L/70LL		– 85L/85LL		– 10L/10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	twc	55	—	70	—	85	—	100	—	ns
Address valid to end of write	tAW	50	—	60	—	70	—	80	—	ns
Chip enable to end of write	tcw	50	—	60	—	70	—	80	—	ns
Data to write time overlap	tdw	25	—	30	—	35	—	40	—	ns
Data hold from write time	tdH	0	—	0	—	0	—	0	—	ns
Write pulse width	tWP	40	—	50	—	60	—	70	—	ns
Address setup time	tAS	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	tWR	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	tWR1	0	—	0	—	0	—	0	—	ns
Output active from end of write	tOW	5	—	5	—	5	—	5	—	ns
Write to output in high Z	tWHZ *	0	20	0	25	0	30	0	30	ns

* tWHZ is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

• Read cycle

(V_{CC}=3V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	- 55L/55LL		- 70L/70LL		- 85L/85LL		- 10L/10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	110	—	140	—	170	—	200	—	ns
Address access time	t _{AA}	—	110	—	140	—	170	—	200	ns
Chip enable access time	t _{CO}	—	110	—	140	—	170	—	200	ns
Output enable to output valid	t _{OE}	—	60	—	80	—	90	—	100	ns
Output hold from address change	t _{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t _{LZ}	20	—	20	—	20	—	20	—	ns
Output enable to output in low Z ($\overline{OE}$)	t _{OLZ}	10	—	10	—	10	—	10	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t _{HZ} *	0	40	0	50	0	60	0	70	ns
Output disable to output in high Z ($\overline{OE}$)	t _{OHZ} *	0	40	0	50	0	60	0	70	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• Write cycle

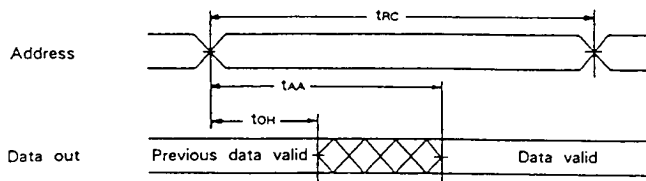
(V_{CC}=3V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	- 55L/55LL		- 70L/70LL		- 85L/85LL		- 10L/10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	110	—	140	—	170	—	200	—	ns
Address valid to end of write	t _{AW}	100	—	120	—	140	—	160	—	ns
Chip enable to end of write	t _{CW}	100	—	120	—	140	—	160	—	ns
Data to write time overlap	t _{DW}	50	—	60	—	70	—	80	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	80	—	100	—	120	—	140	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	t _{WRI}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	40	0	50	0	60	0	60	ns

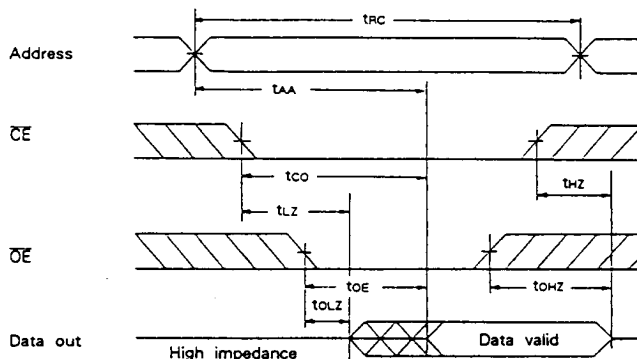
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

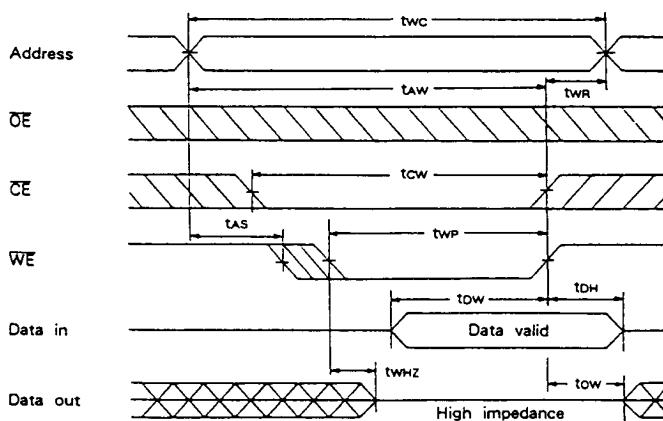
- Read cycle (1) : $\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$



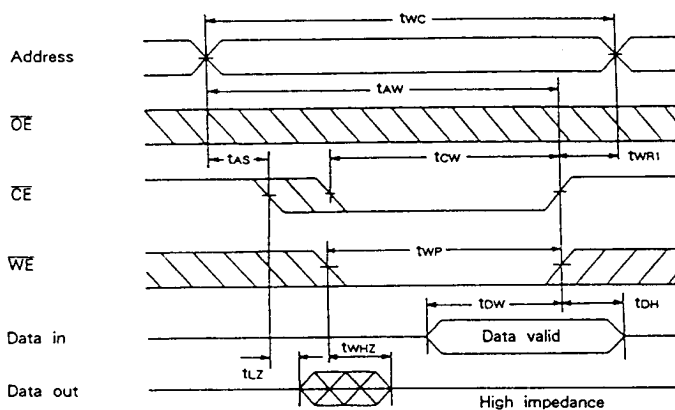
- Read cycle (2) : $\overline{WE}=V_{IH}$



- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



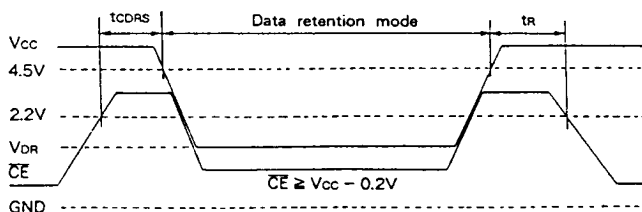
During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

($T_a = 0$ to 70°C)

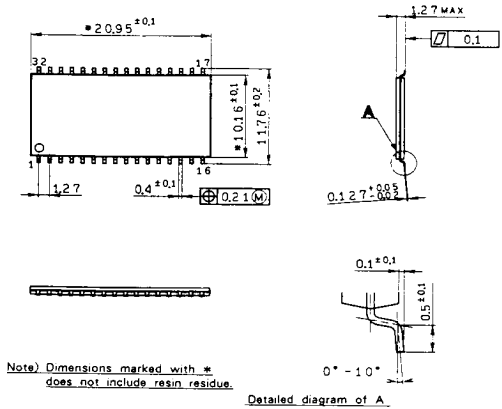
Item	Symbol	Test conditions		- 55L/70L/85L/10L			- 55LL/70LL/85LL/10LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.2\text{V}$		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0\text{V}$ $\overline{CE} \geq 2.8\text{V}$	0 to 70°C	—	—	50	—	—	15	μA
			0 to 40°C	—	—	15	—	—	3	
			25°C	—	1	—	—	0.5	—	
	I_{CCDR2}	$V_{CC} = 2.0$ to 5.5V $\overline{CE} \geq V_{CC} - 0.2\text{V}$		—	2	100	—	2	50	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			5	—	—	5	—	—	ms

Data retention waveform



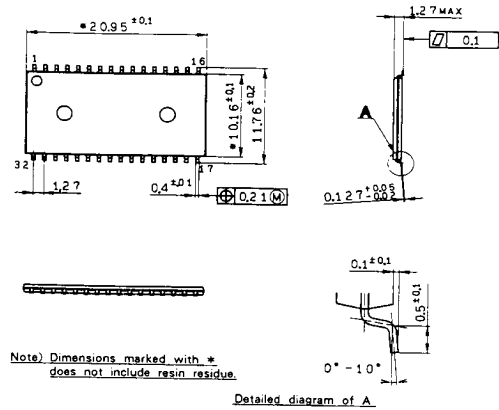
Package Outline Unit : mm

CXK584000TM 32pin TSOP (Plastic) 400mil



SONY NAME	TSOP(I)-32P-L01
EIAJ NAME	TSOP(I)032-P-0400-A
JEDEC CODE	

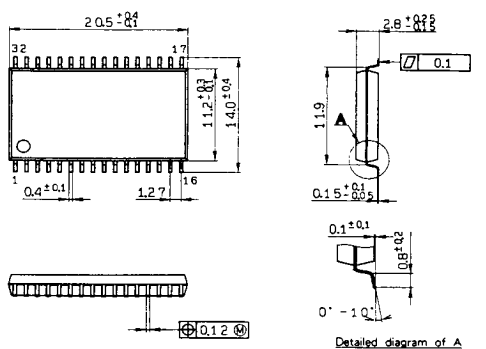
CXK584000YM 32pin TSOP (Plastic) 400mil



SONY NAME	TSOP(I)-32P-L01R
EIAJ NAME	TSOP(I)032-P-0400-B
JEDEC CODE	

CXK584000M

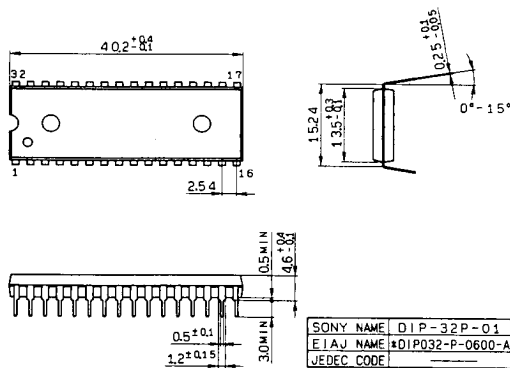
32pin SOP (Plastic) 525mil



SONY NAME	SOP-32P-L02
EIAJ NAME	*SOP032-P-0525-A
JEDEC CODE	

CXK584000P

32pin DIP (Plastic) 600mil 4.5g



SONY NAME	DIP-32P-01
EIAJ NAME	*DIP032-P-0600-A
JEDEC CODE	