# Am2864BE

## 8192 x 8-Bit Electrically Erasable PROM

Advanced Micro Devices

### DISTINCTIVE CHARACTERISTICS

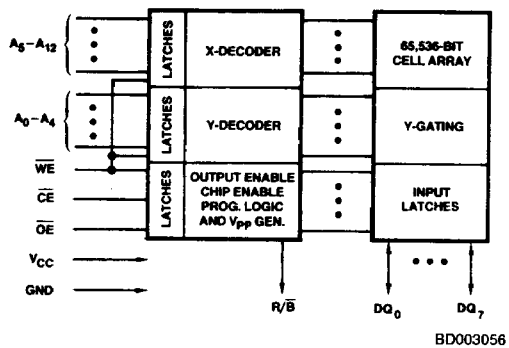
- 5-V only operation
- Military temperature range available
- Self-timed Write Cycle with on-chip latches
- Ready/$\overline{\text{Busy}}$ pin and $\overline{\text{Data}}$ Polling for end-of-write indication
- Allows $\overline{\text{WE}}$ and $\overline{\text{CE}}$ controlled Writes
- Data protection features to prevent writes from occurring during $V_{CC}$ power-up/down
- 32-byte page write mode
- Minimum endurance of 10,000 write cycles per byte with a 10-year retention. For detailed information, see the reliability section within this Handbook.

### GENERAL DESCRIPTION

The Am2864BE is a 65,536-bit Electrically Erasable Programmable Read-Only Memory (EEPROM) organized as 8192 words by 8 bits per word. It operates from a single 5-volt supply and has a fully self-timed write cycle with address, data, and control lines latched during the write operation. The 32-byte page write mode allows programming in as little as 2.6 seconds. The Am2864BE is fabricated on AMD's highly manufacturable N-Channel Silicon gate process, and uses AMD's proprietary EEPROM technology to achieve electrically alterable nonvolatile storage. This technology employs the industry-accepted Fowler-Nordheim tunneling across a thin oxide.

The Am2864BE provides the on-chip logic necessary to interface with most microprocessors. The latched inputs and self-timed write cycle free the microprocessor to perform other tasks during a write. A transparent automatic erase before write enhances system performance.

### BLOCK DIAGRAM




### MODE SELECT TABLE

| Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | R/$\overline{B}$ | I/O | $A_9$ | Mode |
| L | L | H | Hi Z | Data Out | X | Read |
| L | H | ⊓ | Hi Z | Data In | X | Write |
| ⊓ | H | L | Hi Z | Data In | X | Write |
| H | X | X | Hi Z | Hi Z | X | Standby |
| L | H | H | Hi Z | Hi Z | X | Read Inhibit |
| X | L | X | – | – | X | Write Inhibit |
| L | L | H | Hi Z | Code | $V_H$ | Auto Select |
| L | L | H | L | $\overline{D_{in}}$ | X | $\overline{\text{Data}}$ Polling |

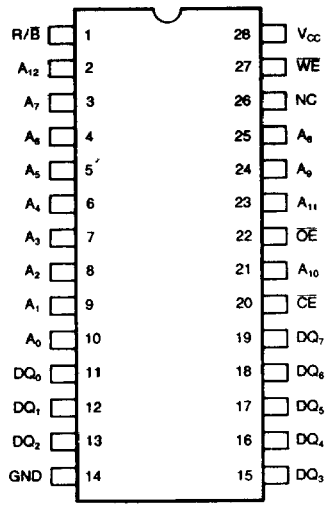
$V_H$ = 12.0 V ± .5 V
H = HIGH
L = LOW
X = Don't Care
⊓ = Pulse

### PRODUCT SELECTOR GUIDE

| Part Number | Am2864BE-205 | Am2864BE-200 | Am2864BE-255 | Am2864BE-250 | Am2864BE-305 | Am2864BE-300 | Am2864BE-355 | Am2864BE-350 |
|---|---|---|---|---|---|---|---|---|
| Maximum Access Time | 200 ns | | 250 ns | | 300 ns | | 350 ns | |
| $V_{CC}$ Supply Tolerance | ±5% | ±10% | ±5% | ±10% | ±5% | ±10% | ±5% | ±10% |

## CONNECTION DIAGRAMS
### Top View

**DIP**

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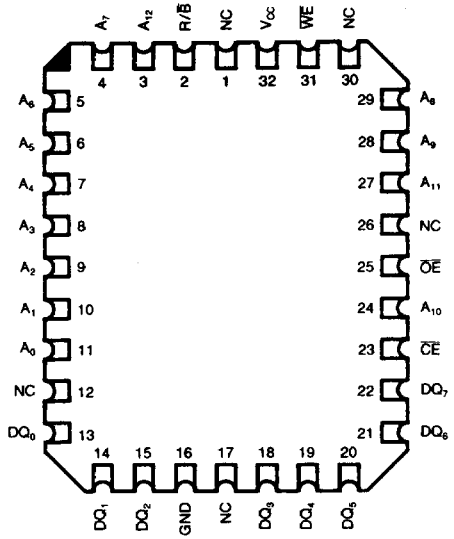
**LCC**

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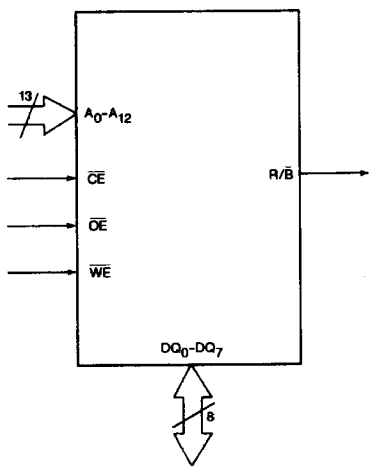
## LOGIC SYMBOL

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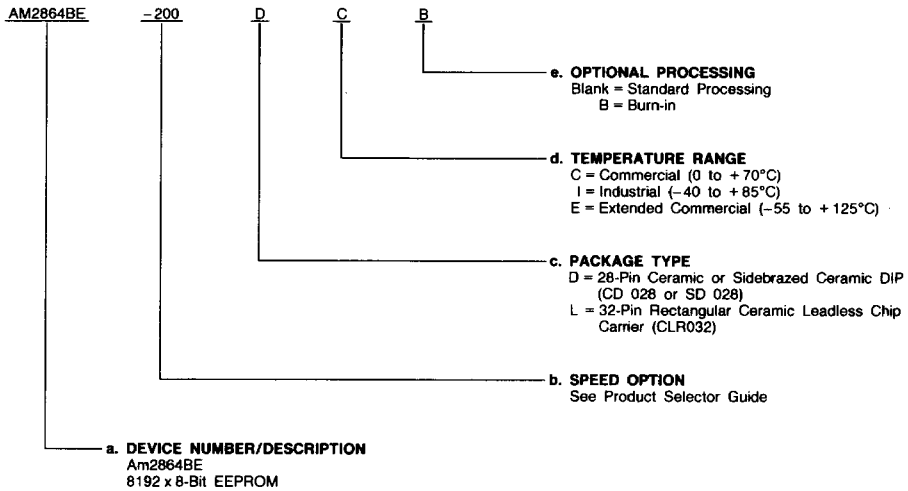
$A_0 - A_{12}$ = Address Pins
$\overline{CE}$ = Chip Enable
$DQ_0 - DQ_7$ = Data Pins
GND = Ground
$\overline{OE}$ = Output Enable
$R/\overline{B}$ = Ready/Busy
$V_{CC}$ = Power Supply
$\overline{WE}$ = Write Enable
NC = No Connect

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

**a. Device Number**
**b. Speed Option**
**c. Package Type**
**d. Temperature Range**
**e. Optional Processing**




| Valid Combinations | |
|---|---|
| AM2864BE-205 | DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB |
| AM2864BE-200 | |
| AM2864BE-255 | |
| AM2864BE-250 | |
| AM2864BE-305 | |
| AM2864BE-300 | |
| AM2864BE-355 | |
| AM2864BE-350 | |

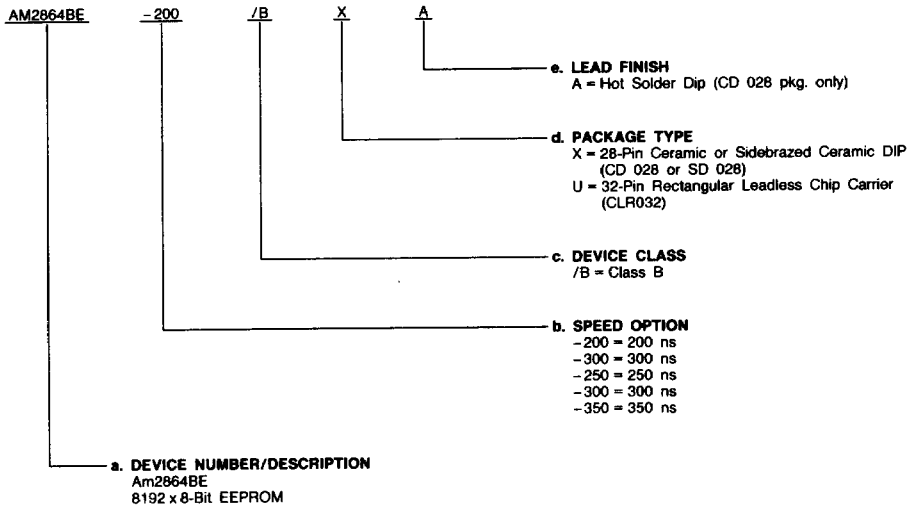
**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
**b. Speed Option**
**c. Device Class**
**d. Package Type**
**e. Lead Finish**




| Valid Combinations | |
|---|---|
| AM2864BE-200 | /BXA, /BUA |
| AM2864BE-250 | |
| AM2864BE-300 | |
| AM2864BE-350 | |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

**Group A Tests**

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## FUNCTIONAL DESCRIPTION

### Read Mode

The Am2864BE has two control functions which must both be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs $t_{OE}$ after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC}$-$t_{OE}$.

### Standby Mode

The Am2864BE has a standby mode which reduces the active power dissipation by 50%, from 735 mW to 368 mW ($V_{CC}$ ±5%). The Am2864BE is placed in the standby mode by applying a TTL HIGH signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

### Data Protection

The Am2864BE incorporates several features that prevent unwanted write cycles during $V_{CC}$ power-up and power-down. These features protect the integrity of the stored data.

To avoid the initiation of a write cycle during $V_{CC}$ power-up and power-down, a write cycle is locked out for $V_{CC}$ less than 3.0 volts (typical 3.3 V). It is the users's responsibility to ensure that the control levels are logically correct when $V_{CC}$ is above 3.0 volts.

There is a $\overline{WE}$ lockout circuit that prevents $\overline{WE}$ pulses of less than 20 ns duration from initiating a write cycle.

When the $\overline{OE}$ control is in logic zero condition, a write cycle cannot be initiated.

### Write Cycle Control Pins

For system design simplification, the Am2864BE is designed in such a way that either $\overline{CE}$ or $\overline{WE}$ can be used to initiate a write cycle. During a system write cycle, the address is latched into the internal address latches upon the last falling edge of $\overline{WE}$ or $\overline{CE}$ providing that $\overline{OE}$ is a logic "1". The first rising edge of $\overline{WE}$ or $\overline{CE}$ latches the data into the data latches. All setup and hold times are with respect to the $\overline{WE}$ signal.

To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this functional description.

### Page Write Mode

The page write allows from 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. The page write mode consists of a load sequence followed by an automatic write sequence.

During the load portion, sequential $\overline{WE}$ pulses load the byte address and the byte data into a 32-byte register. The bytes can be loaded into this register in any order. On each $\overline{WE}$ pulse, the "Y" address is latched on the falling edge of $\overline{WE}$, the data input is latched on the rising edge of $\overline{WE}$, and the page address ($A_5$-$A_{12}$) is latched on the falling edge of the last $\overline{WE}$. Note that in order for a write to occur, $\overline{CE}$ and $\overline{WE}$ must be LOW and $\overline{OE}$ must be HIGH. The load portion of the page write is complete when all the data (up to 32 bytes) is loaded into the register.

The automatic write portion starts $t_{WW}$ after each transition of $\overline{WE}$ from LOW-to-HIGH. If $\overline{WE}$ transitions from HIGH-to-LOW before $t_{WW}$ minimum (100 µs), the timer is reset and the automatic write portion does not start. This is how the bytes are loaded into the register. If $\overline{WE}$ is held LOW, this $t_{WW}$ timer never starts and the write cycle is held indefinitely.

When a write pulse is not given to the device within the $t_{WW}$ minimum time (100 µs) from the rising edge of the previous write pulse, the automatic write sequence is initiated. At completion of the automatic write sequence ($t_{WB}$ maximum time has elapsed, or $\overline{Data}$ Polling or R/$\overline{B}$ indicates the write operation is complete), at least one of the control pins must deselect the device from accidental writes ($\overline{OE}$ LOW, $\overline{CE}$ HIGH, or $\overline{WE}$ HIGH).

The automatic write sequence consists of an erase cycle, which erases any data that existed in each addressed cell; and a write cycle, which puts data back into the erased cells. Note that a page write will only write data to the locations being addressed and will not rewrite the entire page. The Ready/$\overline{Busy}$ pin (R/$\overline{B}$) goes to a logic LOW level during the automatic write sequence. This could signal a microprocessor host that the system bus is free for other activity. When R/$\overline{B}$ transitions to a HIGH state, the Am2864BE has completed writing and is ready to accept another cycle.

### Byte Mode Write

When $\overline{WE}$ is toggled once, the Am2864BE operates in the byte mode. A single byte is loaded into the register, and after $\overline{WE}$ goes HIGH, and $t_{WW}$ is satisfied, the automatic write cycle starts. It is in this mode that the Am2864BE is similar to the Am9864.

### Auto Select Mode

The auto select mode allows the reading out of a binary code from an EEPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional at 25°C ±5°C ambient temperature.

To activate this mode, programming equipment must force 11.5 V to 12.5 V on address line $A_9$ of the Am2864BE. Two identifier bytes may then be sequenced from the device outputs by toggling address line $A_0$ from $V_{IL}$ to $V_{IH}$. All other address lines must be held at $V_{IL}$ during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am2864BE, these two identifier bytes are given in Table 1. All identifiers for manufacturer and device codes will possess odd parity, with the MSB ($O_7$) defined as the parity bit.

### Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and be connected to the read line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### Ready/$\overline{\text{Busy}}$ Pin

The Ready/$\overline{\text{Busy}}$ ($R/\overline{B}$) pin is an open-drain output which allows two or more $R/\overline{B}$ signals to be OR-tied together. The value of the pullup resistor required is as follows:

$$R_{pu} = \frac{4.6 \text{ volts}}{2.1 \text{ mA} - I_{IL}}$$

$I_{IL}$ = total $V_{IL}$ input current of devices connected to $R/\overline{B}$

A typical pullup resistor value for $R/\overline{B}$ is 3 kΩ, assuming $I_{IL}$ is less than 0.5 mA.

### $\overline{\text{Data}}$ Polling

$\overline{\text{Data}}$ Polling makes the Am2864BE highly flexible. It allows the designer the option of a software polling technique as well as the hardware interrupt Ready/$\overline{\text{Busy}}$ technique for end-of-write indication. $\overline{\text{Data}}$ Polling requires a simple software routine that performs a read operation when the chip is in the automatic write mode. The data that becomes valid during this $\overline{\text{Data}}$ Polling read is the inverse of all 8 bits last written to the outputs. The true data ($DQ_0 - DQ_7$) will become valid when the automatic write has been completed. Note that all 8 bits invert during $\overline{\text{Data}}$ Polling, thereby giving the user more flexibility during design and layout.

### Chip Clear Mode (Military only)

Another feature included on AMD's Am2864BE for military applications is a single-pulse chip erase. This optional mode allows the user to program all bits to a logic ONE with a single 10-ms write. Additional information is available from AMD regarding this test mode — consult the local AMD sales office.

### Endurance

Since endurance testing is a destructive test, it is sampled and not 100% tested. To test for endurance, a sample of devices are written 10,000 times and checked for data retention capability.

There is one main failure mechanism associated with endurance failures in EEPROMs. This failure mechanism is due to charge trapping in the thin tunneling dielectric. At a point when the amount of trapped charge creates an electric field that exceeds the dielectric breakdown of the oxide, the oxide becomes conductive and reliable storage of charge on the floating gate is no longer possible. This results in the failure of a single bit to properly write and retain data.

There are three different failure rates associated with this failure mechanism, and the failure rates are a function of the number of write cycles. For less than a few hundred write cycles, the failure rate is relatively high. During AMD testing, each part is written hundreds of times to allow those cells that would be infant-mortality failures to be screened out. For the next 20,000 to 30,000 write cycles the failure rate is low. It is in this region that AMD EEPROMs are operated. Somewhere above this region, typically well above the guarantee of $10^4$ total write cycles, the failure rate again starts increasing.

The endurance failure rate is a function of the number of write cycles that the part has experienced. All parts that pass the AMD test screens will write a minimum of 10,000 times and retain data for a period of ten years at every byte location with a maximum failure rate of 5%. In other words, 5% (maximum) of a sample of devices will fail to write or to retain information after write if they are written 10,000 times. Those devices that fail will typically have a single bit that fails to retain the correct data after being written. This failure rate is measured from a sample of devices, in the same manner that other reliability failure mechanisms are measured.

For more detailed information on how this data was obtained, please refer to the reliability section within this Handbook.

## APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1-μF ceramic capacitor (high-frequency, low inherent inductance) should be used on each device between $V_{CC}$ and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EEPROM arrays, a 4.7-μF bulk electrolytic capacitor should be used between $V_{CC}$ and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

## PROGRAMMING

**TABLE 1. IDENTIFIER BYTES** (Notes 1, 2 & 3)

| Identifier | $A_0$ | $DQ_7$ | $DQ_6$ | $DQ_5$ | $DQ_4$ | $DQ_3$ | $DQ_2$ | $DQ_1$ | $DQ_0$ | Hex |
|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer Code | $V_{IL}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| Device Code | $V_{IH}$ | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 8A |

Legend: 1 = HIGH
0 = LOW

Notes: 1. $A_9 = 12.0 \text{ V} \pm 0.5 \text{ V}$
2. $A_1 - A_8$, $A_{10} - A_{12}$, $\overline{CE}$, $\overline{OE} = V_{IL}$
3. $\overline{WE} = V_{IH}$

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied . −65 to +135°C
Voltage on All Inputs with Respect to GND ..... +6.50 to −0.6 V
Voltage on $A_9$ with Respect to GND ..... +13.5 to −0.6 V

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ($T_C$) ..... 0 to +70°C
Supply Voltage ($V_{CC}$ ±5%) ..... +4.75 to +5.25 V
($V_{CC}$ ±10%) ..... +4.50 to +5.50 V
Industrial (I) Devices
Temperature ($T_C$) ..... −40 to +85°C
Supply Voltage ($V_{CC}$ ±5%) ..... +4.75 to +5.25 V
($V_{CC}$ ±10%) ..... +4.50 to +5.50 V
Extended Commercial (E) and Military (M) Devices
Temperature ($T_C$) ..... −55 to +125°C
Supply Voltage ($V_{CC}$ ±10%) ..... +4.50 to +5.50 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

**DC CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

| Parameter Symbol | Parameter Description | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = 0 and 5.5 V | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0 and 5.5 V | | | 10 | µA |
| $I_{CC1}$ | $V_{CC}$ Current (Standby) | $\overline{CE}$ = $V_{IH}$, $\overline{OE}$ = $V_{IL}$ | | | 70 | mA |
| $I_{CC2}$ | $V_{CC}$ Current (Active) | $\overline{OE}$ = $\overline{CE}$ = $V_{IL}$ | | | 140 | mA |
| $V_{IL}$ | Input LOW Voltage | | −1.0 | | .8 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | $V_{CC}$+1 | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 2.1 mA | | | .45 | V |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −400 µA | 2.4 | | | V |
| $V_{RB}$ | R/$\overline{B}$ Output LOW | $I_{RB}$ = 2.1 mA | | | .45 | V |
| $C_{IN}$ | Input Capacitance (Note 1, 2) | $V_{IN}$ = 0 V | | 4 | 8 | pF |
| $C_{OUT}$ | Output Capacitance (Note 1, 2) | $\overline{OE}$ = $\overline{CE}$ = $V_{IH}$, $V_{OUT}$ = 0 V | | 8 | 10 | pF |
| $V_{WI}$ | Write Inhibit Voltage | | 3.0 | 3.3 | | V |

Notes: 1. This parameter is measured only for the initial qualification and after process or design changes which affect capacitance.
2. Freq. = 1 MHz @ 25°C.
3. Typical values are for nominal supply voltages.

3

**SWITCHING CHARACTERISTICS** over operating ranges (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

| No. | Parameter Symbol | Parameter Description | Test Condition | Am2864BE-205, Am2864BE-200 | | Am2864BE-255, Am2864BE-250 | | Am2864BE-305, Am2864BE-300 | | Am2864BE355, Am2864BE-350 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **READ** | | | | | | | | | | | | |
| 1 | $t_{ACC}$ | Address to Output Delay | $\overline{CE} = \overline{OE} = V_{IL}$ | | 200 | | 250 | | 300 | | 350 | ns |
| 2 | $t_{CE}$ | $\overline{CE}$ to Output Delay | $\overline{OE} = V_{IL}$ | | 200 | | 250 | | 300 | | 350 | ns |
| 3 | $t_{OE}$ | Output Enable to Output Delay | $\overline{CE} = V_{IL}$ | | 90 | | 90 | | 110 | | 120 | ns |
| 4 | $t_{DF}$ (Note 1) | Output Enable or Chip Enable HIGH to Output Float | | 10 | 60 | 10 | 60 | 10 | 70 | 10 | 80 | ns |
| 5 | $t_{OH}$ (Note 1) | Output Hold from Address Change | $\overline{CE} = \overline{OE} = V_{IL}$ | 20 | | 20 | | 20 | | 20 | | ns |
| 6 | $t_{RC}$ | Read Cycle Time | | 200 | | 250 | | 300 | | 350 | | ns |
| 7 | $t_{DA}$ (Note 1) | Output Enable or Chip Enable LOW to Output Active | | 10 | | 10 | | 10 | | 10 | | ns |
| **WRITE** | | | | | | | | | | | | |
| 8 | $t_{AS}$ | Address to Write Setup Time | | 10 | | 10 | | 10 | | 20 | | ns |
| 9 | $t_{CS}$ | $\overline{CE}$ to Write Setup Time | | 0 | | 0 | | 0 | | 0 | | ns |
| 10 | $t_{WP}$ | $\overline{WE}$ or $\overline{CE}$ Write Pulse Width | | 150 | | 150 | | 150 | | 200 | | ns |
| 11 | $t_{AH}$ | Address Hold Time | | 80 | | 80 | | 80 | | 100 | | ns |
| 12 | $t_{DS}$ | Data Setup Time | | 100 | | 100 | | 100 | | 120 | | ns |
| 13 | $t_{DH}$ | Data Hold Time | | 20 | | 20 | | 20 | | 30 | | ns |
| 14 | $t_{CH}$ | $\overline{CE}$ Hold Time | | 0 | | 0 | | 0 | | 0 | | ns |
| 15 | $t_{OES}$ | $\overline{OE}$ Setup Time | | 10 | | 10 | | 10 | | 10 | | ns |
| 16 | $t_{OEH}$ | $\overline{OE}$ Hold Time | | 10 | | 10 | | 10 | | 10 | | ns |
| 17 | $t_{DB}$ | Time to Device Busy | | | 100 | | 100 | | 100 | | 100 | ns |
| 18 | $t_{WC}$ | Byte Load Cycle Time | | 1 | | 1 | | 1 | | 1 | | µs |
| 19 | $t_{WW}$ | Page Write Window (Note 3) | | 100 | | 100 | | 100 | | 100 | | µs |
| 20 | $t_{WH}$ | $\overline{WE}$ or $\overline{CE}$ Write Pulse HIGH Time | | 50 | | 50 | | 50 | | 100 | | ns |
| 21 | $t_{WB}$ | Byte or Page Write Cycle Time (Note 4) | | | 10 | | 10 | | 10 | | 10 | ms |
| 22 | $t_{WPH}$ | Write Deselect Hold Time (Note 5) | | 10 | | 10 | | 10 | | 10 | | ns |
| 23 | (Notes 1 & 2) | Number of Writes per Byte | | 10 | | 10 | | 10 | | 10 | | x1000 |

Notes: 1. This parameter is measured only at the initial qualification and after process or design changes which affect the parameter.
2. See Reliability Section within this HANDBOOK.
3. A timer of $t_{WW}$ duration starts at every LOW-to-HIGH transition of $\overline{WE}$. If it is allowed to time out, a page write will start. A transition of $\overline{WE}$ from HIGH-to-LOW will stop the timer.
4. When $t_{WB}$ maximum time has elapsed or Data Polling (or R/$\overline{B}$) indicates the write operation is complete, at least one of the control pins must deselect the device ($\overline{WE}$ or $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IL}$). Once the write cycle is complete, the device is available for the next operation.
5. This is the time from deselecting the device ($\overline{WE}$ or $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IL}$) to the other control pins being a don't care.

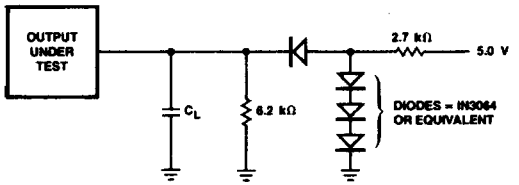
## SWITCHING TEST CIRCUIT

### Switching Test Conditions

Output load: 1 TTL gate and $C_L = 100$ pF
Input pulse levels: 0.45 V to 2.4 V

### Timing Measurement Reference Levels

Input: 0.8 V and 2.0 V
Output: 0.8 V and 2.0 V

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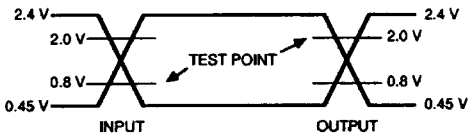
$C_L = 100$ pF, including jig capacitance.

## SWITCHING TEST WAVEFORM

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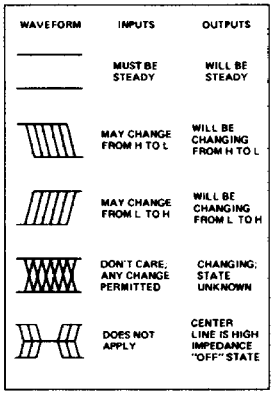
AC Testing: Inputs are driven at 2.4 V for logic "1" and 0.45 V for logic "0". Timing measurements are made at 0.8 V and 2.0 V. Input pulse rise and fall times are 10 ns.

## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

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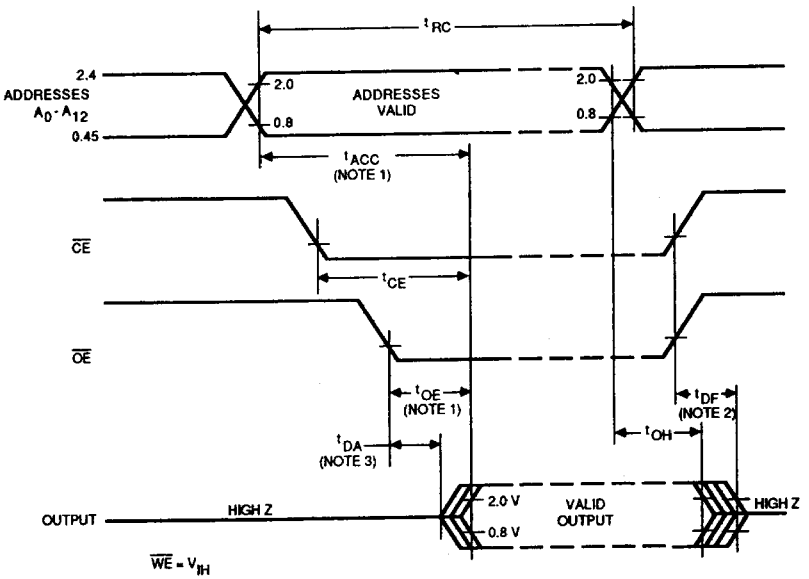
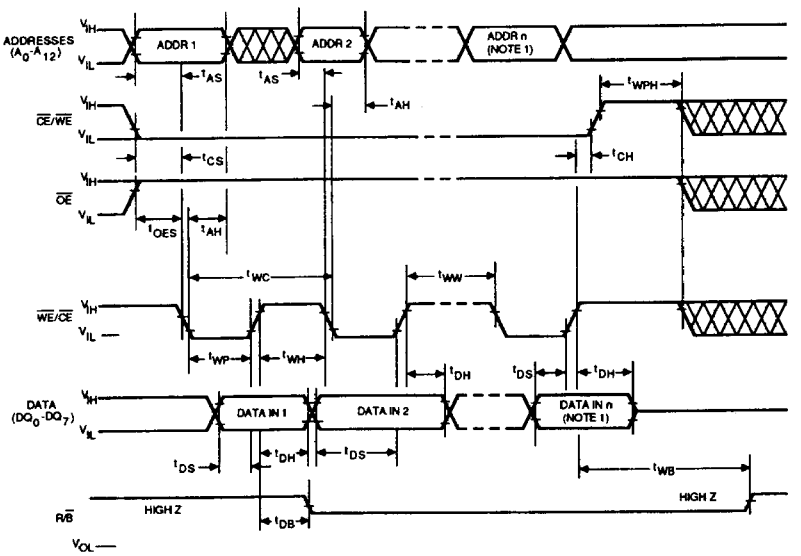
3

## SWITCHING WAVEFORMS (Cont'd.)




**Read**

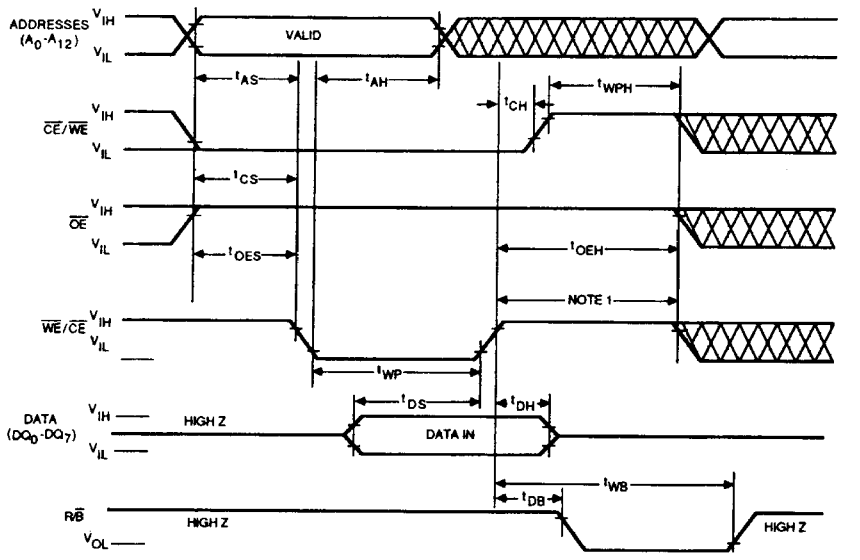
Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC}$-$t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{ACC}$.
2. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
3. $t_{DA}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs last.




**Page Write**

Notes: 1. $n \leq 32$.

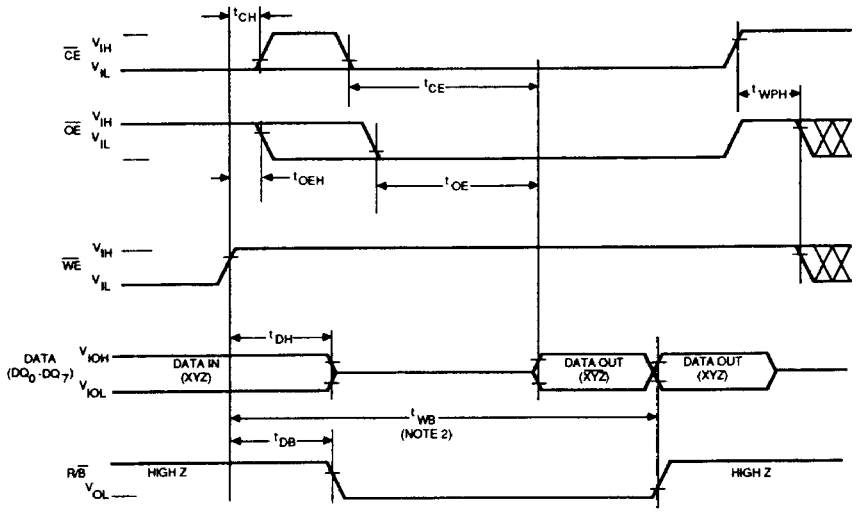
## SWITCHING WAVEFORMS (Cont'd.)




WF025172

**Byte Write**

Notes: 1. This time period = $t_{CH} + t_{RISE} + t_{WPH}$.




WF025190

**$\overline{\text{Data}}$ Polling**

Notes: 1. This is shown for single byte write. In page write, R/$\overline{B}$ goes LOW on first LOW-to-HIGH transition of $\overline{WE}$.

2. When the Write cycle is completed (R/$\overline{B}$ is HIGH or data out TRUE), the user must meet one of the following conditions to prevent an accidental write: $\overline{OE}$ LOW, $\overline{CE}$ HIGH, or $\overline{WE}$ HIGH.