TRANSCEIVERS

Marvell Solutions

88E3015/88E3018 Datasheet

Integrated 10/100 Fast Ethernet Transceiver

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Document Status	
Advance Information	This document contains design specifications for initial product development. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
Preliminary Information	This document contains preliminary data, and a revision of this document will be published at a later date. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
Final Information	This document contains specifications on a product that is in final release. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
Revision Code: Rev. C	
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Overview

The Marvell® 88E3015/88E3018 devices are the fourth generation Marvell® DSP-based physical layer transceivers for Fast Ethernet applications. The devices contain all the active circuitry to convert data streams to and from a Media Access Controller (MAC) and the physical media. The 88E3015/88E3018 devices incorporate IEEE 802.3u Auto-Negotiation in support of both 100BASE-TX and 10BASE-T networks over twisted-pair cable in full-duplex or half-duplex mode.

The 88E3015/88E3018 devices both support the Reduced Gigabit Media Independent Interface (RGMII), and the Media Independent Interface (MII).

The 88E3015/88E3018 devices feature a mode of operation supporting IEEE compliant 100BASE-FX fiber-optic networks. Additionally, the 88E3015/88E3018 devices implement Far-End Fault Indication (FEFI) in order to provide a mechanism for transferring information from the local station to the link partner that indicates a remote fault has occurred in 100BASE-FX mode.

The 88E3015/88E3018 devices feature the Marvell Virtual Cable Tester® (VCT™) technology, which enables IT managers and networking equipment manufacturers to remotely analyze the quality and characteristics of the attached cable plant.

The 88E3015/88E3018 devices use advanced mixed-signal processing and power management techniques for extremely low power dissipation and high port count system integration. The 88E3015/88E3018 devices are manufactured in an all CMOS process.

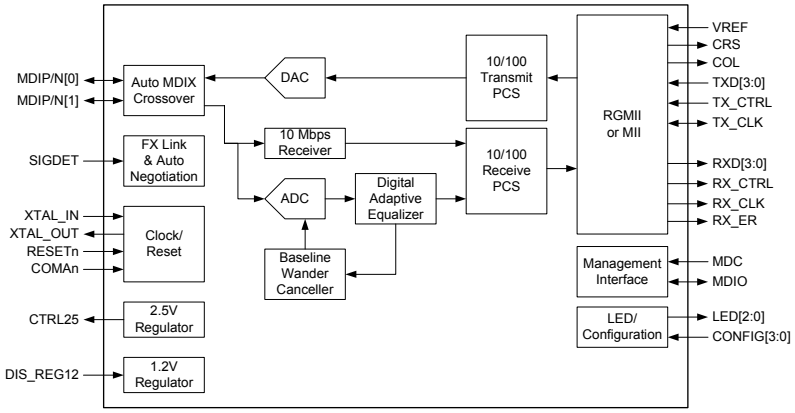
88E3015/88E3018 Specific Features

The 88E3018 device, housed in a 64-pin QFN package, offers a pin-upgradeable path toward future Gigabit Ethernet PHY designs. The 88E3018 device includes support for IEEE 1149.1 JTAG Standard Test Access Port and Boundary Scan. The 88E3108 device is available in Industrial grade (RoHS 6/6 compliant package only)

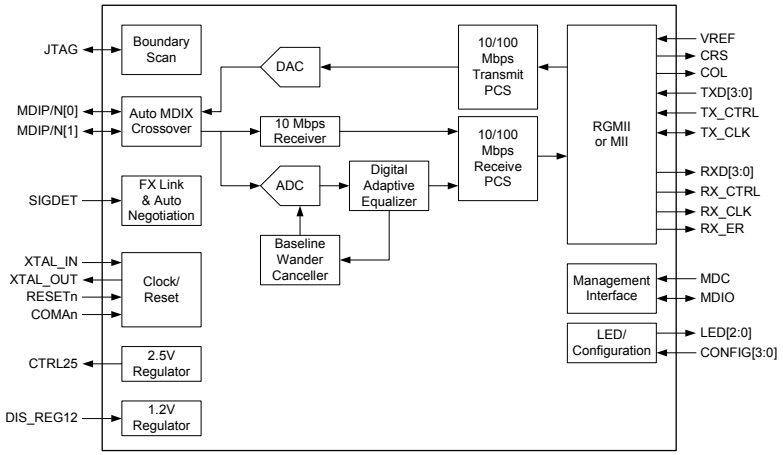
The 88E3015 device, housed in a 56-pin QFN package, provides a cost-efficient, increased board savings option to the 88E3018.

Features

- IEEE 802.3 compliant 100BASE-TX and 10BASE-T ports
- Reduced Gigabit Media Independent Interface (RGMII)
- Media Independent Interface (MII) support
- Source Synchronous MII support
- Virtual Cable Tester® (VCT™) Technology
- PECL interface supporting 100BASE-FX applications
- Automatic MDI/MDIX crossover for 10BASE-T and 100BASE-TX
- Jumbo frame support to 10 Kbytes with up to ±150 ppm clock frequency difference
- IEEE 802.3u Auto-Negotiation support for automatic speed and duplex selection
- Far-End Fault Indication (FEFI) support for 100BASE-FX applications
- Supports 802.3ah Unidirectional Enable
- Energy detect feature
- Baseline wander correction
- Auto-Calibration for MAC Interface outputs
- COMA Mode support
- Flexible serial management interface (MDC/MDIO) for register access
- Programmable interrupt to minimize polling
- IEEE 1149.1 Standard Test Access Port and boundary scan compatible (88E3018 only)
- Supports three (3) LEDs per port
- 0.15 µm standard digital CMOS process
- 56-pin QFN 8 mm x 8 mm package (88E3015 device)
- 64-pin QFN 9 mm x 9 mm package (88E3018 device)
- Available in Industrial grade (88E3018 device, RoHS 6/6 package only)



88E3015 Device Functional Block Diagram



88E3018 Device Functional Block Diagram

Table 1: 88E3015/88E3018 Devices Feature Differences

	88E3015	88E3018
Package	56-pin QFN	64-pin QFN
MII	Yes	Yes
RGMII	Yes	Yes
Virtual Cable Tester®	Yes	Yes
Fiber Support	Yes	Yes
Parallel LEDs	Yes	Yes
Power Management	Yes	Yes
JTAG Support	No	Yes
Industrial Grade	No	RoHS 6/6 Package Only

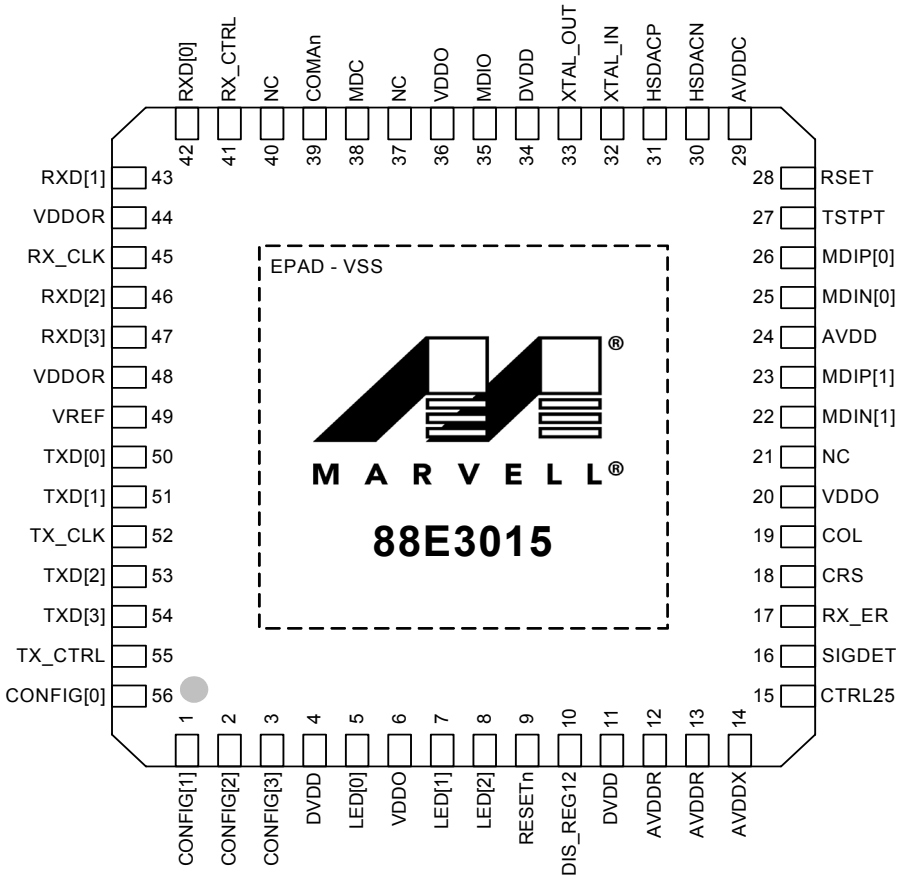
Table of Contents

Section 1. Signal Description

1.1 88E3015 Device 56-Pin QFN Pinout

The 88E3015 is manufactured in a 56-pin QFN.

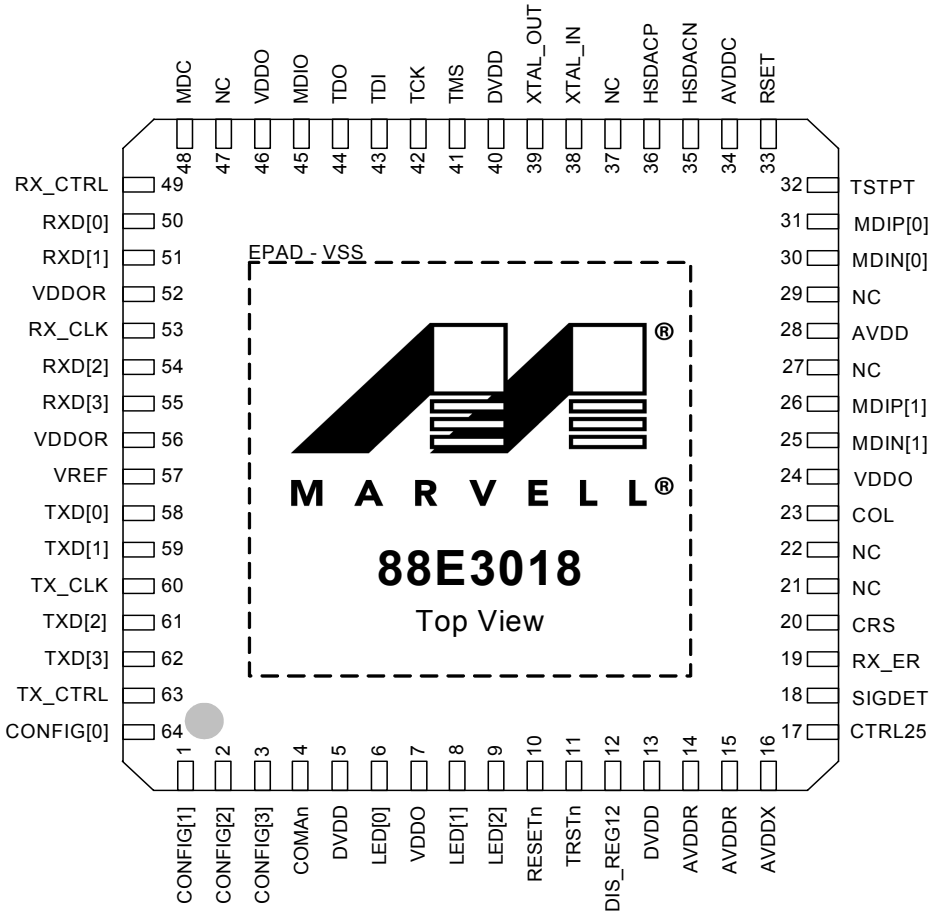
Figure 1: 88E3015 Integrated 10BASE-T/100BASE-TX Fast Ethernet Transceiver 56-Pin QFN Package



1.2 88E3018 Device 64-Pin QFN Pinout

The 88E3018 is manufactured in a 64-pin QFN.

Figure 2: 88E3018 Integrated 10BASE-T/100BASE-TX Fast Ethernet Transceiver 64-Pin QFN Package



1.3 Pin Description

1.3.1 Pin Type Definitions

Pin Type	Definition
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull up
PD	Internal pull down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

Table 2: RGMII Interface

88E3015	88E3018	Pin Name	Type	Description
52	60	TX_CLK/TXC	I	RGMII Transmit Clock provides a 25 MHz or 2.5 MHz reference clock with ± 50 ppm tolerance depending on speed. In RGMII mode, TX_CLK is used as TXC.
55	63	TX_CTRL/TX_CTL	I	RGMII Transmit Control. TX_EN is presented on the rising edge of TX_CLK. In RGMII mode, TX_CTRL is used as TX_CTL. A logical derivative of TX_EN and TX_ER is presented on the falling edge of TX_CLK.
54 53 51 50	62 61 59 58	TXD[3]/TD[3] TXD[2]/TD[2] TXD[1]/TD[1] TXD[0]/TD[0]	I	RGMII Transmit Data. In RGMII mode, TXD[3:0] are used as TD[3:0]. The transmit data nibble is presented on TXD[3:0] on the rising edge of TX_CLK.
45	53	RX_CLK/RXC	O	RGMII Receive Clock provides a 25 MHz or 2.5 MHz reference clock with ± 50 ppm tolerance derived from the received data stream depending on speed. In RGMII mode, RX_CLK is used as RXC.
41	49	RX_CTRL/ RX_CTL	O	RGMII Receive Control. RX_DV is presented on the rising edge of RX_CLK. In RGMII mode, RX_CTRL is used as RX_CTL. A logical derivative of RX_DV and RX_ER is presented on the falling edge of RX_CLK.
47 46 43 42	55 54 51 50	RXD[3]/RD[3] RXD[2]/RD[2] RXD[1]/RD[1] RXD[0]/RD[0]	O	RGMII Receive Data. In RGMII mode, RXD[3:0] are used as RD[3:0]. The receive data nibble is presented on RXD[3:0] on the rising edge of RX_CLK.

Table 3: MII Interface

88E3015	88E3018	Pin Name	Type	Description
52	60	TX_CLK	I/O, Z	MII Transmit Clock. TX_CLK provides a 25 MHz and 2.5 MHz clock reference for TX_CTRL, TX_ER, and TXD[3:0], depending on the speed. TX_CLK is an output when in normal MII mode, and is an input in source synchronous MII mode.
54 53 51 50	62 61 59 58	TXD[3] TXD[2] TXD[1] TXD[0]	I	MII Transmit Data. TXD[3:0] presents the data nibble to be transmitted onto the cable. TXD[3:0] is synchronous to TX_CLK.
55	63	TX_CTRL/TX_EN		MII Transmit Enable. In MII mode, TX_CTRL is used as TX_EN. When TX_CTRL is asserted, data on TXD[3:0] along with TX_ER is encoded and transmitted onto the cable. TX_EN is synchronous to TX_CLK.
45	53	RX_CLK	O, Z	MII Receive Clock. RX_CLK provides a 25 MHz and 2.5 MHz clock reference for RX_CTRL, RX_ER, and RXD[3:0] depending on the speed.
47 46 43 42	55 54 51 50	RXD[3] RXD[2] RXD[1] RXD[0]	O, Z	MII Receive Data. Symbols received on the cable are decoded and presented on RXD[3:0]. RXD[3:0] is synchronous to RX_CLK.
41	49	RX_CTRL/RX_DV		MII Receive Data Valid. Data received on the cable is decoded and presented on RXD[3:0] and RX_ER. In MII mode, RX_CTRL is used as RX_DV. RX_CTRL is synchronous to RX_CLK.
17	19	RX_ER	I/O, Z	MII Receive Error. When RX_ER and RX_CTRL are both asserted, the signals indicate an error symbol is detected on the cable. When RX_ER is asserted with RX_CTRL de-asserted, a false carrier is detected on the cable. RX_ER is synchronous to RX_CLK.

Table 3: MII Interface (Continued)

88E3015	88E3018	Pin Name	Type	Description
18	20	CRS	O, Z	MII Carrier Sense. CRS asserts when the receive medium is non-idle. CRS is asynchronous to RX_CLK, and TX_CLK.
19	23	COL	O, Z	MII Collision. In full-duplex modes, COL is always low. In 10BASE-T/100BASE-TX half-duplex modes, COL asserts only when both the transmit and receive media are non-idle. In 10BASE-T half-duplex mode, COL is asserted to indicate signal quality error (SQE). Disable SQE by clearing register 16.2 to zero. COL is asynchronous to RX_CLK, and TX_CLK.

Table 4: Network Interface

88E3015	88E3018	Pin Name	Type	Description
26 25	31 30	MDIP[0] MDIN[0]	I/O	Media Dependent Interface[0]. In MDI configuration, MDI[0]± is used for the transmit pair. In MDIX configuration, MDI[0]± is used for the receive pair.
23 22	26 25	MDIP[1] MDIN[1]	I/O	Media Dependent Interface[1]. In MDI configuration, MDI[1]± is used for the receive pair. In MDIX configuration, MDI[1]± is used for the transmit pair.
16	18	SIGDET	I	In 100BASE-FX mode, SIGDET indicates whether a signal is detected by the fiber optic transceiver. In 100BASE-TX/10BASE-T modes, this pin should not be left floating. It should be tied either high or low.

Table 5: Serial Management Interface

88E3015	88E3018	Pin Name	Type	Description
38	48	MDC	I	MDC is the clock reference for the serial management interface. A continuous clock stream is not required (i.e., MDC can be stopped when the MDC/MDIO master is not sending a command). The maximum frequency supported is 8.33 MHz.
35	45	MDIO	I/O	MDIO is the management data. MDIO is used to transfer management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm.

Table 6: LED

88E3015	88E3018	Pin Name	Type	Description
8	9	LED[2]/Interrupt	O	Parallel LED outputs. See Section 2.11 "LED Interface" on page 41 for LED interface details. See Section 2.2.3 "Programming Interrupts" on page 28 for interrupt details.
7	8	LED[1]	O	Parallel LED outputs. See Section 2.11 "LED Interface" on page 41 for details.
5	6	LED[0]	O	Parallel LED outputs. See Section 2.11 "LED Interface" on page 41 for details.

Table 7: JTAG

88E3015	88E3018	Pin Name	Type	Description
--	43	TDI	I	Boundary scan test data input. TDI contains an internal 150 kohm pull-up resistor.
--	41	TMS	I	Boundary scan test mode select input. TMS contains an internal 150 kohm pull-up resistor.
--	42	TCK	I	Boundary scan test clock input. TCK contains an internal 150 kohm pull-up resistor.
--	11	TRSTn	I	Boundary scan test reset input. Active low. TRSTn contains an internal 150 kohm pull-up resistor as per the 1149.1 specification. After power up, the JTAG state machine should be reset by applying a low signal on this pin, or by keeping TMS high and applying 5 TCK pulses, or by pulling this pin low by a 4.7 kohm resistor.
--	44	TDO	O	Boundary scan test data output.

Table 8: Clock/Configuration/Reset

88E3015	88E3018	Pin Name	Type	Description
32	38	XTAL_IN	I	Reference Clock. 25 MHz ± 50 ppm tolerance crystal reference or oscillator input.
33	39	XTAL_OUT	O	Reference Clock. 25 MHz ± 50 ppm tolerance crystal reference. When the XTAL_OUT pin is not connected, it should be left floating. XTAL_OUT is used for crystal only. This pin should be left floating when an oscillator input is connected to XTAL_IN.
3 2 1 56	3 2 1 64	CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	I	Hardware Configuration. See Section 2.6 "Hardware Configuration" on page 36 for details.
9	10	RESETn	I	Hardware reset. Active low. XTAL_IN/XTAL_OUT must be active for a minimum of 10 clock cycles before the rising edge of RESETn. RESETn must be pulled high for normal operation.
49	57	VREF	I	MAC Interface input voltage reference. Must be set to VDDOR/2 when used as 2.5V SSTL_2. Set to VDDOR when used as 2.5V LV CMOS.
39	4	COMAn	I	COMA Control. Active low. If RESETn is low then COMAn has no effect. COMAn contains an internal 150 kohm pull-up resistor. 0 = In power saving mode 1 = Normal operation

Table 9: Regulator & Reference

88E3015	88E3018	Pin Name	Type	Description
28	33	RSET	I	Constant voltage reference. External 2 kohm 1% resistor connection to VSS is required for this pin.
10	12	DIS_REG12	I	1.2V Regulator Disable. Tie to VDDO to disable, Tie to VSS to enable.
15	17	CTRL25	O	2.5V Regulator Control. This signal ties to the base of the BJT. If the 2.5V regulator is not used it can be left floating.

Table 10: Test

88E3015	88E3018	Pin Name	Type	Description
31	36	HSDACP	O	Test Pin. These pins have 49.9 ohm internal termination. They should be brought out to a via or pad to facilitate debug. If debug is not important and there are board space constraints, this pin can be left floating.
30	35	HSDACN	O	Test Pin. These pins have 49.9 ohm internal termination. They should be brought out to a via or pad to facilitate debug. If debug is not important and there are board space constraints, this pin can be left floating.
27	32	TSTPT	O	Test point. Leave unconnected.

Table 11: Power & Ground

88E3015	88E3018	Pin Name	Type	Description
24	28	AVDD	Power	Analog supply. 2.5V. AVDD can be supplied externally with 2.5V, or via the 2.5V regulator.
29	34	AVDDC	Power	Analog supply - 2.5V or 3.3V. AVDDC must be supplied externally. Do not use the 2.5V regulator to power AVDDC.
12 13	14 15	AVDDR	Power	1.2V Regulator supply - 2.5V AVDDR can be supplied externally with 2.5V, or via the 2.5V regulator. If the 1.2V regulator is not used, AVDDR must still be tied to 2.5V.
14	16	AVDDX	Power	2.5V Regulator supply - 3.3V AVDDX must be supplied externally. Note that this supply must be the same voltage as AVDDC. If the 2.5V regulator is not used, then it means a 2.5V supply is in the system. AVDDX should be left floating.
4 11 34	5 13 40	DVDD		Digital core supply - 1.2V. DVDD can be supplied externally with 1.2V, or via the 1.2V regulator.
6 20 36	7 24 46	VDDO	Power	2.5V or 3.3V non-MAC Interface digital I/O supply. VDDO must be supplied externally. Do not use the 2.5V regulator to power VDDO.
44 48	52 56	VDDOR	Power	2.5V or 3.3V MAC Interface digital I/O supply. VDDOR must be supplied externally. Do not use the 2.5V regulator to power VDDOR.
EPAD	EPAD	VSS	Ground	Ground to digital core. The 64-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS. Refer to the package mechanical drawings for the exact location and dimensions of the EPAD.
21 37 40	21 22 27 29 37 47	NC	NC	No Connect. These pins are not bonded to the die and can be tied to anything.

Table 12: I/O State at Various Test or Reset Modes

Pin(s)	Isolate	Loopback	Software Reset	Hardware Reset	Power Down	Power Down and Isolate
MDIP/ N[1:0]	Active	Active	Tri-state	Tri-state	Tri-state	Tri-state
TX_CLK	Tri-state	Active	Active	Tri-state	Active	Tri-state
RXD[0] RXD[2] RXD[3] RXD[1] RX_DV RX_ER CRS COL	Tri-state	Active	Low	Low	Low	Tri-state
RX_CLK	Tri-state	Active	Reg. 28.1 state 1 = Active 0 = Low	Low	Reg. 28.1 state 1 = Active 0 = Low	Tri-state
MDIO	Active	Active	Active	Tri-state	Active	Active
LED	Active	Active	Active	High	High	High
TDO	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state

1.3.2 88E3015 56-Pin QFN Assignments - Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
24	AVDD	37	NC
29	AVDDC	40	NC
12	AVDDR	9	RESETn
13	AVDDR	28	RSET
14	AVDDX	45	RX_CLK
19	COL	41	RX_CTRL
39	COMAn	17	RX_ER
56	CONFIG[0]	42	RXD[0]
1	CONFIG[1]	43	RXD[1]
2	CONFIG[2]	46	RXD[2]
3	CONFIG[3]	47	RXD[3]
18	CRS	16	SIGDET
15	CTRL25	27	TSTPT
10	DIS_REG12	52	TX_CLK
4	DVDD	55	TX_CTRL
11	DVDD	50	TXD[0]
34	DVDD	51	TXD[1]
30	HSDACN	53	TXD[2]
31	HSDACP	54	TXD[3]
5	LED[0]	6	VDDO
7	LED[1]	20	VDDO
8	LED[2]	36	VDDO
38	MDC	44	VDDOR
25	MDIN[0]	48	VDDOR
22	MDIN[1]	49	VREF
35	MDIO	EPAD	VSS
26	MDIP[0]	32	XTAL_IN
23	MDIP[1]	33	XTAL_OUT
21	NC		

1.3.3 88E3018 64-Pin QFN Assignments - Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
28	AVDD	47	NC
34	AVDDC	10	RESETn
14	AVDDR	33	RSET
15	AVDDR	53	RX_CLK
16	AVDDX	49	RX_CTRL
23	COL	19	RX_ER
4	COMAn	50	RXD[0]
64	CONFIG[0]	51	RXD[1]
1	CONFIG[1]	54	RXD[2]
2	CONFIG[2]	55	RXD[3]
3	CONFIG[3]	18	SIGDET
20	CRS	42	TCK
17	CTRL25	43	TDI
12	DIS_REG12	44	TDO
5	DVDD	41	TMS
13	DVDD	11	TRSTn
40	DVDD	32	TSTPT
35	HSDACN	60	TX_CLK
36	HSDACP	63	TX_CTRL
6	LED[0]	58	TXD[0]
8	LED[1]	59	TXD[1]
9	LED[2]	61	TXD[2]
48	MDC	62	TXD[3]
30	MDIN[0]	7	VDDO
25	MDIN[1]	24	VDDO
45	MDIO	46	VDDO
31	MDIP[0]	52	VDDOR
26	MDIP[1]	56	VDDOR
21	NC	57	VREF
22	NC	EPAD	VSS
27	NC	38	XTAL_IN
29	NC	39	XTAL_OUT
37	NC		

Section 2. Functional Description

Figure 3 shows the functional block for each of the 88E3015/88E3018 devices. The transmitter and transmit PCS block are fully described on page 29. The receiver and receive PCS block are fully described on page 29.

Figure 3: 88E3015 Device Functional Block Diagram

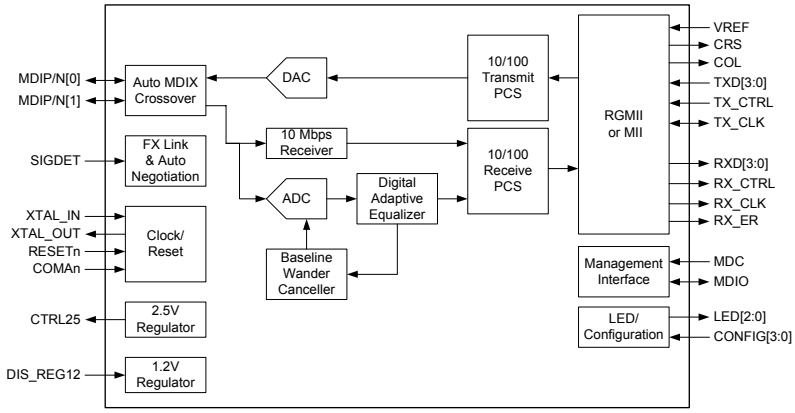
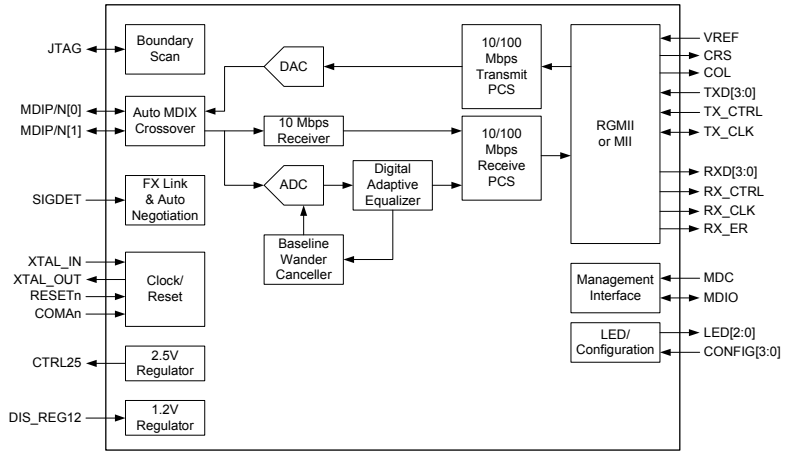


Figure 4: 88E3018 Device Functional Block Diagram



2.1 MAC Interface

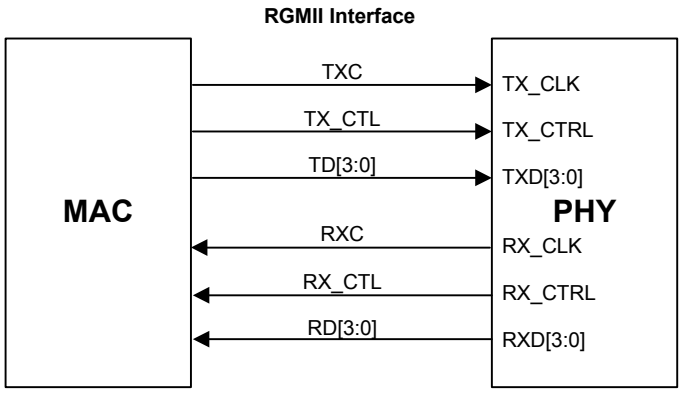
The MAC interfaces that are available for each device are listed in Table 1, “88E3015/88E3018 Devices Feature Differences,” on page 4.

All ports on the devices operate in the same interface mode that is selected.

2.1.1 Reduced Gigabit Media Independent Interface (RGMII)

The 88E3015/88E3018 device supports the RGMII specification (Version 1.2a, 9/22/2000, version 2.0, 04/2002 - instead of HSTL, it supports 2.5V SSTL_2.).

Figure 5: RGMII Signal Diagram



The interface runs at 2.5 MHz for 10 Mbps and 25 MHz for 100 Mbps. The TX_CLK signal is always generated by the MAC, and the RX_CLK signal is generated by the PHY.

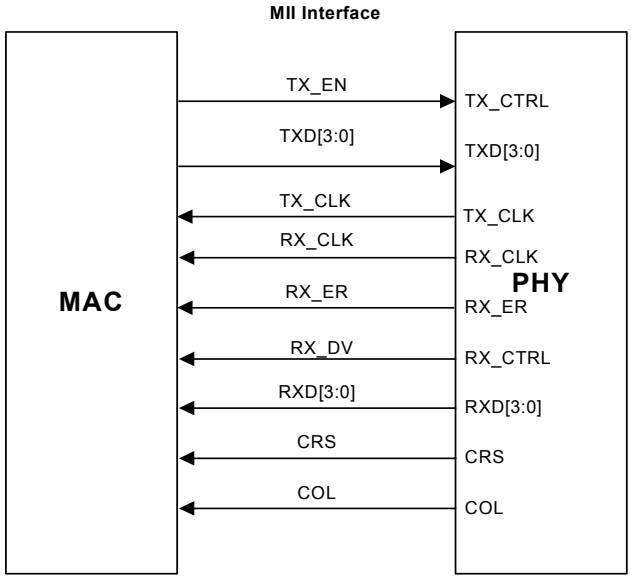
During packet reception, RX_CLK may be stretched on either the positive or negative pulse to accommodate the transition from the free running clock to a data synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulse is allowed. No glitching of the clocks is allowed during speed transitions.

The MAC must hold TX_CTRL low until the MAC has ensured that TX_CTRL is operating at the same speed as the PHY.

2.1.2 Media Independent Interface (MII)

The 88E3015/88E3018 device supports the Media Independent Interface.

Figure 6: MII Signal Diagram

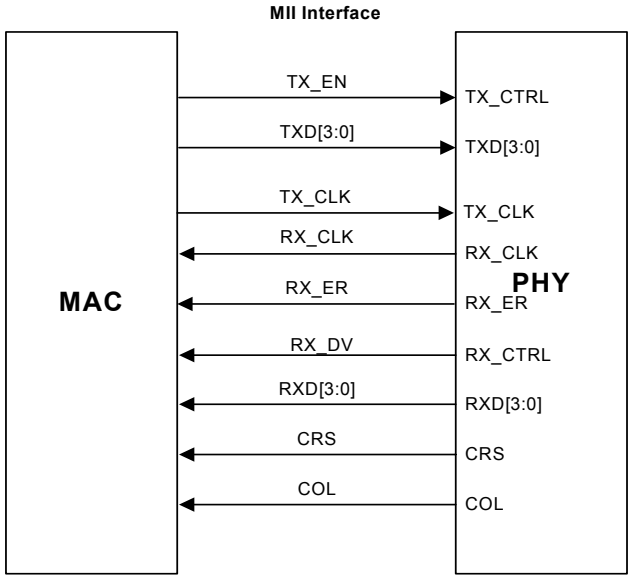


When the MII mode is selected, both TX_CLK and RX_CLK source 2.5 MHz and 25 MHz for 10 Mbps and 100 Mbps respectively.

2.1.3 Source Synchronous MII

The 88E3015/88E3018 device supports Source Synchronous MII.

Figure 7: Source Synchronous MII Signal Diagram



The Source Synchronous MII is identical to the MII, except the TX_CLK is an input. Refer to Section 4.7 for timing details.

2.2 Serial Management Interface

The serial management interface provides access to the internal registers via the MDC and MDIO pins and is compliant to IEEE 802.3u section 22. MDC is the management data clock input and can run from DC to a maximum rate of 8.33 MHz. MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC. The MDIO pin requires a 1.5 kohm pull-up resistor that pulls the MDIO high during idle and turnaround times.

2.2.1 MDC/MDIO Read and Write Operations

All the relevant serial management registers are implemented as well as several optional registers. A description of the registers can be found in Section 3. "Register Description" on page 56.

Figure 8: Typical MDC/MDIO Read Operation

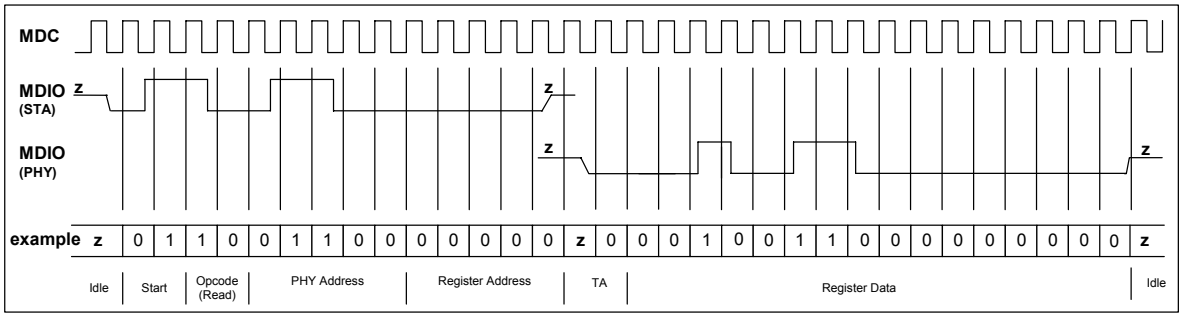


Figure 9: Typical MDC/MDIO Write Operation

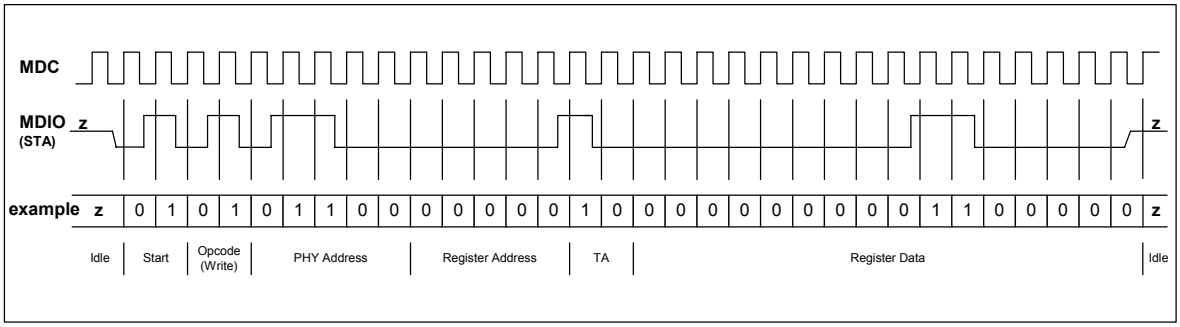


Table 13 is an example of a read operation.

Table 13: Serial Management Interface Protocol

32-Bit Preamble	Start of Frame	Opcode Read = 10 Write = 01	5-Bit Phy Device Address	5-Bit Phy Register Address	2-Bit Turn-around Read = z0 Write = 10	16-Bit Data Field	Idle
11111111	01	10	01100	00000	z0	0001001100000000	11111111

2.2.2 Preamble Suppression

The 88E3015/88E3018 devices are permanently programmed for preamble suppression. A minimum of one idle bit is required between operations.

2.2.3 Programming Interrupts

When Register 22:11:8 is set to 1110, the interrupt functionality is mapped to the LED[2] pin.The interrupt function drives the LED[2] pin active whenever an interrupt event is enabled by programming register 18. The polarity of the interrupt signal is determined by Register 25.14. This function minimizes the need for polling via the serial management interface. Table 14 shows the interrupts that may be programmed.

Table 14: Programmable Interrupts

Register Address	Programmable Interrupts
18.14	Speed Changed Interrupt Enable
18.13	Duplex Changed Interrupt Enable
18.12	Page Received Interrupt Enable
18.11	Auto-Negotiation Completed Interrupt Enable
18.10	Link Status Changed Interrupt Enable
18.9	Symbol Error Interrupt Enable
18.8	False Carrier Interrupt Enable
18.7	FIFO Over/Underflow Interrupt Enable
18.6	MDI/MDIX Crossover Changed Enable
18.4	Energy Detect Changed Enable
18.1	Polarity Changed Enable
18.0	Jabber Interrupt Enable

Register 18 determines whether the LED[2] pin is asserted when an interrupt event occurs. Register 19 reports interrupt status. When an interrupt event occurs, the corresponding bit in register 19 is set and remains set until register 19 is read via the serial management interface. When interrupt enable bits are not set in register 18, interrupt status bits in register 19 are still set when the corresponding interrupt events occur. However, the LED[2] pin is not asserted.

The LED[2] pin is active as long as at least one interrupt status bit is set in register 19 with its corresponding interrupt enable bit set in register 18, and Register 22:11:8 = 1110.

To de-assert the LED[2] pin:

- Clear of register 19 via a serial management read
- Disable the interrupt enable by writing register 18

2.3 Transmit and Receive Functions

The transmit and receive paths for the 88E3015/88E3018 device are described in the following sections.

2.3.1 Transmit Side Network Interface

2.3.1.1 Multi-mode TX Digital to Analog Converter

The 88E3015/88E3018 device incorporates a multi-mode transmit DAC to generate filtered MLT-3, NRZI, or Manchester coded symbols. The transmit DAC performs signal wave shaping to reduce EMI. The transmit DAC is designed for very low parasitic loading capacitances to improve the return loss requirement, which allows the use of low cost transformers.

2.3.1.2 Slew Rate Control and Waveshaping

In 100BASE-TX mode, slew rate control is used to minimize high frequency EMI. In 10BASE-T mode, the output waveform is pre-equalized via a digital filter.

2.3.2 Encoder

2.3.2.1 100BASE-TX

In 100BASE-TX mode, the transmit data stream is 4B/5B encoded, serialized, and scrambled. Upon initialization, the initial scrambling seed is determined by the PHY address. The datastream is then MLT-3 coded.

2.3.2.2 10BASE-T

In 10BASE-T mode, the transmit data is serialized and converted to Manchester encoding.

2.3.2.3 100BASE-FX

In 100BASE-FX mode, the transmit data stream is 4B/5B encoded, serialized, and converted to NRZI.

2.3.3 Receive Side Network Interface

2.3.3.1 Analog to Digital Converter

The 88E3015/88E3018 device incorporates an advanced high speed ADC on each receive channel with greater resolution for better SNR, and therefore, lower error rates. Patented architectures and design techniques result in high differential and integral linearity, high power supply noise rejection, and low metastability error rate.

2.3.3.2 Baseline Wander Canceller

The 88E3015/88E3018 device employs an advanced baseline wander cancellation circuit to automatically compensate for this DC shift. It minimizes the effect of DC baseline shift on the overall error rate.

2.3.3.3 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

2.3.3.4 Link Monitor

The link monitor is responsible for determining if link is established with a link partner. In 10BASE-T mode, link monitor function is performed by detecting the presence of valid link pulses (NLPs) on the MDI± pins.

In 100BASE-TX mode, link is established by scrambled idles.

See Section 2.8 for unidirectional enable.

2.3.3.5 Copper Signal Detection

In 100BASE-TX mode, the signal detection function is based on the receive signal energy detected on the MDI± pins that is continuously qualified by the squelch detect circuit, and the local receiver acquiring lock.

2.3.3.6 Fiber Signal Detection

The SIGDET pin is used to qualify whether there is receive energy on the line. Register 16.6 determines the polarity of the SIGDET pin. When Register 16.6 is set low, the SIGDET pin polarity is active high, otherwise the polarity is active low.

2.3.4 Decoder

2.3.4.1 100BASE-TX

In 100BASE-TX mode, the receive data stream is recovered and converted to NRZ. The NRZ stream is descrambled and aligned to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded. The receiver does not attempt to decode the data stream unless the scrambler is locked. The descrambler “locks” to the *scrambler* state after detecting a sufficient number of consecutive idle code-groups. Once locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization. The descrambler is always forced into the *unlocked* state when a link failure condition is detected, or when insufficient idle symbols are detected.

2.3.4.2 10BASE-T

In 10BASE-T mode, the recovered 10BASE-T signal is decoded from Manchester to NRZ, and then aligned. The alignment is necessary to insure that the start of frame delimiter (SFD) is aligned to the nibble boundary.

2.3.4.3 100BASE-FX

In 100BASE-FX mode the receive data stream is received and converted to NRZ. The decoding process is identical to 100BASE-TX except no descrambling is necessary.

2.3.5 Auto-Negotiation

The 88E3015/88E3018 device can auto-negotiate to operate in 10BASE-T or 100BASE-TX

If Auto-Negotiation is enabled, then the 88E3015/88E3018 devices negotiate with the link partner to determine the speed and duplex with which to operate. If the link partner is unable to Auto-Negotiate, the 88E3015/88E3018 devices go into the parallel detect mode to determine the speed of the link partner. Under parallel detect mode, the duplex mode is fixed at half-duplex.

2.3.5.1 Register Update

Auto-Negotiation is initiated upon any of the following conditions:

- Power up reset
- Hardware reset
- Software reset
- Restart Auto-Negotiation
- Transition from power down to power up
- Changing from the *link-up* state to the *linkfail* state

Changes to the AnegEn, SpeedLSB, and Duplex bits (Registers 0.12, 0.13, and 0.8, respectively) do not take effect unless one of the following takes place:

- Software reset (SWReset bit - Register 0.15)
- Restart Auto-Negotiation (RestartAneg bit - Register 0.9)
- Transition from power down to power up (PwrDwn bit - Register 0.11)
- The link goes down

The Auto-Negotiation Advertisement register (Register 4) is internally latched once every time Auto-Negotiation enters the *ability detect* state in the arbitration state machine. Hence, a write into the Auto-Negotiation Advertisment Register has no effect once the 88E3015/88E3018 devices begin to transmit Fast Link Pulses (FLPs). This guarantees that a sequence of FLPs transmitted is consistent with one another.

The Next Page Transmit register (Register 7) is internally latched once every time Auto-Negotiation enters the *next page exchange* state in the arbitration state machine.

2.3.5.2 Next Page Support

The 88E3015/88E3018 devices support the use of next page during Auto-Negotiation. By default, the received base page and next page are stored in the Link Partner Ability register - Base Page (Register 5). The 88E3015/88E3018 devices have an option to write the received next page into the Link Partner Next Page register - Register 8 - (similar to the description provided in the IEEE 802.3ab standard) by programming the Reg8NxtPg bit (PHY Specific Control Register - Register 16.12).

2.4 Power Management

The 88E3015/88E3018 devices support advanced power management modes that conserve power.

Three low power modes are supported in the 88E3015/88E3018 devices.

- IEEE 802.3 22.2.4.1.5 compliant power down
- Energy Detect+™
- COMA mode

IEEE 22.2.4.1.5 power down compliance allows for the PHY to be placed in a low-power consumption state by register control.

Energy Detect+™ allows the 88E3015/88E3018 devices to wake up when energy is detected on the wire with the additional capability to wake up a link partner. The 10BASE-T link pulses are sent once every second while listening for energy on the line.

COMA mode shuts down the PHY into a low power state.

Table 15 displays the low power operating mode selection.

Table 15: Operating Mode Selection

Power Mode	How to Activate Mode
IEEE Power Down	PwrDwn bit write (Register 0.11)
Energy Detect+™	Register EDet bit write (Register 16.14)
COMA	COMAn pin

2.4.1 IEEE Power Down Mode

The standard IEEE power down mode is entered by setting Register 0.11 equal to one. In this mode, the PHY does not respond to any MAC interface signals except the MDC/MDIO. It also does not respond to any activity on the CAT 5 cable.

In this power down mode, the PHY cannot wake up on its own by detecting activity on the CAT 5 cable. It can only wake up by clearing the PwrDwn bit to 0.

2.4.2 Energy Detect +™

When Register 16.14 is enabled, the Energy Detect +™ mode is enabled. In this mode, the PHY sends out a single 10 Mbps NLP (Normal Link Pulse) every one second. If the 88E3015/88E3018 devices are in Energy Detect+ mode, it can wake a connected device. The 88E3015/88E3018 devices also respond to MDC/MDIO.

2.4.3 Normal 10/100 Mbps Operation

Normal 10/100 Mbps operation can be entered by either using a register write during the energy detect mode.

2.4.4 COMA Mode

COMA mode shuts down the PHY into a low power state when it is not being used. When the PHY is in the COMA mode, the PHY is completely non-functional including register access. COMA mode is entered when the COMAn pin is set low.

If hardware reset pin (RESETn) and the COMA pin (COMAn) are asserted simultaneously the hardware reset function has priority over the COMA function.

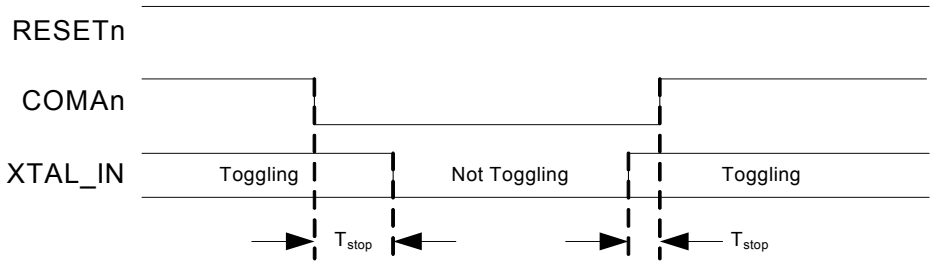
If the PHY is disabled by removing any one or more of the external power supplies then the COMAn pin has no functionality. If the PHY is re-enabled then the proper power up sequence must be followed and a hardware reset applied before the PHY enters into the normal operating state.

If the reference clock (XTAL_IN, XTAL_OUT) stops when the PHY is disabled then the reference clock must be restarted and hardware reset must be applied before the PHY enters into the normal operating state.

If all external power supplies remain powered up and the reference clock continues to run then the PHY can enter and exit the COMA state without the need for hardware reset by simply controlling the COMAn pin. If XTAL_IN is attached to an oscillator instead of a crystal and if the reference clock can be cleanly switched between toggling at 25 MHz and non-toggling state without glitches then the XTAL_IN can be stopped if the relationship shown in Figure 10 can be met. Tstop should be at least 1 ms. Tstart should be at least 0 ms.

Note that if the power supply and reference clock requirements can be met then all registers will retain their values during the COMA state.

Figure 10: XTAL_IN to COMAn Relationship



2.5 Regulators and Power Supplies

The 88E3015/88E3018 device can operate from a single 2.5V or 3.3V supply if the regulators are used. If regulators are not used then a 2.5V and 1.2V supply are needed. Table 16 lists the valid combinations of regulator usage.

The VDDO supply can run at 2.5V or 3.3V and that the VDDOR supply can run at 2.5V or 3.3V. The 2.5V generated by the 2.5V regulator must not be used to supply VDDO or VDDOR.

The AVDDC and AVDDX must always be at the same voltage level if AVDDX is not floating.

Table 16: Power Supply Options

Supply Configuration Option	Pin Name	AVDDC	AVDDX	AVDD	AVDDR	DVDD
	Comment	High Voltage Analog	2.5V Regulator	2.5V Analog	1.2V Regulator	1.2V Digital
Single 3.3V supply	Need External BJT DIS_REG12 = VSS	3.3V External	3.3V External	2.5V from BJT	2.5V from BJT	1.2V from Internal Regulator
3.3V supply and 1.2V supply	Need External BJT DIS_REG12 = VDDO	3.3V External	3.3V External	2.5V from BJT	2.5V from BJT	1.2V External
Single 2.5V supply	Do not connect external BJT DIS_REG12 = VSS	2.5V External	Floating	2.5V External	2.5V External	1.2V from Internal Regulator
2.5V supply and 1.2V supply	Do not connect external BJT DIS_REG12 = VDDO	2.5V External	Floating	2.5V External	2.5V External	1.2V External

The 2.5V regulator is not used if CTRL25 is left floating and not connected to a BJT.

The 1.2V regulator is disabled when DIS_REG12 is tied to VDDO. It is enabled when DIS_REG12 is tied to VSS.

2.5.1 AVDD

AVDD is used as the 2.5V analog supply. AVDD can be supplied externally with 2.5V, or via the 2.5V regulator.

2.5.2 AVDDC

AVDDC is used as the high voltage analog supply and can run on 2.5V or 3.3V.

AVDDC must be supplied externally. Do not use the 2.5V regulator to power AVDDC.

2.5.3 AVDDR

AVDDR is used as the 2.5V supply to the internal regulator that generates the 1.2V digital supply.

AVDDR can be supplied externally with 2.5V, or via the 2.5V regulator.

If the 1.2V regulator is not used, AVDDR must still be tied to 2.5V.

2.5.4 AVDDX

AVDDX is used as the 3.3V supply to the external regulator that generates the 2.5V supply.

AVDDX must be supplied externally. Note that this supply must be the same voltage as AVDDC.

If the 2.5V regulator is not used, then the CTRL25 pin should be left floating. In this particular case when the 2.5V regulator is not used, the AVDDX pin should be left floating.

2.5.5 DVDD

DVDD is used as the 1.2V digital supply.

DVDD can be supplied externally with 1.2V, or via the 1.2V regulator.

All DVDD pins should be shorted together. A decoupling capacitor should be attached to pin 11 of the 88E3015 device and pin 13 of the 88E3018 device.

2.5.6 VDDO

VDDO supplies the non-MAC Interface digital I/O pins. The voltage range is 2.5V or 3.3V.

VDDO must be supplied externally. Do not use the 2.5V regulator to power VDDO.

Note

The CRS, COL, and RX_ER pins are on the VDDO supply.

2.5.7 VDDOR

VDDOR supplies the MAC Interface digital I/O pins. The voltage should be 2.5V or 3.3V.

VDDOR must be supplied externally. Do not use the 2.5V regulator to power VDDOR.

Three options are supported:

- 2.5V LVCMOS
- 3.3V LVCMOS
- 2.5V SSTL_2

The VREF pin should be set to 0.5 x VDDOR for SSTL_2 behavior.

The VREF pin should be tied to VDDOR for LVCMOS behavior.

Note that 3.3V SSTL_2 is not supported.

Note

The CRS, COL, and RX_ER pins are not on the VDDOR supply.

2.6 Hardware Configuration

The 88E3015/88E3018 devices are configured by tying LED[2:0], CRS, COL, VDDO, or VSS to CONFIG[3:0]. After the deassertion of RESET the 88E3015/88E3018 will be hardware configured.

Note

LED[2], CRS, and COL should not be tied to CONFIG[2:0]. Use VDDO to set bits [1:0] of CONFIG[2:0] to ’11’.

The CONFIG pins should not be left floating.

The LED, CRS, and COL outputs a bit stream during initialization that is used by the CONFIG pin inputs. The bit values are latched at the deassertion of hardware reset. The bit stream mapping is shown in Table 17

Table 17: Three bit Mapping

Pin	Bits 2,1,0
VSS	000
LED[0]	001
LED[1]	010
LED[2]	011
CRS	100
COL	110
VDDO	111

The 3 bits for each CONFIG pin are mapped as shown in Table 18.

Table 18: Configuration Mapping

Pin	Bit 2	Bit 1	Bit 0
CONFIG[0]	Reserved	PHYAD[1]	PHYAD[0]
CONFIG[1]	Reserved	PHYAD[3]	PHYAD[2]
CONFIG[2]	Reserved	ENA_XC	PHYAD[4]
CONFIG[3]	MODE[2]	MODE[1]	MODE[0]

Each bit in the configuration is defined as shown in Table 19

Table 19: Configuration Definition

Bits	Definition	Bits Affected
PHYAD[4:0]	PHY Address	None
ENA_XC	0 = Default Disable Auto-Crossover	16.5:4 In 100BASE-FX mode, this should be disabled.
	1 = Default Enable Auto-Crossover	
MODE[2:0]	000 = Copper - RGMII, Receive clock transition when data transitions	28.11:10, 28.3
	001 = Copper - RGMII, Receive clock transition when data stable	
	010 = Fiber - RGMII, Receive clock transition when data transitions	
	011 = Copper - MII	
	100 = Fiber - MII	
	110 = Copper - Source Synchronous MII	
	111 = Fiber - RGMII, Receive clock transition when data stable	

Table 20 clarifies how the MODE[2:0] affects the register defaults.

Table 20: MODE[2:0] to Register Default Mapping

MODE[2:0]	MAC Interface Mode	Fiber/Copper
	28.11:10	28.3
000 (CONFIG3 = VSS)	00	0
001 (CONFIG3 = LED[0])	01	0
010 (CONFIG3 = LED[1])	00	1
011 (CONFIG3 = LED[2])	10	0
100 (CONFIG3 = CRS)	10	1
110 (CONFIG3 = COL)	11	0
111 (CONFIG3 = VDDO)	01	1

2.7 Far End Fault Indication (FEFI)

Far end fault indication provides a mechanism for transferring information from the local station to the link partner that a remote fault has occurred in 100BASE-FX mode.

A remote fault is an error in the link that one station can detect while the other one cannot. An example of this is a disconnected wire at a station's transmitter. This station is receiving valid data and detects that the link is good via the link monitor, but is not able to detect that its transmission is not propagating to the other station.

A 100BASE-FX station that detects this remote fault modifies its transmitted idle stream pattern from all ones to a group of 84 ones followed by one zero. This is referred to as the FEFI idle pattern.

The FEFI function is controlled by the FEFI bits in 100BASE-FX mode.

Register 16.8 enables and disables the FEFI function. This bit has no effect in 10BASE-T and 100BASE-TX modes.

2.8 802.3ah Unidirectional Enable

The 88E3015/88E3018 devices support the 802.3ah Unidirectional Enable function. When this function is enabled the PHY transmit path is enabled even if there is no link established. To enable unidirectional transmitting, all the following conditions must be met:

- Unidirectional is enabled (0.5 = 1)
- Auto-Negotiation is disabled (0.12 = 0)
- Full- duplex enabled (0.8 = 1).

Register 1.7 indicates that the PHY is able to transmit from the media independent interface regardless of whether the PHY has determined that a valid link has been established.

2.9 Virtual Cable Tester® Feature

The 88E3015/88E3018 devices Virtual Cable Tester (VCT™) feature uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors, and terminations. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and bad magnetics.

The 88E3015/88E3018 devices transmit a signal of known amplitude (+1V) down each of the two pairs of an attached cable. It will conduct the cable diagnostic test on each pair, testing the TX and RX pairs sequentially. The transmitted signal will continue down the cable until it reflects off of a cable imperfection. The magnitude of the reflection and the time it takes for the reflection to come back are shown in the VCT registers 26.12:8, 26.7:0, 27.12:8, and 27.7:0 respectively.

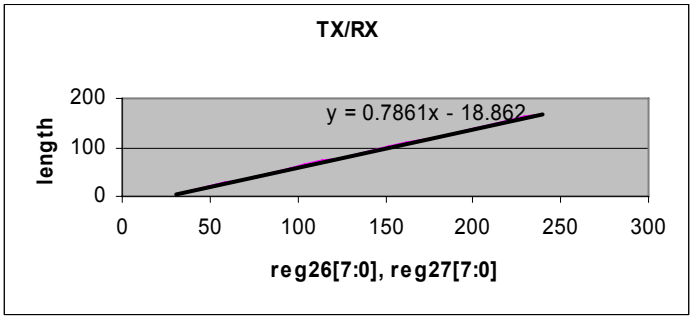
Using the information from the VCT Registers 26 and 27, the distance to the problem location and the type of problem can be determined. For example, the time it takes for the reflection to come back, can be converted to distance using the cable fault distance trend line tables in Figure 11. The polarity and magnitude of the reflection together with the distance will indicate the type of discontinuity. For example, a +1V reflection will indicate an open close to the PHY and a -1V reflection will indicate a short close to the PHY.

When the cable diagnostic feature is activated by setting Register 26.15 bit to one, a pre-determined amount of time elapses before a test pulse is transmitted. This is to ensure that the link partner loses link, so that it stops sending 100BASE-TX idles or 10 Mbit data packets. This is necessary to be able to perform the TDR test. The TDR test can be performed either when there is no link partner or when the link partner is Auto-Negotiating or sending 10 Mbit idle link pulses. If the 88E3015/88E3018 devices receive a continuous signal for 125 ms, it will declare test failure because it cannot start the TDR test. In the test fail case, the received data is not valid. The results of the test are also summarized in Register 26.14:13 and 27.14:13.

- 11 = Test fail (The TDR test could not be run for reasons explained above)
- 00 = Valid test, normal cable (no short or open in cable)
- 10 = Valid test, open in cable (Impedance > 333 ohms)
- 01 = Valid test, short in cable (Impedance < 33 ohms)

The definition for shorts and opens is arbitrary and the user can define it anyway they desire using the information in the VCT registers. The impedance mismatch at the location of the discontinuity could also be calculated knowing the magnitude of the reflection. Refer to the App Note "Virtual Cable Tester® -- How to use TDR results" for details.

Figure 11: Cable Fault Distance Trend Line



2.10 Auto MDI/MDIX Crossover

The 88E3015/88E3018 devices automatically determine whether or not it needs to cross over between pairs so that an external crossover cable is not required. If the 88E3015/88E3018 devices interoperate with a device that cannot automatically correct for crossover, the 88E3015/88E3018 devices make the necessary adjustment prior to commencing Auto-Negotiation. If the 88E3015/88E3018 devices interoperate with a device that implements MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 section 40.4.4 determines which device performs the crossover.

When the 88E3015/88E3018 devices interoperate with legacy 10BASE-T devices that do not implement Auto-Negotiation, the 88E3015/88E3018 devices follow the same algorithm as described above since link pulses are present. However, when interoperating with legacy 100BASE-TX devices that do not implement Auto-Negotiation (i.e. link pulses are not present), the 88E3015/88E3018 devices use signal detect to determine whether or not to crossover.

The Auto MDI/MDIX crossover function can be disabled via Register 16.5:4.

The 88E3015/88E3018 devices are set to MDI mode by default if auto MDI/MDIX crossover is disabled at hardware reset.

Auto MDI/MDIX should be disabled for 100BASE-FX mode. MDI should be forced for 100BASE-FX.

The pin mapping in MDI and MDIX modes is specified in Table 21. Refer to Figure 33 on page 117 for magnetics details.

Table 21: MDI/MDIX Pin Functions

Physical Pin	MDIX		MDI	
	100BASE-TX	10BASE-T	100BASE-TX	10BASE-T
MDIP/N[1]	Transmit	Transmit	Receive	Receive
MDIP/N[0]	Receive	Receive	Transmit	Transmit

2.11 LED Interface

The LEDs can either be controlled by the PHY or controlled externally, independent of the state of the PHY.

2.11.1 Manual Override

External control is achieved by writing to the PHY Manual LED Override register 25.5:0. Any of the LEDs can be turned on, off, or made to blink at variable rates independent of the state of the PHY. This independence eliminates the need for driving LEDs from the MAC or the CPU. If the LEDs are driven from the CPU located at the back of the board, the LED lines crossing the entire board will pick up noise. This noise will cause EMI issues. Also, PCB layout will be more difficult due to the additional lines routed across the board.

When the LEDs are controlled by the PHY, the activity of the LEDs is determined by the state of the PHY. Each LED can be programmed to indicate various PHY states, with variable blink rate.

Any one of the LEDs can be controlled independently of the other LEDs (i.e one LED can be externally controlled while another LED can be controlled by the state of the PHY).

Table 22: Manual Override

Bits	Field	Description
25.5:4	ForceLED2	00 = Normal
		01 = Blink[1]
		10 = LED Off
		11 = LED On
25.3:2	ForceLED1	00 = Normal
		01 = Blink
		10 = LED Off
		11 = LED On
25.1:0	ForceLED0	00 = Normal
		01 = Blink
		10 = LED Off
		11 = LED On

2.11.2 PHY Control

Manual override is disabled (25.5:4, 25.3:2, 25.1:0 is set to 00) then the LED behavior is defined by register 22.11:8, 22.7:4, and 22.3:0 (Table 23). If SPEED is selected then the LED behavior is further qualified by register 24.8:6, 24.5:3, and 24.2:0 (Table 24). See 2.2.3 "Programming Interrupts" when 22.11:8 is set to 1110.

Table 23: PHY LED Control

Bits	Field	Description
22.11:8	LED2	LED2 Control. This is a global setting.
		0000 = COLX
		0001 = ERROR
		0010 = DUPLEX
		0011 = DUPLEX/COLX
		0100 = SPEED
		0101 = LINK
		0110 = TX
		0111 = RX
		1000 = ACT
		1001 = LINK/RX
		1010 = LINK/ACT
		1011 = ACT (Blink mode)
		1100 = TX (Blink Mode)
		1101 = RX (Blink Mode)
		1110 = Interrupt
		1111 = Force off

Table 23: PHY LED Control (Continued)

Bits	Field	Description
22.7:4	LED1	LED1 Control. This is a global setting.
		0000 = COLX
		0001 = ERROR
		0010 = DUPLEX
		0011 = DUPLEX/COLX
		0100 = SPEED
		0101 = LINK
		0110 = TX
		0111 = RX
		1000 = ACT
		1001 = LINK/RX
		1010 = LINK/ACT
		1011 = ACT (Blink mode)
		1100 = TX (Blink Mode)
		1101 = RX (Blink Mode)
		1110 = COLX (Blink Mode)
		1111 = Force off

Table 23: PHY LED Control (Continued)

Bits	Field	Description
22.3:0	LED0	LED0 Control. This is a global setting.
		0000 = COLX
		0001 = ERROR
		0010 = DUPLEX
		0011 = DUPLEX/COLX
		0100 = SPEED
		0101 = LINK
		0110 = TX
		0111 = RX
		1010 = LINK/ACT
		1011 = ACT (Blink mode)
		1100 = TX (Blink Mode)
		1101 = RX (Blink Mode)
		1110 = COLX (Blink Mode)
		1111 = Force off

Table 24: Speed Dependent Behavior

Bits	Field	Description
24.8:6	LED2 Speed	LED 2 Speed Select 000 = Active for 10BASE-T Link 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Active for 100BASE-X 110 = Off 111 = Reserved
24.5:3	LED1 Speed	LED 1 Speed Select 000 = Active for 10BASE-T Link 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Active for 100BASE-X 110 = Off 111 = Reserved
24.2:0	LED0 Speed	LED 0 Speed Select 000 = Active for 10BASE-T Link 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Active for 100BASE-X 110 = Off 111 = Reserved

2.11.3 LED Polarity

The polarity of the LED in the active state can be set through register 25.14:12.

Table 25: LED Active Polarity

Bits	Field	Description
25.14	InvLED2	Invert LED2. This bit controls the active level of the LED2 pin. 0 = Active Low LED2 1 = Active High LED2
25.13	InvLED1	Invert LED1. This bit controls the active level of the LED1 pin. 0 = Active Low LED1 1 = Active High LED1
25.12	InvLED0	Invert LED0. This bit controls the active level of the LED0 pin. 0 = Active Low LED0 1 = Active High LED0

2.11.4 Stretching and Blinking

Some of the statuses can be pulse stretched. Pulse stretching is necessary because the duration of these status events might be too short to be observable on the LEDs. The pulse stretch duration can be programmed via Register 24.14:12. The default pulse stretch duration is set to 170 to 340 ms. The pulse stretch duration applies to all applicable LEDs.

Some of the statuses indicate multiple events by blinking LEDs. The blink period can be programmed via Register 24.11:9. The default blink period is set to 84 ms. The blink rate applies to all applicable LEDs.

2.12 Automatic and Manual Impedance Calibration

2.12.1 MAC Interface Calibration Circuit

The auto calibration is available for the MAC interface I/Os. The PHY runs the automatic calibration circuit with a 49 ohm impedance target by default after hardware reset. Other impedance targets are available by changing the impedance target and restarting the auto calibration through register writes. Individual NMOS and PMOS output transistors could be controlled for 38 to 80 ohm targets in various increments.

Manual NMOS and PMOS settings are available if the automatic calibration is not desired. If the PCB traces are different from 50 ohms, the output impedance of the MAC interface I/O buffers can be programmed to match the trace impedance. Users can adjust the NMOS and PMOS driver output strengths to perfectly match the transmission line impedance and eliminate reflections completely.

Note

The CRS, COL, and RX_ER pins are not calibrated.

2.12.2 MAC Interface Calibration Register Definitions

If Register 29 = 0x000A, then Register 30 is defined as follows:

Table 26: Register 30 Page 10 - MAC Interface Calibration Definitions

Reg bit	Function	Setting description	Mode	HW Reset	SW Reset
15	Restart Calibration	0 = Normal 1 = Restart Bit 15 is a self-clearing register. Calibration will start once the register is cleared.	R/W	0	Retain
14	Calibration Complete	1 = Calibration complete 0 = Calibration in progress	RO	0	Retain
13	Reserved	0	R/W	0	Retain
12:8	PMOS Value	00000 = All fingers off ... 11111 = All fingers on The automatic calibrated values are stored here after calibration completes. Once the LATCH bit is set to 1, the new calibration value is written. The automatic calibrated value is lost.	R/W	Auto calibrated value	Retain
7	Reserved	0	R/W	0	Retain
6	Latch	1 = Latch in new value. This bit self clears. (Used for manual settings)	R/W, SC	0	Retain

Table 26: Register 30 Page 10 - MAC Interface Calibration Definitions (Continued)

Reg bit	Function	Setting description	Mode	HW Reset	SW Reset
5	PMOS/NMOS select	1 = PMOS value is written when LATCH is set to 1 0 = NMOS value is written when LATCH is set to 1	R/W	0	Retain
4:0	NMOS Value	00000 = All fingers off ... 11111 = All fingers on The automatic calibrated values are stored here after calibration completes. Once the LATCH bit is set to 1, the new calibration value is written. The automatic calibrated value is lost.	R/W	Auto calibrated value	Retain

2.12.3 Changing Auto Calibration Targets

The PHY runs the automatic calibration circuit with a 49 ohm impedance target by default after hardware reset. Other impedance targets are available by changing the impedance target and restarting the auto calibration through register writes.

To change the auto calibration targets, write to the following registers:

Write to register 29 = 0x000B

Write to register 30, bit 6:4 = ppp (write new PMOS Target value)

Write to register 30, bit 2:0 = nnn (write new NMOS Target value)

Write to register 29 = 0x000A

Write to register 30 = 0x8000 (Restarts the auto calibration with the new target)

Example: To set the approximate 54 ohm auto calibration target, write the following:

Reg29 = 0x000B

Reg30, bit 6:4 = '011' and bit 2:0 = '011'

Reg29 = 0x000A

Reg30 = 0x8000

2.12.4 Manual Settings to The Calibration Registers

To use manual calibration, write to the following registers:

Write to register 29 = 0x000A

Write to register 30 = b'000P PPPP 011N NNNN -- adjusts PMOS strength

Write to register 30 = b'000P PPPP 010N NNNN -- adjusts NMOS strength

Where PPPPP is the 5 bit value for the PMOS strength.

Where NNNNN is the 5 bit value for the NMOS strength.

The value of PPPPP or NNNNN will depend on your board. The '11111' value enables all fingers for maximum drive strength, for minimum impedance. The '00000' value turns all fingers off for minimum drive strength, for maximum impedance. Use a scope to monitor the RX_CLK pin close to the destination. Start with the default auto-calibrated value and move in each direction to see how it affects signal integrity on your board.

Example: The automatic calibration has a 49 ohm target, but if the MII trace impedance on board was 60 ohms, you see reflections from a scope capture taken at the destination. See Figure 14. After manual calibration, you see that the reflections are eliminated in Figure 15.

Figure 12 and Figure 13 display the trend lines for 1.8V and 2.5V PMOS and NMOS impedance settings.

NOTE: The trend lines displayed in Figure 12 and Figure 13 use nominal values and may vary in production.

Figure 12: PMOS Output Impedance (1.8V, 2.5V) Trend Lines (TBD)

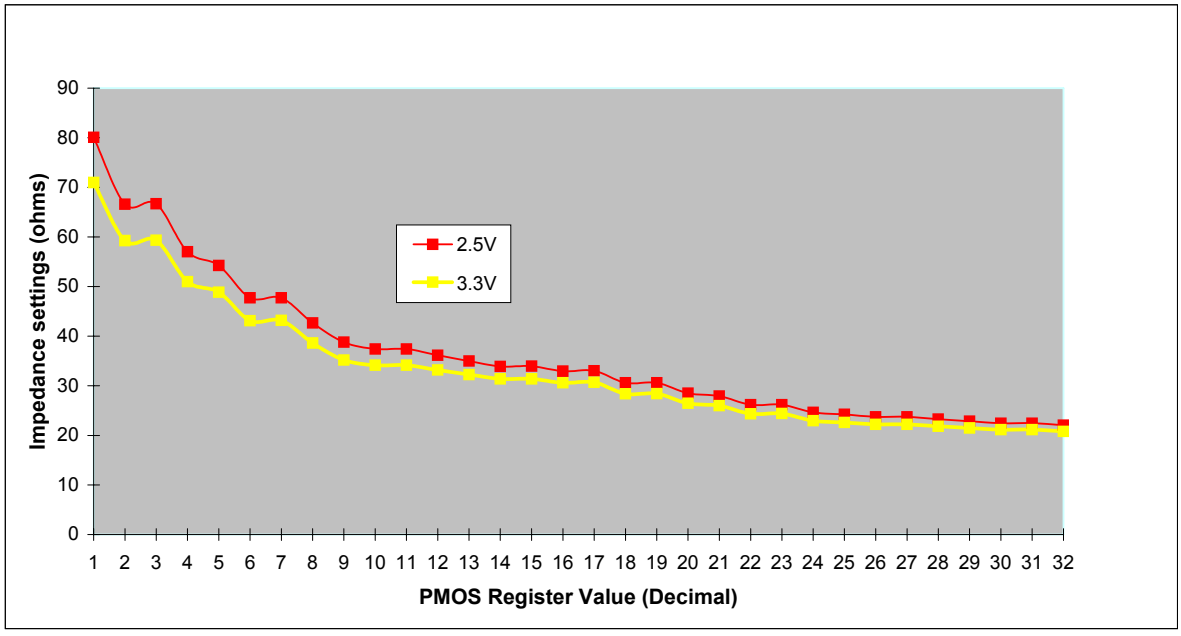
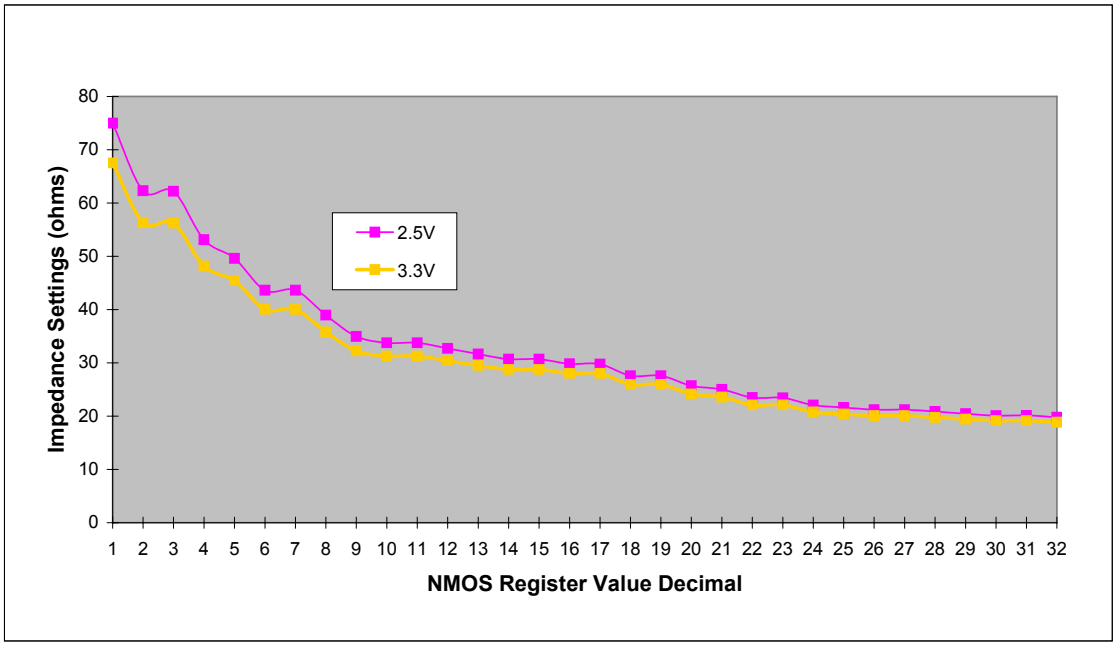


Figure 13: NMOS Output Impedance (1.8V, 2.5V) Trend Lines (TBD)



Example: The automatic calibration has a 50 ohm target, but if the MII trace impedance on board was 60 ohms, you see reflections from a scope capture taken at the destination. Refer to Figure 14. After manual calibration, you see that the reflections are eliminated as in Figure 15.

Figure 14: Signal Reflections, using the 50 ohm Setting, 60 ohm line

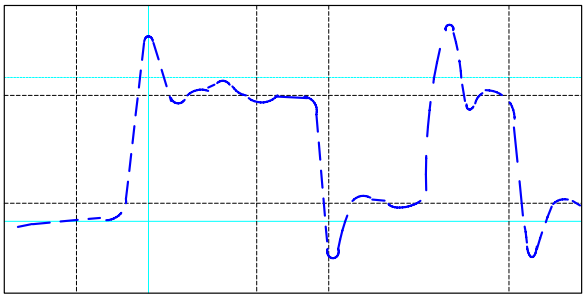
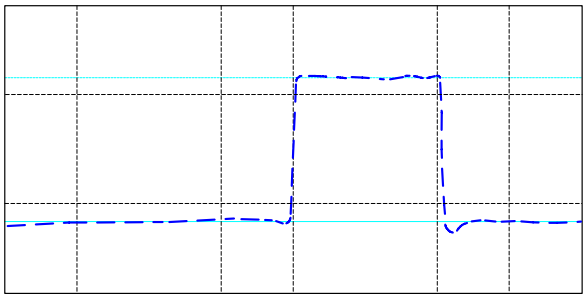


Figure 15: Clean signal after manual calibration for the 60 ohm



2.13 CRC Error Counter

The CRC counter, normally found in MACs, is available in the 88E3015/88E3018 device. The error counter feature is enabled through register writes and the counter is stored in an eight bit register.

2.13.1 Enabling The CRC Error Counter

2.13.1.1 Enabling Counter

Write to the following registers will enable both counters.

Register 29: 0x0009 (points to page 9 of Register 30)

Register 30: 0x0001 (enables CRC error counter)

2.13.1.2 Disabling and Clearing Counter

Write to the following register will disable and clear both counters.

Register 29: 0x0009 (points to page 9 of Register 30)

Register 30: 0x0000 (disable and clear CRC error)

2.13.1.3 Reading Counter Content

To read the CRC counter, write to the following registers.

Register 29: 0x0009 (points to page 9 of Register 30)

Register 30: bits 15:8 (CRC error count is stored in these bits)

The counter does not clear on a read command. To clear the CRC error counter, disable and enable the counters. See Page 9 of Register 30 for details.

2.14 IEEE 1149.1 Controller

The 88E3018 supports the IEEE1149.1 Test Access port and Boundary Scan. The 88E3015 does not support this feature.

The IEEE 1149.1 standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits.

The standard provides a solution for testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques.

The 88E3018 device implements six basic instructions: bypass, sample/preload, extest, clamp, HIGH-Z, and ID CODE. Upon reset, ID_CODE instruction is selected. The instruction opcodes are shown in Table 27.

Table 27: TAP Controller Op Codes

Instruction	OpCode
EXTEST	00000000
SAMPLE/PRELOAD	00000001
CLAMP	00000010
HIGH-Z	00000011
BYPASS	11111111
ID CODE	00000100

The 88E3018 device reserves 5 pins called the Test Access Port (TAP) to provide test access Test Mode Select Input (TMS), Test Clock Input (TCK), Test Data Input (TDI), and Test Data Output (TDO), and Test Reset Input (TRSTn). To ensure race-free operation all input and output data is synchronous to the test clock (TCK). TAP input signals (TMS and TDI) are clocked into the test logic on the rising edge of TCK, while output signal (TDO) is clocked on the falling edge. For additional details refer to the IEEE 1149.1 Boundary Scan Architecture document.

2.14.1 Bypass Instruction

The bypass instruction uses the bypass register. The bypass register contains a single shift-register stage and is used to provide a minimum length serial path between the TDI and TDO pins of the 88E3018 device. This allows rapid movement of test data to and from other testable devices in the system.

The extest instruction allows circuitry external to the 88E3018 device (typically the board interconnections) to be tested. Prior to executing the extest instruction, the first test stimulus to be applied is shifted into the boundary-scan registers using the sample/preload instruction. Thus, when the change to the extest instruction takes place, known data is driven immediately from the 88E3018 device to its external connections.

2.14.2 Sample/Preload Instruction

The sample/preload instruction allows scanning of the boundary-scan register without causing interference to the normal operation of the 88E3018 device. Two functions are performed when this instruction is selected: sample and preload.

Sample allows a snapshot to be taken of the data flowing from the system pins to the on-chip test logic or vice versa, without interfering with normal operation. The snapshot is taken on the rising edge of TCK in the Capture-DR controller state, and the data can be viewed by shifting through the component's TDO output.

While sampling and shifting data out through TDO for observation, preload allows an initial data pattern to be shifted in through TDI and to be placed at the latched parallel output of the boundary-scan register cells that are connected to system output pins. This ensures that known data is driven through the system output pins upon entering the extest instruction. Without preload, indeterminate data would be driven until the first scan sequence is complete. The shifting of data for the sample and preload phases can occur simultaneously. While data capture is being shifted out, the preload data can be shifted in.

One scan chain is available for the 88E3018 devices.

Table 28: 88E3018 Boundary Scan Chain Order

PIN	I/O
MDIO	Output Enable
MDIO	Output
MDIO	Input
MDC	Input
(RGMII)	Output Enable
RX_CTRL	Output
RXD[0]	Output
RXD[1]	Output
RX_CLK	Output
RXD[2]	Output
RXD[3]	Output
TXD[0]	Input
TXD[1]	Input
TX_CLK	Input
TXD[2]	Input
TXD[3]	Input
TX_CTRL	Input
CONFIG[0]	Input
CONFIG[1]	Input
CONFIG[2]	Input
CONFIG[3]	Input
LED[0]	Output Enable
LED[0]	Output
LED[1]	Output Enable
LED[1]	Output
LED[2]	Output Enable
LED[2]	Output
COMAn	Input
RESET	Input
SIGDET	Input

Table 28: 88E3018 Boundary Scan Chain Order (Continued)

PIN	I/O
(MII)	Output Enable
RX_ER	Output
CRS	Output
COL	Output

2.14.3 Extest Instruction

The extest instruction allows circuitry external to the PHY (typically the board interconnections) to be tested. Prior to executing the extest instruction, the first test stimulus to be applied is shifted into the boundary-scan registers using the sample/preload instruction. Thus, when the change to the extest instruction takes place, known data is driven immediately from the PHY to its external connections.

2.14.4 The Clamp Instruction

The clamp instruction allows the state of the signals driven from component pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the component pins will not change while the clamp instruction is selected.

2.14.5 The HIGH-Z Instruction

The HIGH-Z instruction places the component in a state in which all of its system logic outputs are placed in an inactive drive state (e.g., high impedance). In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component.

2.14.6 ID CODE Instruction

The ID CODE contains the manufacturer identity, part and version.

Table 29: ID CODE

Version	Part Number	Manufacturer Identity	
Bit 31 to 28	Bit 27 to 12	Bit 11 to 1	0
0000	0000 0000 0010 0001	001 1110 1001	1

Section 3. Register Description

The IEEE defines only 32 registers address space for the PHY. In order to extend the number of registers address space available a paging mechanism is used. For register address 30, register 29 bits 4 to 0 are used to specify the page. There is no paging for registers 1 and 28.

In this document, the short hand used to specify the registers take the form register_page.bit:bit, register_page.bit, register.bit:bit, or register.bit.

For example:

Register 30 page 9 bits 15 to 8 are specified as 30_9.15:8.

Register 30 page 9 bit 0 is specified as 30_9.0.

Register 2 bit 3 to 0 is specified as 2.3:0.

Note that in this context the setting of the page register (register 29) has no effect.

Register 2 bit 3 is specified as 2.3.

Table 30 defines the register types used in the register map.

Table 30: Register Types

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to a one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to zero and remains zero until a read operation is performed through the management interface or a reset occurs.
Retain	Value written to the register field does take effect without a software reset, and the register maintains its value after a software reset.
RES	Reserved for future use. All reserved bits are read as zero unless otherwise noted.
RO	Read only.
ROC	Read only clear. After read, register field is cleared to zero.
R/W	Read and write with initial value indicated.
RWC	Read/Write clear on read. All bits are readable and writable. After reset or after the register field is read, register field is cleared to zero.
SC	Self-Clear. Writing a one to this register causes the desired function to be immediately executed, then the register field is automatically cleared to zero when the function is complete.
Update	Value written to the register field does not take effect until soft reset is executed; however, the written value can be read even before the software reset.
WO	Write only. Reads to this type of register field return undefined data.

Table 31: Register Map

Register Name	Register Address	Table and Page
PHY Control Register	Register 0	Table 32, p. 59
PHY Status Register	Register 1	Table 33, p. 61
PHY Identifier	Register 2	Table 34, p. 63
PHY Identifier	Register 3	Table 35, p. 63
Auto-Negotiation Advertisement Register	Register 4	Table 36, p. 64
Link Partner Ability Register (Base Page)	Register 5	Table 37, p. 66
Link Partner Ability Register (Next Page)	Register 5	Table 38, p. 67
Auto-Negotiation Expansion Register	Register 6	Table 39, p. 68
Next Page Transmit Register	Register 7	Table 40, p. 69
Link Partner Next Page Register	Register 8	Table 41, p. 69
PHY Specific Control Register	Register 16	Table 42, p. 70
PHY Specific Status Register	Register 17	Table 43, p. 72
PHY Interrupt Enable	Register 18	Table 44, p. 73
PHY Interrupt Status	Register 19	Table 45, p. 75
PHY Interrupt Port Summary	Register 20	Table 46, p. 76
Receive Error Counter	Register 21	Table 47, p. 76
LED Parallel Select Register	Register 22	Table 48, p. 77
PHY LED Control Register	Register 24	Table 49, p. 79
PHY Manual LED Override	Register 25	Table 50, p. 80
VCT™ Register for MDIP/N[0] Pins	Register 26	Table 51, p. 81
VCT™ Register for MDIP/N[1] Pins	Register 27	Table 52, p. 82
PHY Specific Control Register II	Register 28	Table 53, p. 83
Test Mode Select	Register 29	Table 54, p. 84
CRC Status Register	Register 30_9	Table 55, p. 84
MAC Interface Output Impedance Calibration Override	Register 30_10	Table 56, p. 85
MAC Interface Output Impedance Target	Register 30_11	Table 57, p. 86

Table 32: PHY Control Register
Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	SWReset	R/W, SC	0x0	0x0	PHY Software Reset Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 0 = Normal operation 1 = PHY reset
14	Loopback	R/W	0x0	Retain	Enable Loopback Mode When loopback mode is activated, the transmitter data presented on TXD is looped back to RXD internally. The PHY has to be in forced 10 or 100 Mbps mode. Auto-Negotiation must be disabled. 0 = Disable loopback 1 = Enable loopback
13	SpeedLSB	R/W	0x1	Update	Speed Selection (LSB) When a speed change occurs, the PHY drops link and tries to determine speed when Auto-Negotiation is on. A write to this register bit has no effect unless any one of the following also occurs: Software reset is asserted (bit 15) or Power down (bit 11) transitions from power down to normal operation. 0 = 10 Mbps 1 = 100 Mbps
12	AnegEn	R/W	0x1	Update	Auto-Negotiation Enable A write to this register bit has no effect unless any one of the following also occurs: Software reset is asserted (bit 15, above), Power down (bit 11, below), or the PHY transitions from power down to normal operation. If the AnegEn bit is set to 0, the speed and duplex bits of the PHY Control Register (register 0) take effect. If the AnegEn bit is set to 1, speed and duplex advertisement is found in the Auto-Negotiation Advertisement Register (Register 4). 0 = Disable Auto-Negotiation Process 1 = Enable Auto-Negotiation Process

Table 32: PHY Control Register (Continued)
Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
11	PwrDwn	R/W	0x0	Retain	Power Down Mode When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (bit 15, above) and Restart Auto-Negotiation (bit 9, below) are not set by the user. 0 = Normal operation 1 = Power down
10	Isolate	R/W	0x0	Retain	Isolate Mode 0 = Normal operation 1 = Isolate
9	RestartAneg	R/W, SC	0x0	Self Clear	Restart Auto-Negotiation Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit is set. 0 = Normal operation 1 = Restart Auto-Negotiation Process
8	Duplex	R/W	0x1	Update	Duplex Mode Selection A write to this registers has no effect unless any one of the following also occurs: Software reset is asserted (bit 15), Power down (bit 11), or transitions from power down to normal operation. 0 = Half-duplex 1 = Full-duplex
7	ColTest	R/W	0x0	Retain	Collision Test Mode - This applies to E3010 only. 0 = Disable COL signal test 1 = Enable COL signal test
6	SpeedMSB	RO	Always 0	Always 0	Speed Selection Mode (MSB) Will always be 0. 0 = 100 Mbps or 10 Mbps
5	Unidirectional Enable	R/W	0x0	Retain	0 = Enable transmit direction only when valid link is established. 1 = Enable transmit direction regardless of valid link if register 0.12 = 0 and 0.8 = 1. Otherwise enable transmit direction only when valid link is established.
4:0	Reserved	RO	Always 0	Always 0	Will always be 0.

Table 33: PHY Status Register
Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100T4	RO	Always 0	Always 0	100BASE-T4 This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100FDX	RO	Always 1	Always 1	100BASE-T and 100BASE-X full-duplex 1 = PHY able to perform full-duplex
13	100HDX	RO	Always 1	Always 1	100BASE-T and 100BASE-X half-duplex 1 = PHY able to perform half-duplex
12	10FDX	RO	Always 1	Always 1	10BASE-T full-duplex 1 = PHY able to perform full-duplex
11	10HPX	RO	Always 1	Always 1	10BASE-T half-duplex 1 = PHY able to perform half-duplex
10	100T2FDX	RO	Always 0	Always 0	100BASE-T2 full-duplex. This protocol is not available. 0 = PHY not able to perform full-duplex
9	100T2HDX	RO	Always 0	Always 0	100BASE-T2 half-duplex This protocol is not available. 0 = PHY not able to perform half-duplex
8	ExtdStatus	RO	Always 0	Always 0	Extended Status 0 = No extended status information in Register 15
7	Unidirectional Ability	RO	Always 1	Always 1	1 = PHY able to transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established
6	MFPreSup	RO	Always 1	Always 1	MF Preamble Suppression Mode Must be always 1. 1 = PHY accepts management frames with preamble suppressed
5	AnegDone	RO	0x0	0x0	Auto-Negotiation Complete 0 = Auto-Negotiation process not completed 1 = Auto-Negotiation process completed
4	RemoteFault	RO, LH	0x0	0x0	Remote Fault Mode 0 = Remote fault condition not detected 1 = Remote fault condition detected
3	AnegAble	RO	Always 1	Always 1	Auto-Negotiation Ability Mode 1 = PHY able to perform Auto-Negotiation

Table 33: PHY Status Register (Continued)
Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
2	Link	RO, LL	0x0	0x0	Link Status Mode This register indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read RTLink (17.10). 0 = Link is down 1 = Link is up
1	JabberDet	RO, LH	0x0	0x0	Jabber Detect 0 = Jabber condition not detected 1 = Jabber condition detected
0	ExtdReg	RO	Always 1	Always 1	Extended capability mode. 1 = Extended register capabilities

Table 34: PHY Identifier Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organization-ally Unique Identifier Bit 3:18	RO	0x0141	0x0141	Marvell® OUI is 0x005043 0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 101000001 ^ ^ bit 3.....bit 18

Table 35: PHY Identifier Register 3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	Always 000011	Always 000011	Organizationally Unique Identifier bits 19:24 00 0011 ^.....^ bit 19...bit 24
9:4	ModelNum	RO	Always 100010	Always 100010	Model Number = 100010
3:0	RevNum	RO	Varies	Varies	Revision Number Contact Marvell® FAEs for information on the device revision number.

Table 36: Auto-Negotiation Advertisement Register
Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	AnegAd NxtPage	R/W	0x0	Retain	Next Page 0 = Not advertised 1 = Advertise Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg 0.9) or link goes down.
14	Ack	RO	Always 0	Always 0	Must be 0.
13	AnegAd ReFault	R/W	0x0	Retain	Remote Fault Mode 0 = Do not set Remote Fault bit 1 = Set Remote Fault bit Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg 0.9) or link goes down.
12	Reserved	R/W	0x0	Retain	Must be 0. Reserved bits are R/W to allow for forward compatibility with future IEEE standards. Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg 0.9) or link goes down.
11	AnegAd Asymmetric Pause	R/W	0x0	Retain	Asymmetric Pause Mode 0 = Asymmetric PAUSE not implemented 1 = Asymmetric PAUSE implemented Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg 0.9) or link goes down.
10	AnegAd Pause	R/W	0x0	Retain	Pause Mode 0 = MAC PAUSE not implemented 1 = MAC PAUSE implemented Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg 0.9) or link goes down.
9	AnegAd 100T4	R/W	0x0	Retain	100BASE-T4 mode 0 = Not capable of 100BASE-T4 Must be 0.
8	AnegAd 100FDX	R/W	0x1	Retain	100BASE-TX full-duplex Mode 0 = Not advertised 1 = Advertise Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg 0.9) or link goes down.

Table 36: Auto-Negotiation Advertisement Register (Continued)
Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
7	AnegAd 100HDX	R/W	0x1	Retain	100BASE-TX half-duplex Mode 0 = Not advertised 1 = Advertise Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg 0.9) or link goes down.
6	AnegAd 10FDX	R/W	0x1	Retain	10BASE-TX full-duplex Mode 0 = Not advertised 1 = Advertise Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg 0.9) or link goes down.
5	AnegAd 10HDX	R/W	0x1	Retain	10BASE-TX half-duplex Mode 0 = Not advertised 1 = Advertise Values programmed into the Auto-Negotiation Advertisement Register have no effect unless Auto-Negotiation is restarted (RestartAneg 0.9) or link goes down.
4:0	AnegAd Selector	R/W	Always 0x01	Always 0x01	Selector Field Mode 00001 = 802.3

Table 37: Link Partner Ability Register (Base Page) Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	LPNxt Page	RO	0x0	0x0	Next Page Mode Base page will be overwritten if next page is received and if Reg8NxtPg (16.12) is disabled. When Reg8NxtPg (16.12) is enabled, then next page is stored in the Link Partner Next Page register, and the Link Partner Ability Register holds the base page. Received Code Word Bit 15 0 = Link partner not capable of next page 1 = Link partner capable of next page
14	LPAck	RO	0x0	0x0	Acknowledge Received Code Word Bit 14 0 = Link partner did not receive code word 1 = Link partner received link code word
13	LPRemote Fault	RO	0x0	0x0	Remote Fault Received Code Word Bit 13 0 = Link partner has not detected remote fault 1 = Link partner detected remote fault
12:5	LPTechAble	RO	0x00	0x00	Technology Ability Field Received Code Word Bit 12:5
4:0	LPSelector	RO	0x00	0x00	Selector Field Received Code Word Bit 4:0

Table 38: Link Partner Ability Register (Next Page) Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	LPNxtPage	RO	--	--	Next Page Mode Base page will be overwritten if next page is received and if Reg8NxtPg (16.12) is disabled. When Reg8NxtPg (16.12) is enabled, then next page is stored in the Link Partner Next Page register, and Link Partner Ability Register holds the base page. Received Code Word Bit 15
14	LPAck	RO	--	--	Acknowledge Received Code Word Bit 14
13	LPMessage	RO	--	--	Message Page Received Code Word Bit 13
12	LPack2	RO	--	--	Acknowledge 2 Received Code Word Bit 12
11	LPToggle	RO	--	--	Toggle Received Code Word Bit 11
10:0	LPData	RO	--	--	Message/Unformatted Field Received Code Word Bit 10:0

Table 39: Auto-Negotiation Expansion Register
Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	Always 0x000	Always 0x000	Reserved. The Auto-Negotiation Expansion Register is not valid until the AnegDone (1.5) indicates completed.
4	ParFaultDet	RO/LH	0x0	0x0	Parallel Detection Level 0 = A fault has not been detected via the Parallel Detection function 1 = A fault has been detected via the Parallel Detection function
3	LPNxtPg Able	RO	0x0	0x0	Link Partner Next Page Able 0 = Link Partner is not Next Page able 1 = Link Partner is Next Page able
2	LocalNxtPg Able	RO	Always 0x1	Always 0x1	Local Next Page Able This bit is equivalent to AnegAble. 1 = Local Device is Next Page able
1	RxNewPage	RO/LH	0x0	0x0	Page Received 0 = A New Page has not been received 1 = A New Page has been received
0	LPAnegAble	RO	0x0	0x0	Link Partner Auto-Negotiation Able 0 = Link Partner is not Auto-Negotiation able 1 = Link Partner is Auto-Negotiation able

Table 40: Next Page Transmit Register
Register 7

Bits	Field	Mode	HW Rst	SW Rst	Description
15	TxNxtPage	R/W	0x0	0x0	A write to the Next Page Transmit Register implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Reserved Transmit Code Word Bit 14
13	TxMessage	R/W	0x1	0x1	Message Page Mode Transmit Code Word Bit 13
12	TxAck2	R/W	0x0	0x0	Acknowledge2 Transmit Code Word Bit 12
11	TxToggle	RO	0x0	0x0	Toggle Transmit Code Word Bit 11
10:0	TxData	R/W	0x001	0x001	Message/Unformatted Field Transmit Code Word Bit 10:0

Table 41: Link Partner Next Page Register
Register 8

Bits	Field	Mode	HW Rst	SW Rst	Description
15	RxNxtPage	RO	0x0	0x0	If Reg8NxtPg (16.12) is enabled, then next page is stored in the Link Partner Next Page register; otherwise, the Link Partner Next Page register is cleared to all 0ís. Received Code Word Bit 15
14	RxAck	RO	0x0	0x0	Acknowledge Received Code Word Bit 14 0 = Link partner not capable of next page 1 = Link partner capable of next page
13	RxMessage	RO	0x0	0x0	Message Page Received Code Word Bit 13
12	RxAck2	RO	0x0	0x0	Acknowledge 2 Received Code Word Bit 12
11	RxToggle	RO	0x0	0x0	Toggle Received Code Word Bit 11
10:0	RxData	RO	0x000	0x000	Message/Unformatted Field Received Code Word Bit 10:0

Table 42: PHY Specific Control Register
Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	
14	EDet	R/W	0x0	Retain	Energy Detect 0 = Disable 1 = Enable with sense and pulse Enable with sense only is not supported
13	DisNLP Check	R/W	0x0	0x0	Disable Normal Linkpulse Check Linkpulse check and generation disable have no effect, if Auto-Negotiation is enabled locally. 0 = Enable linkpulse check 1 = Disable linkpulse check
12	Reg8NxtPg	R/W	0x0	0x0	Enable the Link Partner Next Page register to store Next Page. If set to store next page in the Link Partner Next Page register (register 8), then 802.3u is violated to emulate 802.3ab. 0 = Store next page in the Link Partner Ability Register (Base Page) register (register 5). 1 = Store next page in the Link Partner Next Page register.
11	DisNLPGen	R/W	0x0	0x0	Disable Linkpulse Generation. Linkpulse check and generation disable have no effect, when Auto-Negotiation is enabled locally. 0 = Enable linkpulse generation 1 = Disable linkpulse generation
10	Reserved	R/W	0x0	0x0	Set to 0
9	DisScrambler	R/W	0x0	Retain	Disable Scrambler If either 100BASE-FX or 10BASE-T forced mode is selected, then the scrambler is disabled at hardware reset. However, when 100BASE-TX is selected, this register bit equals 0. 0 = Enable scrambler 1 = Disable scrambler
8	DisFEFI	R/W	0x1	Retain	Disable FEFI FEFI is automatically disabled regardless of the state of this bit if copper mode is selected. 0 = Enable FEFI 1 = Disable FEFI

Table 42: PHY Specific Control Register (Continued)
Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
7	ExtdDistance	R/W	0x0	0x0	Enable Extended Distance When using cable exceeding 100 meters, the 10BASE-T receive threshold must be lowered in order to detect incoming signals. 0 = Normal 10BASE-T receive threshold 1 = Lower 10BASE-T receive threshold
6	SIGDET Polarity	R/W	0x0	Update	0 = SIGDET Active High 1 = SIGDET Active Low
5:4	AutoMDI[X]	R/W	See Desc.	Update	MDI/MDIX Crossover During Hardware Reset register 16.5:4 defaults as follows ENA_XC 16.5:4 0 00 1 11 This setting can be changed by writing to these bits followed by software reset. 00 = Transmit on pins MDIP/N[0], Receive on pins MDIP/N[1] 01 = Transmit on pins MDIP/N[1], Receive on pins MDIP/N[0] 1x = Enable Automatic Crossover
3	Reserved	R/W	0x0	Retain	
2	SQE Test	R/W	0x0	Retain	SQE Test is automatically disabled in full duplex mode 0 = Disable SQE Test 1 = Enable SQE Test
1	AutoPol	R/W	0x0	0x0	Polarity Reversal If Automatic polarity is disabled, then the polarity is forced to be normal in 10BASE-T mode. Polarity reversal has no effect in 100BASE-TX mode. This bit only controls polarity correction at the inputs. The output polarity is not programmable. 0 = Enable automatic polarity reversal 1 = Disable automatic polarity reversal
0	DisJabber	R/W	0x0	0x0	Disable Jabber Jabber has no effect in full-duplex or in 100BASE-X mode. 0 = Enable jabber function 1 = Disable jabber function

Table 43: PHY Specific Status Register
Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	0
14	ResSpeed	RO	0x1	Retain	Resolved Speed The values are updated after the completion of Auto-Negotiation. The registers retain their values during software reset. This bit is valid only after the resolved bit 11 is set. 0 = 10 Mbps 1 = 100 Mbps.
13	ResDuplex	RO	0x1	Retain	Resolved Duplex Mode The values are updated after the completion of Auto-Negotiation. The registers retain their values during software reset. This bit is valid only after the resolved bit 11 is set. 0 = Half-duplex 1 = Full-duplex
12	RcvPage	RO, LH	0x0	0x0	Page Receive Mode 0 = Page not received 1 = Page received
11	Resolved	RO	0x0	0x0	Speed and Duplex Resolved. Speed and duplex bits (14 and 13) are valid only after the Resolved bit is set. The Resolved bit is set when Auto-Negotiation has resolved the highest common capabilities or Auto-Negotiation is disabled. 0 = Not resolved 1 = Resolved
10	RTLink	RO	0x0	0x0	Link (real time) 0 = Link down 1 = Link up
9:7	Reserved	RES	Always 000	Always 000	Always 000.
6	MDI/MDIX	RO	0x0	0x0	MDI/MDIX Crossover Status 0 = Transmit on pins TXP/TXN, Receive on pins RXP/RXN 1 = Transmit on pins RXP/RXN, Receive on pins TXP/TXN
5	Reserved	RES	Always 0	Always 0	Always 0.
4	Sleep	RO	0x0	0x0	Energy Detect Status 0 = Chip is not in sleep mode (Active) 1 = Chip is in sleep mode (No wire activity)

Table 43: PHY Specific Status Register (Continued)
Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
3:2	Reserved	RES	Always 00	Always 00	Always 00.
1	RTPolarity	RO	0x0	0x0	Polarity (real time) 0 = Normal 1 = Reversed
0	RTJabber	RO	0x0	Retain	Jabber (real time) 0 = No Jabber 1 = Jabber

Table 44: PHY Interrupt Enable
Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	0
14	SpeedIntEn	R/W	0x0	Retain	Speed Changed Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
13	DuplexIntEn	R/W	0x0	Retain	Duplex Changed Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
12	RxPageIntEn	R/W	0x0	Retain	Page Received Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
11	AnegDone IntEn	R/W	0x0	Retain	Auto-Negotiation Completed Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
10	LinkIntEn	R/W	0x0	Retain	Link Status Changed Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
9	SymErrIntEn	R/W	0x0	Retain	Symbol Error Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
8	FlsCrsIntEn	R/W	0x0	Retain	False Carrier Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
7	FIFOErrInt	R/W	0x0	Retain	FIFO Over/Underflow Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable

Table 44: PHY Interrupt Enable Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
6	MDI[x]IntEn	R/W	0x0	0x0	MDI/MDIX Crossover Changed Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
5	Reserved	RES	0x0	Retain	Must be 0.
4	EDetIntEn	R/W	0x0	Retain	Energy Detect Interrupt Enable 0 = Disable 1 = Enable
3:2	Reserved	RES	0x0	Retain	Must be 00.
1	PolarityIntEn	R/W	0x0	Retain	Polarity Changed Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable
0	JabberIntEn	R/W	0x0	Retain	Jabber Interrupt Enable 0 = Interrupt disable 1 = Interrupt enable

Table 45: PHY Interrupt Status Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	0
14	SpeedInt	RO, LH	0x0	0x0	Speed Changed 0 = Speed not changed 1 = Speed changed
13	DuplexInt	RO, LH	0x0	0x0	Duplex Changed 0 = Duplex not changed 1 = Duplex changed
12	RxPageInt	RO, LH	0x0	0x0	0 = Page not received 1 = Page received
11	AnegDoneInt	RO, LH	0x0	0x0	Auto-Negotiation Completed 0 = Auto-Negotiation not completed 1 = Auto-Negotiation completed
10	LinkInt	RO, LH	0x0	0x0	Link Status Changed 0 = Link status not changed 1 = Link status changed
9	SymErrInt	RO, LH	0x0	0x0	Symbol Error 0 = No symbol error 1 = Symbol error
8	FlsCrsInt	RO, LH	0x0	0x0	False Carrier 0 = No false carrier 1 = False carrier
7	FIFOErrInt	RO, LH	0x0	0x0	FIFO Over /Underflow Error 0 = No over/underflow error 1 = Over/underflow error
6	MDIMDIXInt	RO, LH	0x0	0x0	MDI/MDIX Crossover Changed 0 = MDI/MDIX crossover not changed 1 = MDI/MDIX crossover changed
5	Reserved	RO	Always 0	Always 0	Always 0
4	EDetChg	RO, LH	0x0	0x0	Energy Detect Changed 0 = No Change 1 = Changed
3:2	Reserved	RO	Always 00	Always 00	Always 00
1	PolarityInt	RO	0x0	0x0	Polarity Changed 0 = Polarity not changed 1 = Polarity changed

Table 45: PHY Interrupt Status (Continued)
Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
0	JabberInt	RO, LH	0x0	0x0	Jabber Mode 0 = No Jabber 1 = Jabber

Table 46: PHY Interrupt Port Summary
Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RO	0x0000	0x0000	

Table 47: Receive Error Counter
Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RxErrCnt	RO	0x0000	0x0000	Receive Error Count This register counts receive errors on the media inter face. When the maximum receive error count reaches 0xFFFF, the counter will roll over.

Table 48: LED Parallel Select Register
Register 22

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x4	Retain	
11:8	LED2	R/W	0xA	Retain	LED2 Control. This is a global setting. 0000 = COLX 0001 = ERROR 0010 = DUPLEX 0011 = DUPLEX/COLX 0100 = SPEED 0101 = LINK 0110 = TX 0111 = RX 1000 = ACT 1001 = LINK/RX 1010 = LINK/ACT 1011 = ACT (Blink mode) 1100 = TX (Blink Mode) 1101 = RX (Blink Mode) 1110 = Interrupt 1111 = Force to 1 (inactive)
7:4	LED1	R/W	0x4	Retain	LED1 Control. This is a global setting. 0000 = COLX 0001 = ERROR 0010 = DUPLEX 0011 = DUPLEX/COLX 0100 = SPEED 0101 = LINK 0110 = TX 0111 = RX 1000 = ACT 1001 = LINK/RX 1010 = LINK/ACT 1011 = ACT (Blink mode) 1100 = TX (Blink Mode) 1101 = RX (Blink Mode) 1110 = COLX (Blink Mode) 1111 = Force to 1 (inactive)

Table 48: LED Parallel Select Register (Continued)
Register 22

Bits	Field	Mode	HW Rst	SW Rst	Description
3:0	LED0	R/W	0x4	Retain	LED0 Control. This is a global setting. 0000 = COLX 0001 = ERROR 0010 = DUPLEX 0011 = DUPLEX/COLX 0100 = SPEED 0101 = LINK 0110 = TX 0111 = RX 1010 = LINK/ACT 1011 = ACT (Blink mode) 1100 = TX (Blink Mode) 1101 = RX (Blink Mode) 1110 = COLX (Blink Mode) 1111 = Force to 1 (inactive)

Table 49: PHY LED Control Register
Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0	Always 0	Must be 0.
14:12	PulseStretch	R/W	0x4	Retain	Pulse stretch duration. This is a global setting. 000 = No pulse stretching 001 = 21 ms to 42 ms 010 = 42 ms to 84 ms 011 = 84 ms to 170 ms 100 = 170 ms to 340 ms 101 = 340 ms to 670 ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s
11:9	BlinkRate	R/W	0x1	Retain	Blink Rate. This is a global setting. 000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved
8:6	LED2 Speed	R/W	0x0	Retain	LED 2 Speed Select 000 = Active for 10BASE-T Link 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Active for 100BASE-X 110 = Reserved 111 = Reserved
5:3	LED1 Speed	R/W	0x0	Retain	LED 1 Speed Select 000 = Active for 10BASE-T Link 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Active for 100BASE-X 110 = Reserved 111 = Reserved

Table 49: PHY LED Control Register (Continued)
Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
2:0	LED0 Speed	R/W	0x5	Retain	LED 0 Speed Select 000 = Active for 10BASE-T Link 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Active for 100BASE-X 110 = Reserved 111 = Reserved

Table 50: PHY Manual LED Override
Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	0
14	InvLED2	R/W	0x0	Retain	Invert LED2. This bit controls the active level of the LED2 pin. 0 = Active Low LED2 1 = Active High LED2
13	InvLED1	R/W	0x0	Retain	Invert LED1. This bit controls the active level of the LED1 pin. 0 = Active Low LED1 1 = Active High LED1
12	InvLED0	R/W	0x0	Retain	Invert LED0. This bit controls the active level of the LED0 pin. 0 = Active Low LED0 1 = Active High LED0
11:6	Reserved	R/W	0x00	Retain	000000
5:4	ForceLED2	R/W	0x0	Retain	00 = Normal 01 = Blink[1] 10 = LED Off 11 = LED On
3:2	ForceLED1	R/W	0x0	Retain	00 = Normal 01 = Blink 10 = LED Off 11 = LED On
1:0	ForceLED0	R/W	0x0	Retain	00 = Normal 01 = Blink 10 = LED Off 11 = LED On

Table 51: VCT™ Register for MDIP/N[0] Pins Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	EnVCT	R/W, SC	0x0	0x0	Enable VCT 0 = VCT completed 1 = Run VCT After running VCT once, bit 15 = 0 indicates VCT completed. The cable status is reported in the VCTTst bits in registers 26 and 27. Refer to the Virtual Cable Tester® feature.
14:13	VCTTst	RO	0x0	Retain	VCT Test Status These VCT test status bits are valid after completion of VCT. 00 = Valid test, normal cable (no short or open in cable) 01 = Valid test, short in cable (Impedance < 33 ohm) 10 = Valid test, open in cable (Impedance > 333 ohm) 11 = Test fail
12:8	AmpRfln	RO	0x00	Retain	Amplitude of Reflection The amplitude of reflection is stored in these register bits. These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude 0x13 = Zero amplitude 0x07 = Maximum negative amplitude These bits are valid after completion of VCT (bit 15) and if the VCT test status bits (bits 14:13) have not indicated test failure.
7:0	DistRfln	RO	0x00	Retain	Distance of Reflection These bits refer to the approximate distance (± 1m) to the open/short location, measured at nominal conditions (room temperature and typical VDDs) These bits are valid after completion of VCT (bit 15) and if the VCT test status bits (bit 14:13) have not indicated test failure.

Table 52: VCT™ Register for MDIP/N[1] Pins
Register 27

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0	Always 0	Reserved
14:13	VCTTst	RO	0x0	Retain	VCT Test Status The VCT test status bits are valid after completion of VCT. 00 = Valid test, normal cable (no short or open in cable) 01 = Valid test, short in cable (Impedance < 33 ohm) 10 = Valid test, open in cable (Impedance > 333 ohm) 11 = Test fail
12:8	AmpRfln	RO	0x00	Retain	Amplitude of Reflection The amplitude of reflection is stored in these register bits. These amplitude bits range from 0x07 to 0x1F. 0x1F = Maximum positive amplitude 0x13 = Zero amplitude 0x07 = Maximum negative amplitude These bits are valid after completion of VCT (bit 15) and if VCT test status bits (bit 14:13) have not indicated test failure.
7:0	DistRfln	RO	0x00	Retain	Distance of Reflection These bits refer to the approximate distance (± 1m) to the open/short location, measured at nominal conditions (room temperature and typical VDDs) These bits are valid after completion of VCT (bit 15) and if VCT test status bits (bits 14:13) have not indicated test failure.

Table 53: PHY Specific Control Register II
Register 28

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x0	Retain	Must be 0000
11:10	MAC Interface Mode	R/W	See Desc.	Update	During Hardware Reset register 28.11:10 defaults as follows MODE[2:0] 28.11:10 000 00 001 01 010 00 011 10 100 10 110 11 111 01 00 = RGMII where receive clock transition when data transitions 01 = RGMII where receive clock transition when data stable 10 = Non-Source Synchronous MII 11 = Source Synchronous MII
9:5	Reserved	R/W	0x00	Update	Set to 00000
4	EnLineLpbk	R/W	0x0	Retain	0 = Disable Line Loopback 1 = Enable Line Loopback
3	SoftwareMedia Select	R/W	See Desc.	Update	During Hardware Reset register 28.3 defaults as follows MODE[2:0] 28.3 000 0 001 0 010 1 011 0 100 1 110 0 111 1 0 = Select Copper Media 1 = Select Fiber Media
2	TDRWaitTime	R/W	0x0	Retain	0 = Wait time is 1.5s before TDR test is started 1 = Wait time is 25 ms before TDR test is started
1	EnRXCLK	R/W	0x1	Update	0 = Disable MAC interface clock (RXCLK) in sleep mode 1 = Enable MAC interface clock (RXCLK) in sleep mode
0	SelClsA	R/W	0x0	Update	0 = Select Class B driver (typically used in CAT 5 applications) 1 = Select Class A driver - available for 100BASE-TX mode only (typically used in Backplane or direct connect applications, but may be used with CAT 5 applications)

Table 54: Test Mode Select Register 29

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	R/W	0x000	Retain	Must set to all 0s.
4:0	Page	R/W	0x00	Retain	Register 30 Page

Table 55: CRC Status Register Register 30_9

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	CRC Error Count	RO	0x00	Retain	Represents the CRC Error count for received packets since 30_9.0 is set
7:1	Reserved	R/W	Always 0	0x00	0000000
0	CRC Enable	R/W	0x0	Retain	1=Enable CRC checker for all ports. 0=Disable CRC checker for all ports

Table 56: MAC Interface Output Impedance Calibration Override Register 30_10

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Restart Calibration	R/W, SC	0x0	Retain	Calibration will start once bit 15 is set to 1. 0 = Normal 1 = Restart
14	Calibration Complete	RO	0x0	Retain	Calibration is done once bit 14 becomes 1. 0 = Not done 1 = Done
13	Reserved	R/W	0x0	Retain	0
12:8	PMOS Value	R/W	See Descr	Retain	00000 = all fingers off 11111 = all fingers on The automatic calibrated values are stored here after calibration completes. Once LATCH is set to 1 the new calibration value is written into the I/O pad. The automatic calibrated value is lost.
7	Reserved	RW	0x0	Retain	0
6	LATCH	R/W, SC	0x0	Retain	1 = Latch in new value. This bit self clears. (Used for manual settings)
5	PMOS/NMOS Select	R/W	0x0	Retain	0 = NMOS value written when LATCH is set to 1. 1 = PMOS value written when LATCH is set to 1.
4:0	NMOS value	R/W	See Descr	Retain	00000 = All fingers off 11111 = All fingers on The automatic calibrated values are stored here after calibration completes. Once LATCH is set to 1 the new calibration value is written into the I/O pad. The automatic calibrated value is lost.

Table 57: MAC Interface Output Impedance Target Register 30_11

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	000000000
6:4	Calibration PMOS Target Impedance	RW	0x4	Retain	000 = 80 Ohm 001 = 69 Ohm 010 = 61 Ohm 011 = 54 Ohm 100 = 49 Ohm 101 = 44 Ohm 110 = 41 Ohm 111 = 38 Ohm
3	Reserved	RO	0x0	0x0	0
2:0	Calibration NMOS Target Impedance	RW	0x4	Retain	000 = 80 Ohm 001 = 69 Ohm 010 = 61 Ohm 011 = 54 Ohm 100 = 49 Ohm 101 = 44 Ohm 110 = 41 Ohm 111 = 38 Ohm

Section 4. Electrical Specifications

4.1. Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Typ	Max	Units
V_{DDA}	Power Supply Voltage on AVDD with respect to VSS	-0.5		3.6	V
V_{DDAC}	Power Supply Voltage on AVDDC with respect to VSS	-0.5		3.6	V
V_{DDAR}	Power Supply Voltage on AVDDR with respect to VSS	-0.5		3.6	V
V_{DDAX}	Power Supply Voltage on AVDDX with respect to VSS	-0.5		3.6	V
V_{DD}	Power Supply Voltage on VDD with respect to VSS	-0.5		3.6	V
V_{DDO}	Power Supply Voltage on VDDO with respect to VSS	-0.5		3.6	V
V_{DDOR}	Power Supply Voltage on VDDOR with respect to VSS	-0.5		3.6	V
V_{PIN}	Voltage applied to any digital input pin	-0.5		VDDO(R) + 0.7, whichever is less	V
$T_{STORAGE}$	Storage temperature	-55		+125[1]	°C

1. 125 °C is only used as bake temperature for not more than 24 hours. Long term storage (e.g weeks or longer) should be kept at 85 °C or lower.

4.2. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDA}[1]	AVDD supply	For AVDD	2.38	2.5	2.62	V
V_{DDAC}[1]	AVDDC supply	For AVDDC at 2.5V	2.38	2.5	2.62	V
		For AVDDC at 3.3V	3.14	3.3	3.46	V
V_{DDAR}[1]	AVDDR supply	For AVDDR	2.38	2.5	2.62	V
V_{DDAX}[1]	AVDDX supply	For AVDDX at 3.3V	3.14	3.3	3.46	V
V_{DD}[1]	DVDD supply	For DVDD	1.14	1.2	1.26	V
V_{DDO}[1]	VDDO supply	For VDDO at 2.5V	2.38	2.5	2.62	V
		For VDDO at 3.3V	3.14	3.3	3.46	V
V_{DDOR}[1]	VDDOR supply	For VDDOR at 2.5V	2.38	2.5	2.62	V
		For VDDOR at 3.3V	3.14	3.3	3.46	V
RSET	Internal bias reference	Resistor connected to V_{SS}	1980	2000	2020	Ω
T_A	Ambient operating temperature	Commercial parts	0		70[2]	°C
		Industrial parts[3]	-40		85	°C
T_J	Maximum junction temperature				125[4]	°C

1. Maximum noise allowed on supplies is 50 mV peak-peak.
2. Commercial operating temperatures are typically below 70 °C, e.g, 45 °C ~55 °C. The 70 °C max is Marvell® specification limit
3. Industrial part numbers have an "I" following the commercial part numbers. See "“Ordering Part Numbers and Package Markings” on page 123 for details.
4. Refer to white paper on TJ Thermal Calculations for more information.

4.3 Package Thermal Information

4.3.1 88E3015 Device 56-Pin QFN package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance - junction to ambient of the 56-Pin QFN package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		33.40		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		29.50		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		28.20		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		27.50		C/W
ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the 56-Pin QFN package $\psi_{JT} = (T_J-T_C)/P.$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.55		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		0.94		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		1.19		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		1.33		C/W
θ_{JC}	Thermal resistance[1] - junction to case for the 56-Pin QFN package $\theta_{JC} = (T_J - T_C)/ PTop$ PTop = Power Dissipation from the top of the package	JEDEC with no air flow		17.90		°C/W
θ_{JB}	Thermal resistance[1] - junction to board for the 56-Pin QFN package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		21.80		°C/W

1. Refer to white paper TJ Thermal Calculations for more information.

4.3.2 88E3018 Device 64-Pin QFN package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance - junction to ambient of the 64-Pin QFN package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow		32.40		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		28.60		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		27.40		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		26.70		°C/W
ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the 64-Pin QFN package $\psi_{JT} = (T_J-T_C)/P$. P = Total Power Dissipation	JEDEC 4 in. x 4.5 in. 4-layer PCB with no air flow		0.52		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		0.89		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		1.12		°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		1.26		°C/W
θ_{JC}	Thermal resistance[1] - junction to case for the 64-Pin QFN package $\theta_{JC} = (T_J - T_C)/ PTop$ PTop = Power Dissipation from the top of the package	JEDEC with no air flow		17.30		°C/W
θ_{JB}	Thermal resistance[1] - junction to board for the 64-Pin QFN package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		21.10		°C/W

1. Refer to white paper TJ Thermal Calculations for more information.

4.4 Current Consumption

Note

The following current consumption numbers are shown when external supplies are used. If internal regulators are used, the current consumption will not change; however, the power consumed inside the package will increase.

4.4.1 Current Consumption AVDD + Center Tap

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ[1,2]	Max	Units
I_{DDA}	2.5V Power to analog core, analog I/O	AVDD	10BASE-T idle		25		mA
			10BASE-T with traffic		90		mA
			100BASE-TX with traffic or idle		54		mA
			Auto-Negotiation with no link		25		mA
			100BASE-FX with traffic or idle		57		mA
			COMA		7		mA
			Sleep (Energy Detect+™)		25		mA
			Power Down		7		mA

1. The values listed are typical values with three LEDs and Auto-Negotiation on.
2. If the 2.5V PNP option is used, then this current is consumed by AVDDX.

4.4.2 Current Consumption AVDDC

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ[1]	Max	Units
I_{DDC}	2.5V/3.3V Power to analog core	AVDDC	10BASE-T idle		5		mA
			10BASE-T with traffic		5		mA
			100BASE-TX with traffic or idle		5		mA
			Auto-Negotiation with no link		5		mA
			100BASE-FX with traffic or idle		4		mA
			COMA		4		mA
			Sleep (Energy Detect+™)		4		mA
			Power Down		4		mA

1. The values listed are typical values with three LEDs and Auto-Negotiation on.

Note

The following current consumption numbers are shown when external supplies are used. If internal regulators are used, the current consumption will not change; however, the power consumed inside the package will increase.

4.4.3 Current Consumption DVDD

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ[1,2]	Max	Units
I_{DD}	1.2V Power to digital I/O	DVDD	10BASE-T idle		7		mA
			10BASE-T with traffic		8		mA
			100BASE-TX with traffic or idle		25		mA
			Auto-Negotiation with no link		7		mA
			100BASE-FX with traffic or idle		11		mA
			COMA		4		mA
			Sleep (Energy Detect+™)		8		mA
			Power Down		4		mA

1. The values listed are typical values with three LEDs and Auto-Negotiation on.
2. If the internal 1.2V regulator is used, the DVDD current is consumed by AVDDR.

4.4.4 Current Consumption VDDO + VDDOR

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ[1]	Max	Units
I_{DDO}	2.5V/3.3V non-MAC Interface digital I/O and MAC Interface digital I/O	VDDO	10BASE-T idle		1		mA
			10BASE-T with traffic		5		mA
			100BASE-TX with traffic or idle		8		mA
			Auto-Negotiation with no link		1		mA
			100BASE-FX with traffic or idle		9		mA
			COMA		3		mA
			Sleep (Energy Detect+™)		1		mA
			Power Down		2		mA

1. The values listed are typical values with three LEDs and Auto-Negotiation on.

4.5. DC Operating Conditions

4.5.1 Non-MAC Interface Digital Pins

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

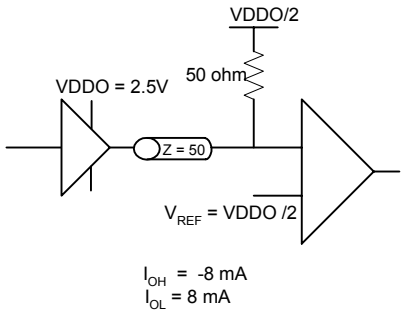
Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
VIH	Input high voltage	All digital inputs	VDDO = 3.3V	2.31			V
			VDDO = 2.5V	1.75			V
VIL	Input low voltage	All digital inputs	VDDO = 3.3V			0.99	V
			VDDO = 2.5V			0.75	V
VOH	High level output voltage	All digital outputs	IOH = -4 mA	VDDO - 0.4V			V
VOL	Low level output voltage	All digital outputs	IOL = 4 mA			0.4	V
I_{ILK}	Input leakage current	With internal pull-up resistor				10 -50	uA
		All others without resistor				10	uA
CIN	Input capacitance	All pins				5	pF

Table 58: 88E3018 Device Internal Resistor Description

88E3015 Device Pin #	88E3018 Device Pin #	Pin Name	Resistor
--	13	TCK	Internal pull-up
--	14	TMS	Internal pull-up
--	37	TRSTn	Internal pull-up
--	12	TDI	Internal pull-up
22	4	COMAn	Internal pull-up

4.5.2 Stub-Series Transceiver Logic (SSTL_2)

Figure 16: SSTL_2 Termination Circuit



Note

This circuit can be used if termination is required. This circuit can also be used unterminated if the interconnect is short.

Figure 17: SSTL_2 Input Voltage Levels

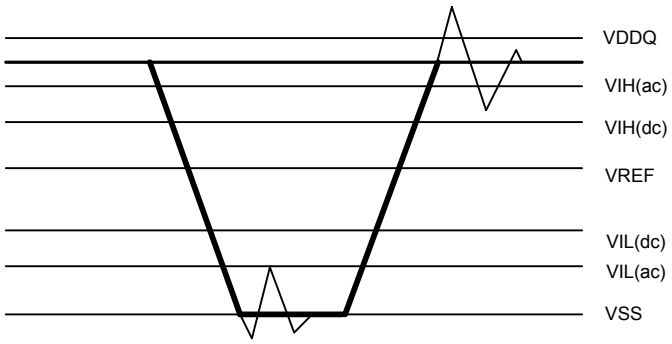


Table 59: Reference I/O Parameters[1]

Parameter	Description	Corner	2.5V SSTL_2	3.3V SSTL_2	Units
VDDQ	Output Supply Voltage	min	2.38	3.14	V
		nom	2.5	3.3	V
		max	2.62	3.46	V
VREF	Input Reference Voltage	min	1.19	1.57	V
		nom	1.25	1.65	V
		max	1.31	1.73	V
VTT	Termination Voltage	min	VREF - 0.04		V
		nom	VREF		V
		max	VREF + 0.04		V
VIH(dc)	DC Input Logic High	min	VREF + 0.18	VREF + 0.25	V
		max	VDDQ + 0.30	VDDQ + 0.30	V
VIL(dc)	DC Input Logic Low	min	- 0.30	- 0.30	V
		max	VREF - 0.18	VREF - 0.25	V
VIH(ac)	AC Input Logic High	min	VREF + 0.35	VREF + 0.50	V
		max	--	--	V
VIL(ac)	AC Input Logic Low	min	--	--	V
		max	VREF - 0.35	VREF - 0.50	V
VOH(dc)	DC Output Logic High	min			V
		max			V
VOL(dc)	DC Output Logic Low	min			V
		max			V
VOH(ac)	AC Output Logic High	min	VTT + 0.57	VTT + 0.9	V
		max	--		V
VOL(ac)	AC Output Logic Low	min	--		V
		max	VTT - 0.57	VTT - 0.9	V
IOH(dc)	Output Minimum Source DC Current	min	7.60	7.60	mA
		max	--	--	mA
IOL(dc)	Output Minimum Sink DC Current	min	7.60	7.60	mA
		max	--	--	mA
	Input Timing Reference Level		VREF	VREF	V
	Input Signal Swing		1.5	2.0	V
	Input Signal Edge Rate		± 1.0	± 1.0	V/ns
	Output Timing Reference Level		VDDQ/2	VDDQ/2	V

1. These numbers are preliminary. Marvell® reserves the right to change these parameters.

4.5.3 IEEE DC Transceiver Parameters

IEEE tests are typically based on template and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications.

- 10BASE-T IEEE 802.3 Clause 14
- 100BASE-TX ANSI X3.263-1995

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{ODIFF}	Absolute peak differential output voltage	MDIP/N[0] MDIP/N[1]	10BASE-T no cable	2.2	2.5	2.8	V
		MDIP/N[0] MDIP/N[1]	10BASE-T cable model	585[1]			mV
		MDIP/N[0] MDIP/N[1]	100BASE-FX mode	0.4	0.8	1.2	V
		MDIP/N[0] MDIP/N[1]	100BASE-TX mode	0.950	1.0	1.05	V
	Overshoot	MDIP/N[0] MDIP/N[1]	100BASE-TX mode	0		5%	V
	Amplitude symmetry (P/N)	MDIP/N[0] MDIP/N[1]	100BASE-TX mode	0.98x		1.02x	V+/V-
V_{IDIFF}	Peak differential input voltage accept level	MDIP/N[0] MDIP/N[1]	10BASE-T mode	585[2]			mV
		MDIP/N[0] MDIP/N[1]	100BASE-FX mode	200			mV
	Peak differential input voltage reject level	MDIP/N[0] MDIP/N[1]	100BASE-FX mode	100			mV
	Signal detect assertion	MDIP/N[0] MDIP/N[1]	100BASE-TX mode	1000	460[3]		mV peak-peak
	Signal detect de-assertion	MDIP/N[0] MDIP/N[1]	100BASE-TX mode	200	360[4]		mV peak-peak

1. IEEE 802.3 Clause 14-2000, Figure 14.9 shows the template for the “far end” wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
2. The input test is actually a template test, IEEE 802.3 Clause 14-2000. Figure 14.17 shows the template for the receive wave form.
3. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode). The will accept signals typically with 460 mV peak-to-peak differential amplitude.
4. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude less than 200 mV should be de-assert signal detect (internal signal in 100BASE-TX mode). The will reject signals typically with peak-to-peak differential amplitude less than 360 mV.

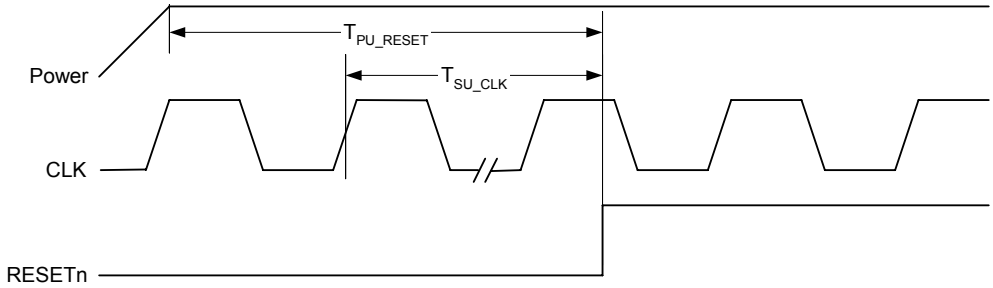
4.6 AC Electrical Specifications

4.6.1 Reset and Configuration Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Power up to hardware de-asserted		10			ms
T_{SU_CLK}	Number of valid REFCLK cycles prior to RESETn de-asserted		10			clks

Figure 18: Reset Timing



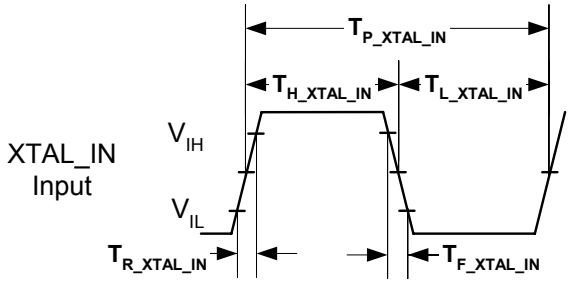
4.6.2 XTAL_IN Input Clock Timing[1]

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_XTAL\_IN}$	XTAL_IN Period	25 MHz	40 -50 ppm	40	40 +50 ppm	ns
$T_{H\_XTAL\_IN}$	XTAL_IN High time	25 MHz	14	20	26	ns
$T_{L\_XTAL\_IN}$	XTAL_IN Low time	25 MHz	14	20	26	ns
$T_{R\_XTAL\_IN}$	XTAL_IN Rise	V_{IL}(max) to V_{IH}(min) - 25 MHz	-	3.0	-	ns
$T_{F\_XTAL\_IN}$	XTAL_IN Fall	V_{IH}(min) to V_{IL}(max) - 25 MHz	-	3.0	-	ns
$T_{J\_XTAL\_IN}$	XTAL_IN total jitter[2]	25 MHz	-	-	200	ps[3]

1. If the crystal option is used, ensure that the frequency is 25 MHz ± 50 ppm. Capacitors must be chosen carefully - see application note supplied by the crystal vendor.
2. PLL generated clocks are not recommended as input to XTAL_IN since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.
3. Broadband peak-peak = 200 ps, Broadband rms = 3 ps, 12 kHz to 20 MHz rms = 1 ps.

Figure 19: Clock Timing



4.7 MII Interface Timing

4.7.1 100 Mbps MII Transmit Timing - Non Source Synchronous

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_MII\_TX\_CLK}$	MII Setup Time		15			ns
$T_{HD\_MII\_TX\_CLK}$	MII Hold Time		0			ns
$T_{H\_MII\_TX\_CLK}$	TX_CLK High		18	20	22	ns
$T_{L\_MII\_TX\_CLK}$	TX_CLK Low		18	20	22	ns
$T_{P\_MII\_TX\_CLK}$	TX_CLK Period			40		ns

4.7.2 10 Mbps MII Transmit Timing - Non Source Synchronous

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_MII\_TX\_CLK}$	MII Setup Time		15			ns
$T_{HD\_MII\_TX\_CLK}$	MII Hold Time		0			ns
$T_{H\_MII\_TX\_CLK}$	TX_CLK High		190	200	210	ns
$T_{L\_MII\_TX\_CLK}$	TX_CLK Low		190	200	210	ns
$T_{P\_MII\_TX\_CLK}$	TX_CLK Period			400		ns

4.7.3 100 Mbps MII Transmit Timing - Source Synchronous

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

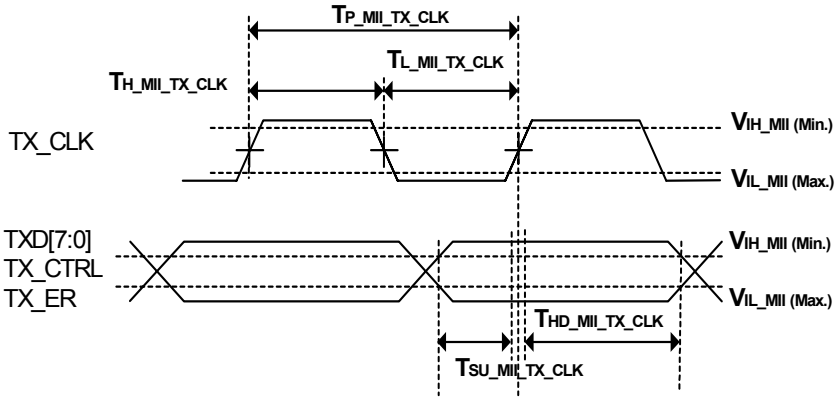
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_MII\_TX\_CLK}$	MII Setup Time		2.75			ns
$T_{HD\_MII\_TX\_CLK}$	MII Hold Time		1.50			ns
$T_{H\_MII\_TX\_CLK}$	TX_CLK High		10	20	30	ns
$T_{L\_MII\_TX\_CLK}$	TX_CLK Low		10	20	30	ns
$T_{P\_MII\_TX\_CLK}$	TX_CLK Period			40		ns

4.7.4 10 Mbps MII Transmit Timing - Source Synchronous

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_MII\_TX\_CLK}$	MII Setup Time		2.75			ns
$T_{HD\_MII\_TX\_CLK}$	MII Hold Time		1.50			ns
$T_{H\_MII\_TX\_CLK}$	TX_CLK High		100	200	300	ns
$T_{L\_MII\_TX\_CLK}$	TX_CLK Low		100	200	300	ns
$T_{P\_MII\_TX\_CLK}$	TX_CLK Period			400		ns

Figure 20: MII Transmit Timing



4.7.5 100 Mbps MII Receive Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

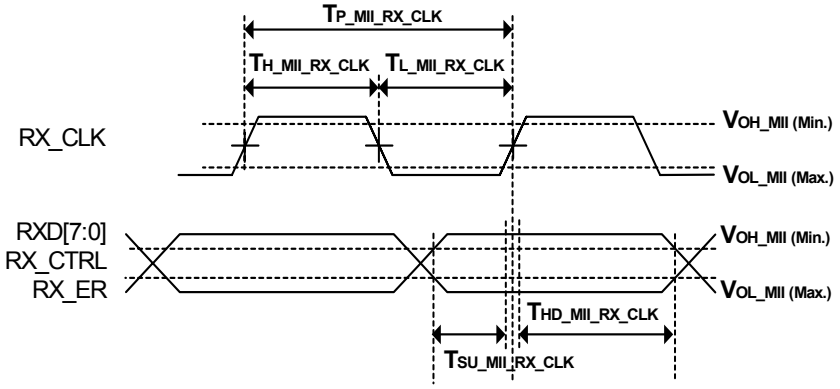
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_MII\_RX\_CLK}$	MII Output to Clock		16			ns
$T_{HD\_MII\_RX\_CLK}$	MII Clock to Output		16			ns
$T_{H\_MII\_RX\_CLK}$	RX_CLK High		18	20	22	ns
$T_{L\_MII\_RX\_CLK}$	RX_CLK Low		18	20	22	ns
$T_{P\_MII\_RX\_CLK}$	RX_CLK Period			40		ns

4.7.6 10 Mbps MII Receive Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_MII\_RX\_CLK}$	MII Output to Clock		190			ns
$T_{HD\_MII\_RX\_CLK}$	MII Clock to Output		190			ns
$T_{H\_MII\_RX\_CLK}$	RX_CLK High		190	200	210	ns
$T_{L\_MII\_RX\_CLK}$	RX_CLK Low		190	200	210	ns
$T_{P\_MII\_RX\_CLK}$	RX_CLK Period			400		ns

Figure 21: MII Receive Timing



4.8 RGMII Interface Timing

4.8.1 RGMII Transmit Timing

4.8.1.1 100 Mbps RGMII Transmit Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

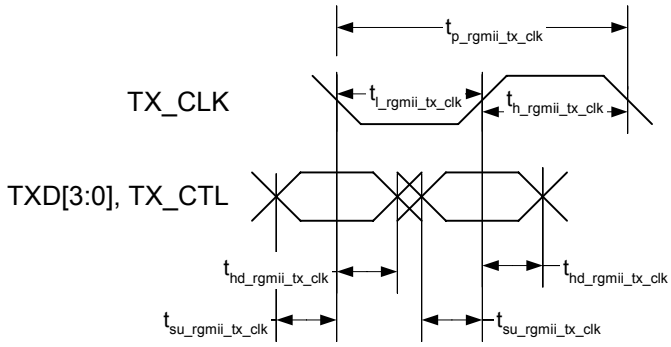
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_RGMII\_TX\_CLK}$	RGMII Setup Time		1.0			ns
$T_{HD\_RGMII\_TX\_CLK}$	RGMII Hold Time		0.8			ns
$T_{H\_RGMII\_TX\_CLK}$	TX_CLK High		10	20	30	ns
$T_{L\_RGMII\_TX\_CLK}$	TX_CLK Low		10	20	30	ns
$T_{P\_RGMII\_TX\_CLK}$	TX_CLK Period			40		ns

4.8.1.2 10 Mbps RGMII Transmit Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_RGMII\_TX\_CLK}$	RGMII Setup Time		1.0			ns
$T_{HD\_RGMII\_TX\_CLK}$	RGMII Hold Time		0.8			ns
$T_{H\_RGMII\_TX\_CLK}$	TX_CLK High		100	200	300	ns
$T_{L\_RGMII\_TX\_CLK}$	TX_CLK Low		100	200	300	ns
$T_{P\_RGMII\_TX\_CLK}$	TX_CLK Period			400		ns

Figure 22: RGMII Transmit Timing



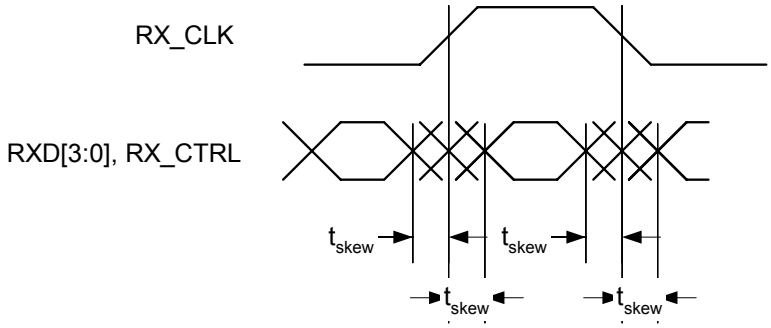
4.8.2 RGMII Receive Timing

4.8.2.1 Register 28.11:10 = 00

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{skew}	All speeds	- 0.5		0.5	ns

Figure 23: RGMII RX_CLK Delay Timing - Register 28.11:10 = 00



4.8.2.2 Register 28.11:10 = 01

100 Mbps RGMII Receive Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

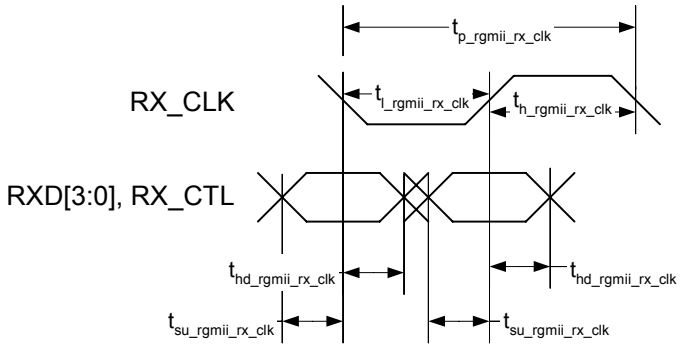
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_RGMII\_RX\_CLK}$	RGMII Output to Clock		5			ns
$T_{HD\_RGMII\_RX\_CLK}$	RGMII Clock to Output		5			ns
$T_{H\_RGMII\_RX\_CLK}$	RX_CLK High		18	20	22	ns
$T_{L\_RGMII\_RX\_CLK}$	RX_CLK Low		18	20	22	ns
$T_{P\_RGMII\_RX\_CLK}$	RX_CLK Period			40		ns

10 Mbps RGMII Receive Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_RGMII\_RX\_CLK}$	RGMII Output to Clock		80			ns
$T_{HD\_RGMII\_RX\_CLK}$	RGMII Clock to Output		80			ns
$T_{H\_RGMII\_RX\_CLK}$	RX_CLK High		190	200	210	ns
$T_{L\_RGMII\_RX\_CLK}$	RX_CLK Low		190	200	210	ns
$T_{P\_RGMII\_RX\_CLK}$	RX_CLK Period			400		ns

Figure 24: RGMII RX_CLK Delay Timing - Register 28.11:10 = 01 (add delay)



4.9 Latency Timing

4.9.1 MII to 100BASE-TX Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

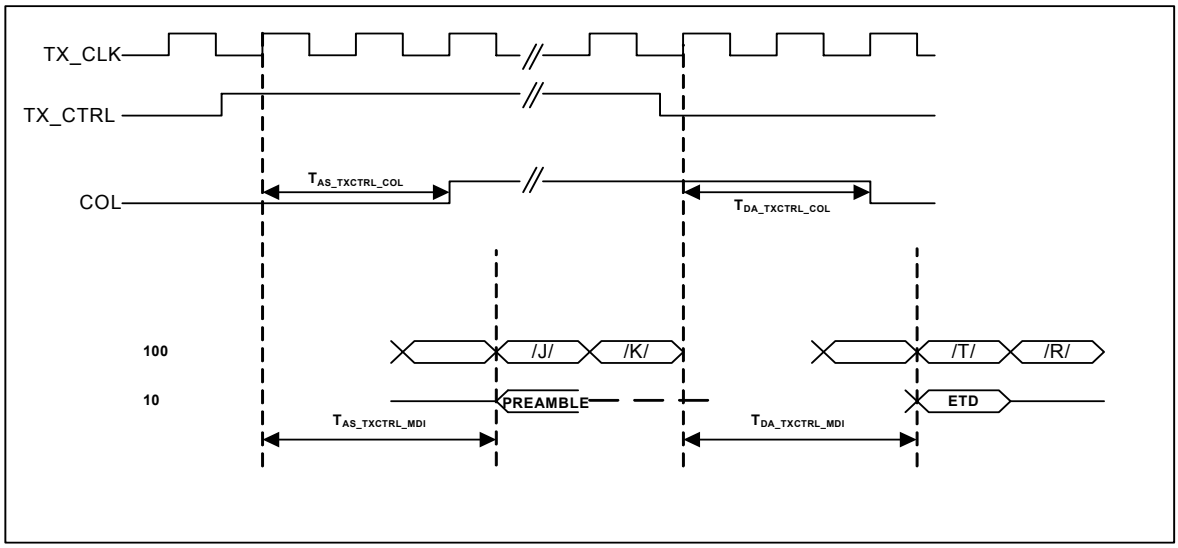
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXCTRL\_COL\_100}$	100BASE-TX TX_CTRL Asserted to COL Asserted		184		202	ns
$T_{AS\_TXCTRL\_MDI\_100}$	100BASE-TX TX_CTRL Asserted to /J/		208		234	ns
$T_{DA\_TXCTRL\_COL\_100}$	100BASE-TX TX_CTRL De-asserted to COL De-asserted		192		210	ns
$T_{DA\_TXCTRL\_MDI\_100}$	100BASE-TX TX_CTRL De-asserted to /T/		208		234	ns

4.9.2 MII to 10BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXCTRL\_COL\_10}$	10BASE-T TX_CTRL Asserted to COL Asserted		1700		1810	ns
$T_{AS\_TXCTRL\_MDI\_10}$	10BASE-T TX_CTRL Asserted to Preamble		1845		1960	ns
$T_{DA\_TXCTRL\_COL\_10}$	10BASE-T TX_CTRL De-asserted to COL De-asserted		1800		1910	ns
$T_{DA\_TXCTRL\_MDI\_10}$	10BASE-T TX_CTRL De-asserted to ETD		1845		1960	ns

Figure 25: MII to 10/100 Transmit Latency Timing



Note

The collision (COL) diagram assumes that the device was already receiving data when transmission started. In half-duplex mode this will cause a collision. Compare this figure with Figure 26.

4.9.3 100BASE-TX to MII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

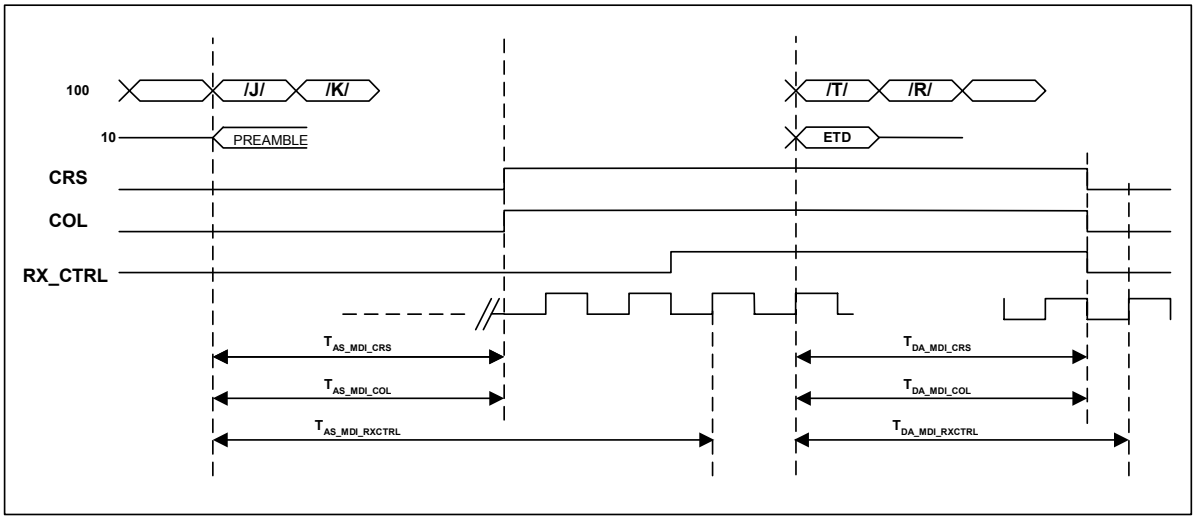
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_CRS\_100}$	100BASE-TX MDI start of Packet to CRS Asserted		128		144	ns
$T_{AS\_MDI\_COL\_100}$	100BASE-TX MDI start of Packet to COL Asserted		128		144	ns
$T_{AS\_MDI\_RXCTRL\_100}$	100BASE-TX MDI start of Packet to RX_CTRL Asserted		239		297	ns
$T_{DA\_MDI\_CRS\_100}$	100BASE-TX MDI /T/ to CRS De-asserted		200		240	ns
$T_{DA\_MDI\_COL\_100}$	100BASE-TX MDI /T/ to COL De-asserted		200		240	ns
$T_{DA\_MDI\_RXCTRL\_100}$	100BASE-TX MDI /T/ to RX_CTRL De-asserted		239		297	ns

4.9.4 10BASE-T to MII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_CRS\_10}$	10BASE-T MDI start of Packet to CRS Asserted		300		510	ns
$T_{AS\_MDI\_COL\_10}$	10BASE-T MDI start of Packet to COL Asserted		300		510	ns
$T_{AS\_MDI\_RXCTRL\_10}$	10BASE-T MDI start of Packet to RX_CTRL Asserted		1400		2010	ns
$T_{DA\_MDI\_CRS\_10}$	10BASE-T MDI ETD to CRS De-asserted		1100		1610	ns
$T_{DA\_MDI\_COL\_10}$	10BASE-T MDI ETD to COL De-asserted		1100		1610	ns
$T_{DA\_MDI\_RXCTRL\_10}$	10BASE-T MDI ETD to RX_CTRL De-asserted		1400		1910	ns

Figure 26: 10/100 to MII Receive Latency Timing



Note

This diagram assumes that the device was already transmitting data when data has started to be received from the link partner. In half-duplex mode this will cause a collision. Compare this figure with Figure 25.

4.9.5 RGMII to 100BASE-TX Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

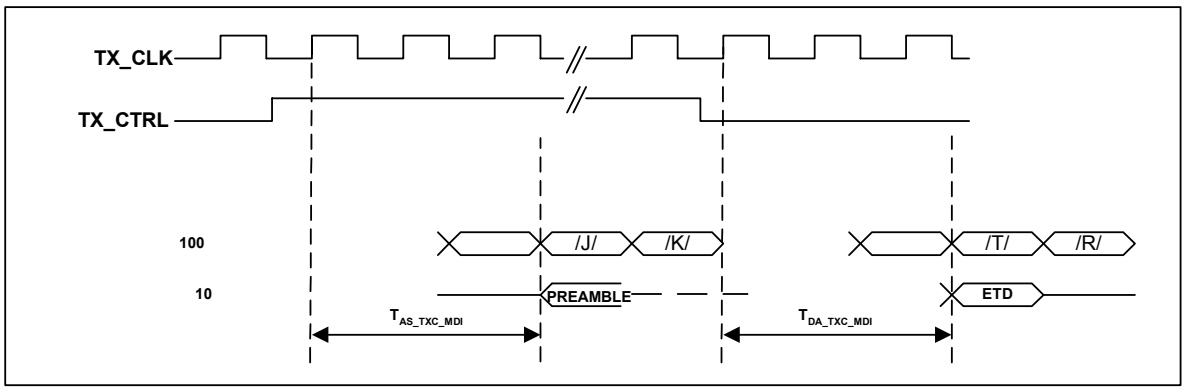
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXC\_MDI\_100}$	100BASE-TX TX_CTRL Asserted to /J/		248		274	ns
$T_{DA\_TXC\_MDI\_100}$	100BASE-TX TX_CTRL De-asserted to /T/		248		274	ns

4.9.6 RGMII to 10BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_TXC\_MDI\_10}$	10BASE-T TX_CTRL Asserted to Preamble		2245		2360	ns
$T_{DA\_TXC\_MDI\_10}$	10BASE-T TX_CTRL De-asserted to ETD		2245		2360	ns

Figure 27: RGMII/MII to 10/100 Transmit Latency Timing



4.9.7 100BASE-TX to RGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

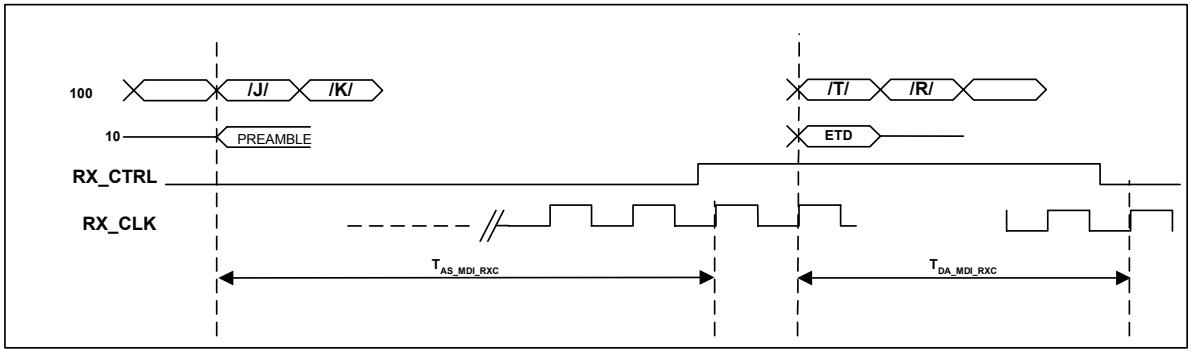
Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_RXC\_100}$	100BASE-TX MDI start of Packet to RX_CTRL Asserted		231		297	ns
$T_{DA\_MDI\_RXC\_100}$	100BASE-TX MDI /T/ to RX_CTRL De-asserted		231		297	ns

4.9.8 10BASE-T to RGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS\_MDI\_RXC\_10}$	10BASE-T MDI start of Packet to RX_CTRL Asserted		1300		1910	ns
$T_{DA\_MDI\_RXC\_10}$	10BASE-T MDI ETD to RX_CTRL De-asserted		1300		1910	ns

Figure 28: 10/100 to RGMII Receive Latency Timing

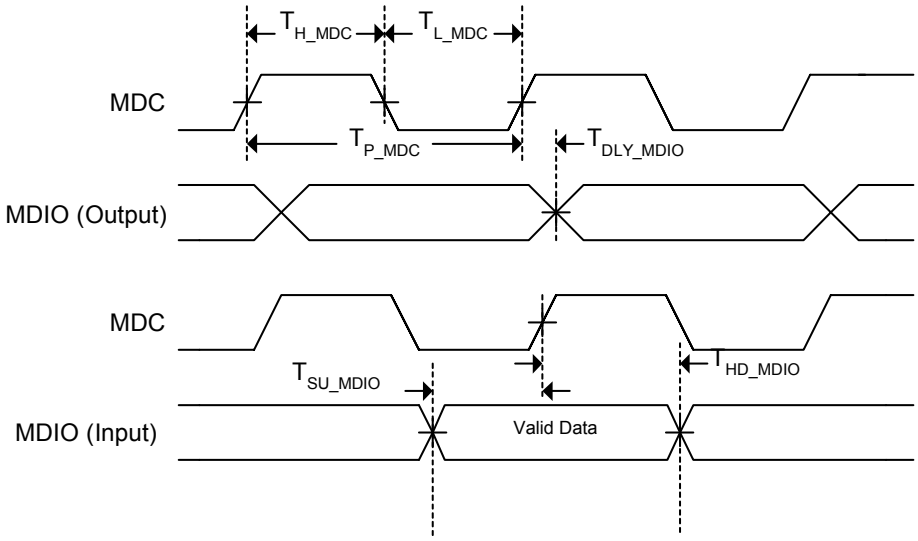


4.10 Serial Management Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DLY_MDIO}	MDC to MDIO (Output) Delay Time		0		25	ns
T_{SU_MDIO}	MDIO (Input) to MDC Setup Time		10			ns
T_{HD_MDIO}	MDIO (Input) to MDC Hold Time		10			ns
T_{P_MDC}	MDC Period		120			ns
T_{H_MDC}	MDC High		30			ns
T_{L_MDC}	MDC Low		30			ns

Figure 29: MII Serial Management Timing

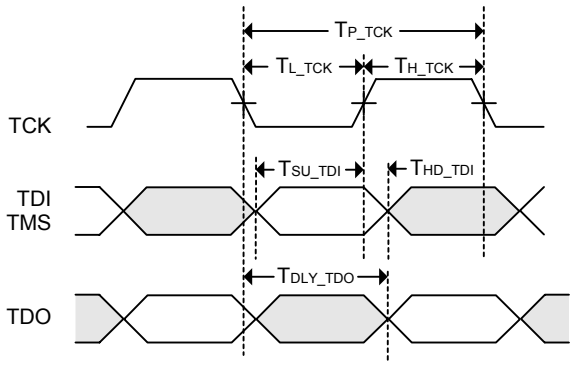


4.11 JTAG Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_TCK}	TCK Period		40			ns
T_{H_TCK}	TCK High		12			ns
T_{L_TCK}	TCK Low		12			ns
T_{SU_TDI}	TDI, TMS to TCK Setup Time		10			ns
T_{HD_TDI}	TDI, TMS to TCK Hold Time		10			ns
T_{DLY_TDO}	TCK to TDO Delay		0		20	ns

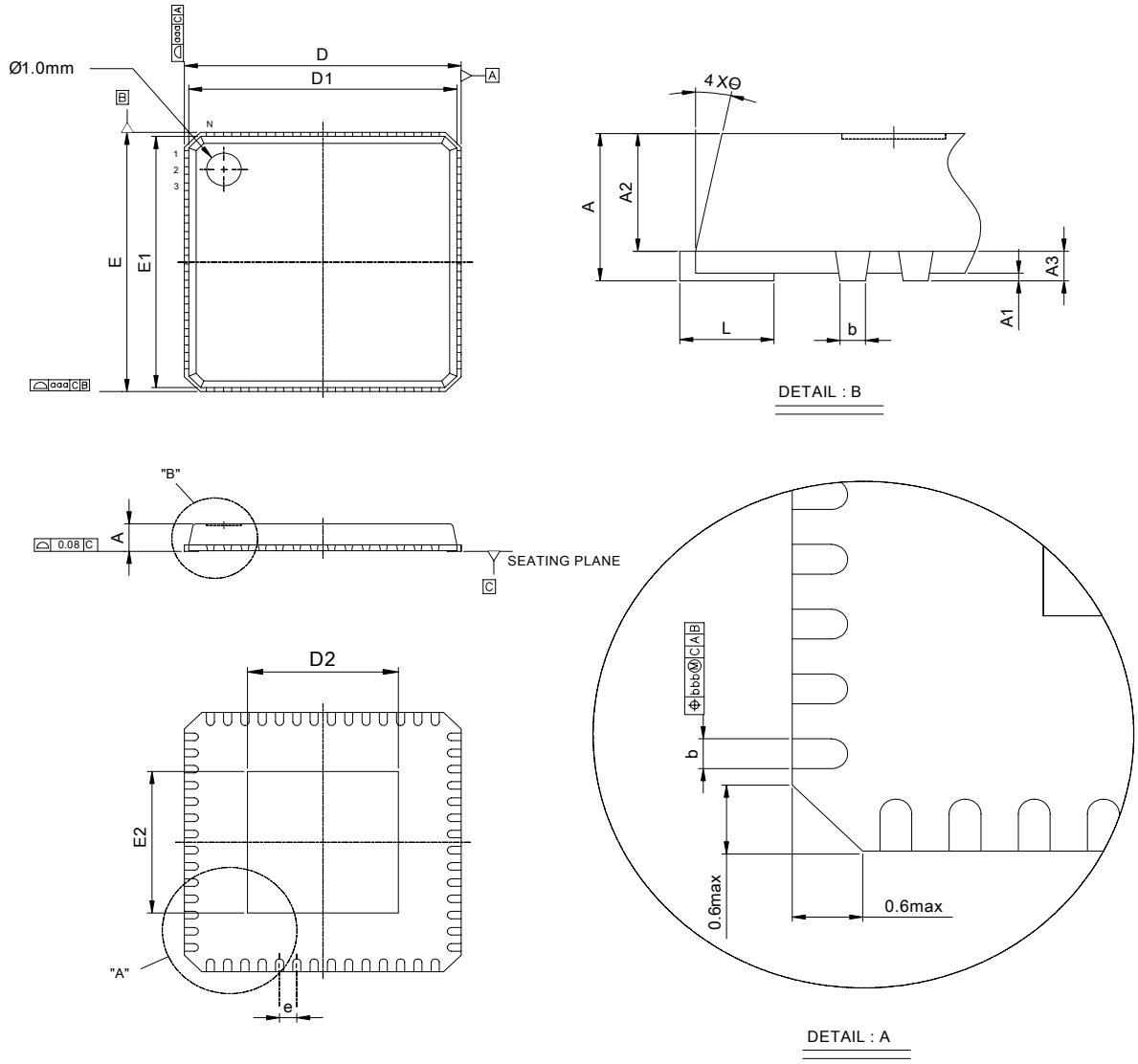
Figure 30: JTAG Timing



Section 5. Package Mechanical Dimensions

5.1 88E3015 Package Mechanical Dimensions

Figure 31: 88E3015 56-pin QFN package



(All dimensions in mm.)

Table 60: Dimensions of the 56-pin QFN Package

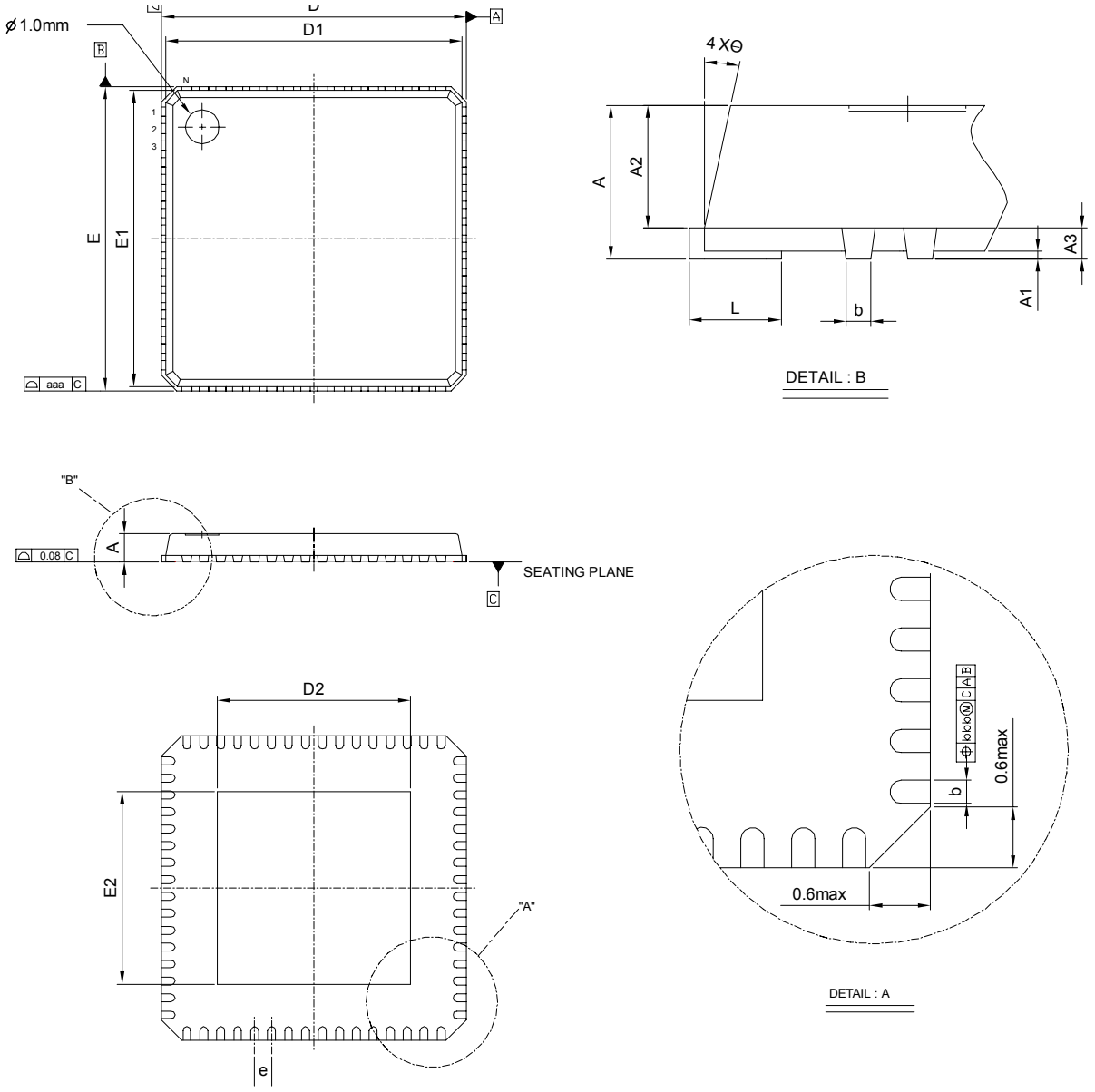
Table 61: 56-Pin QFN Mechanical Dimensions

	Dimensions in mm		
Symbol	**MIN**	**NOM**	**MAX**
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
A2	--	0.65	1.00
A3		0.20 REF	
b	0.18	0.23	0.30
D		8.00 BSC	
D1		7.75 BSC	
E		8.00 BSC	
E1		7.75 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
θ	0°	--	12°
aaa	--	--	0.15
bbb	--	--	0.10
chamfer	--	--	0.60

Die Pad Size	
Symbol	**Dimension in mm**
D_2	4.37 ± 0.20
E_2	4.37 ± 0.20

5.2 88E3018 Package Mechanical Dimensions

Figure 32: 88E3018 64-pin QFN package



(All dimensions in mm.)

Table 62: 64-Pin QFN Mechanical Dimensions

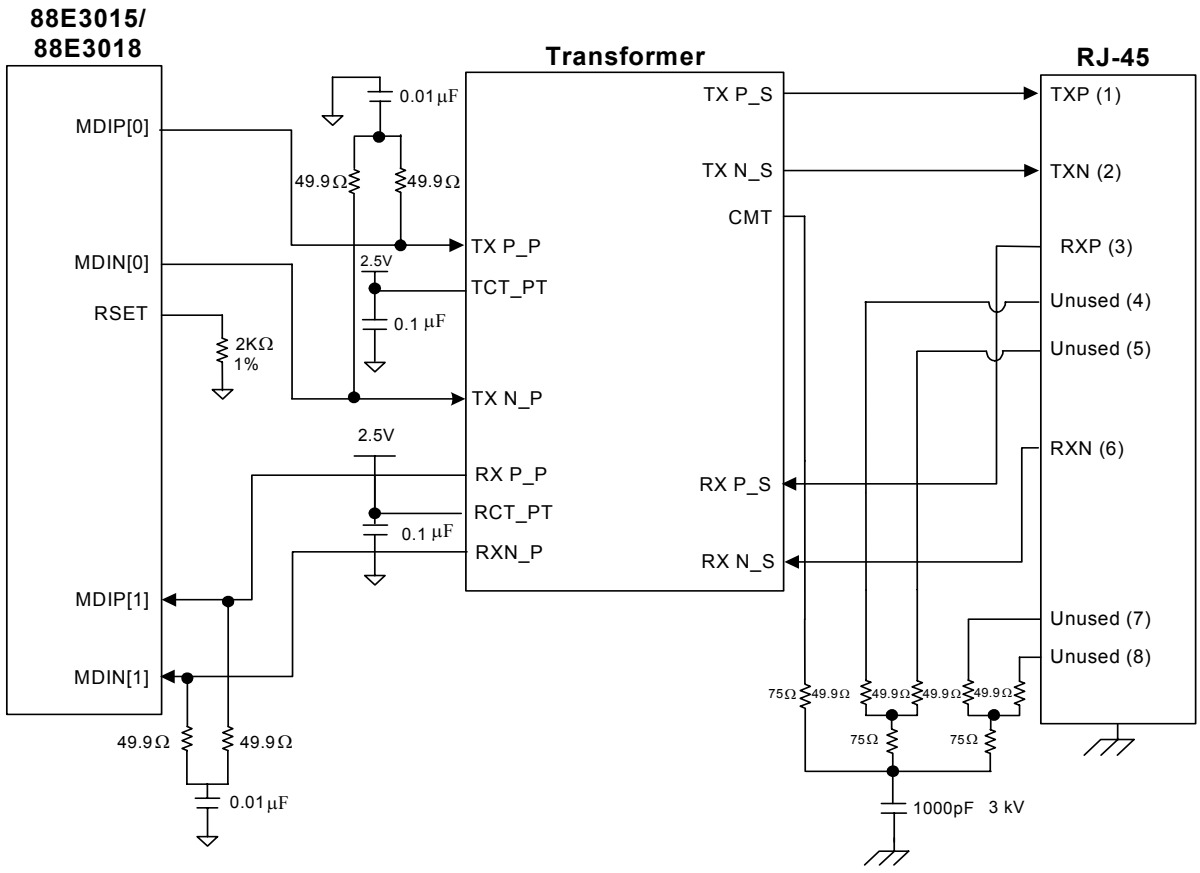
	Dimensions in mm		
Symbol	**MIN**	**NOM**	**MAX**
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
A2	--	0.65	1.00
A3		0.20 REF	
b	0.18	0.23	0.30
D		9.00 BSC	
D1		8.75 BSC	
E		9.00 BSC	
E1		8.75 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
θ	0°	--	12°
aaa	--	--	0.25
bbb	--	--	0.10
chamfer	--	--	0.60

Die Pad Size	
Symbol	**Dimension in mm**
D_2	3.78 ± 0.20
E_2	3.78 ± 0.20

Section 6. Application Examples

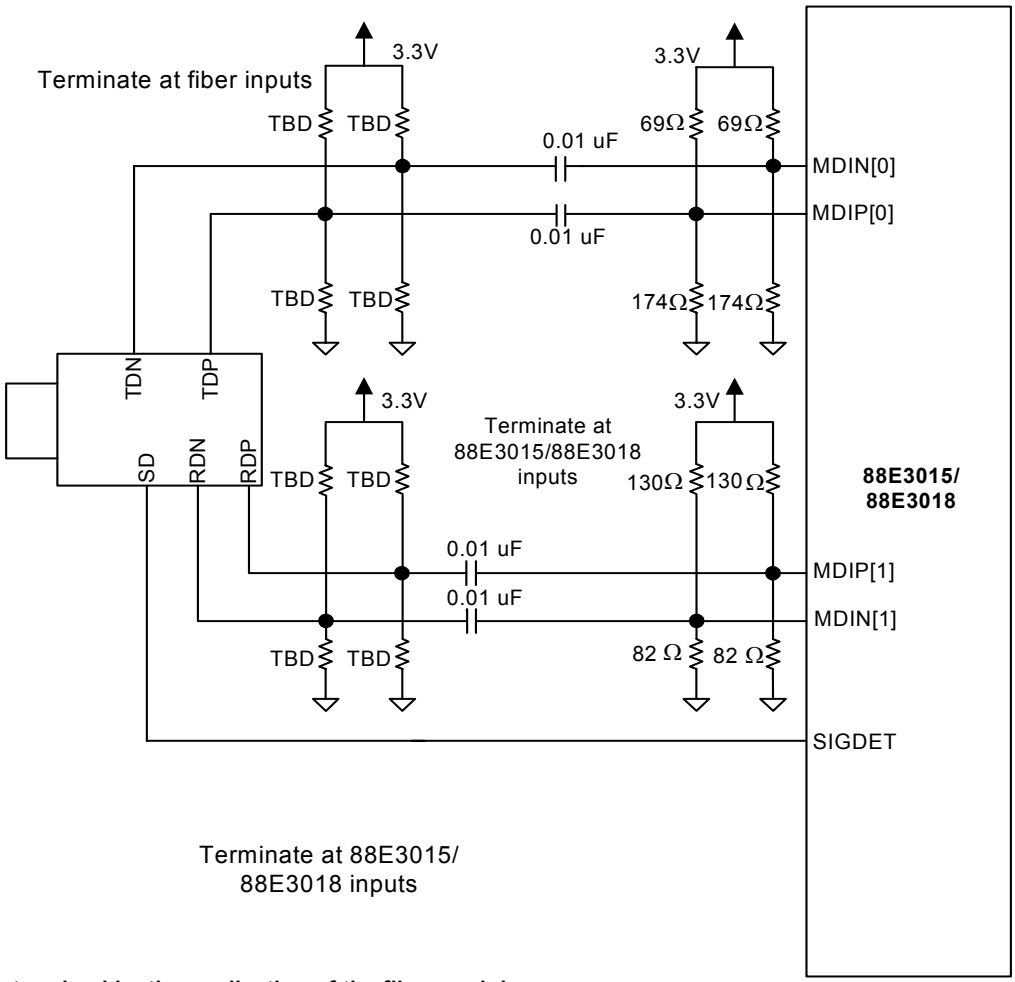
6.1 10BASE-T/100BASE-TX Circuit Application

Figure 33: 10BASE-T/100BASE-TX Circuit Application



6.2 FX Interface to 3.3V Fiber Transceiver

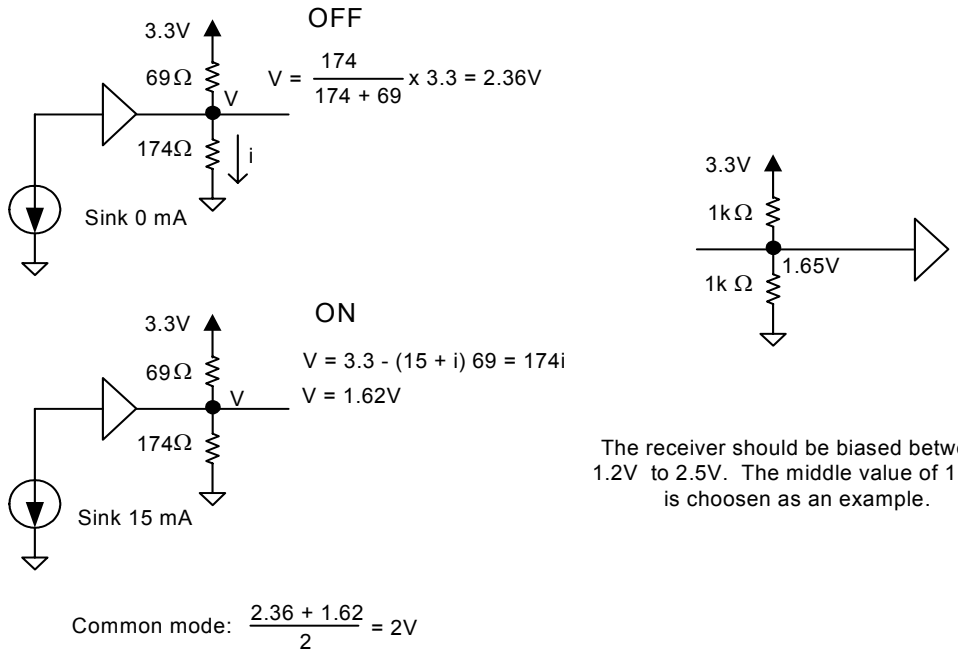
Figure 34: FX Interface to 3.3V Fiber Transceiver



TBD -- To be determined by the application of the fiber module.

6.3 Transmitter - Receiver Diagram

Figure 35: Transmitter - Receiver Diagram

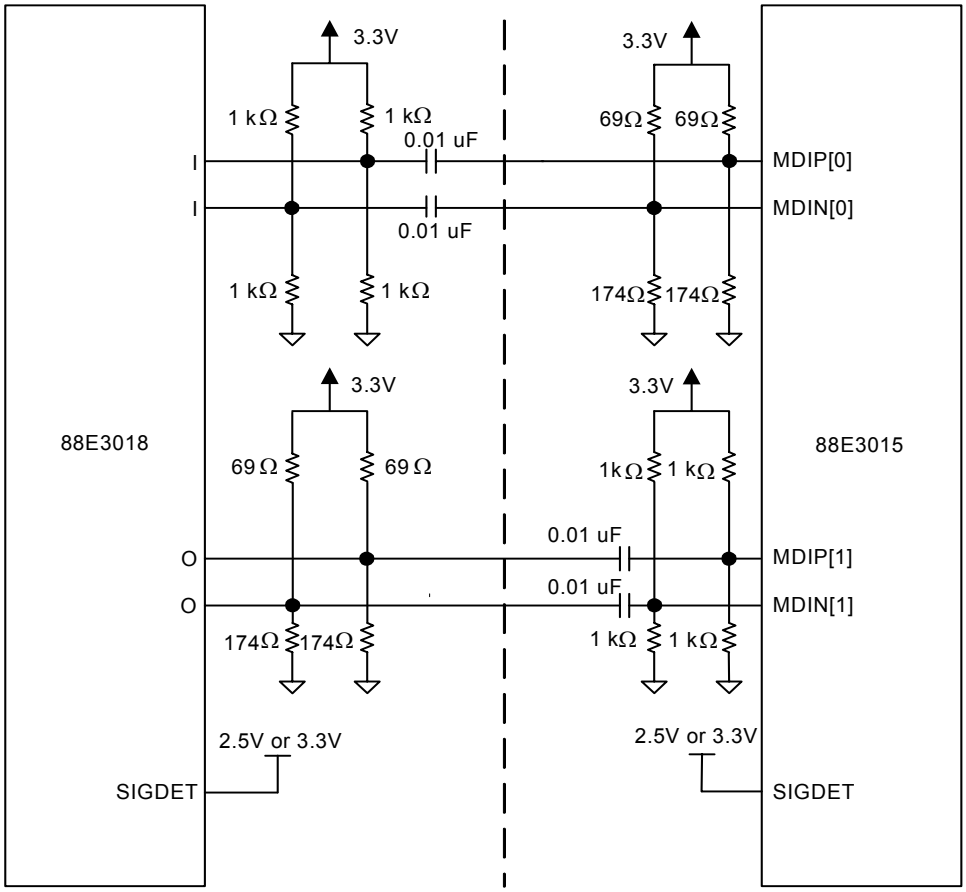


Marvell® 100BASE-FX PHY Transmitter

Marvell® 100BASE-FX PHY Receiver

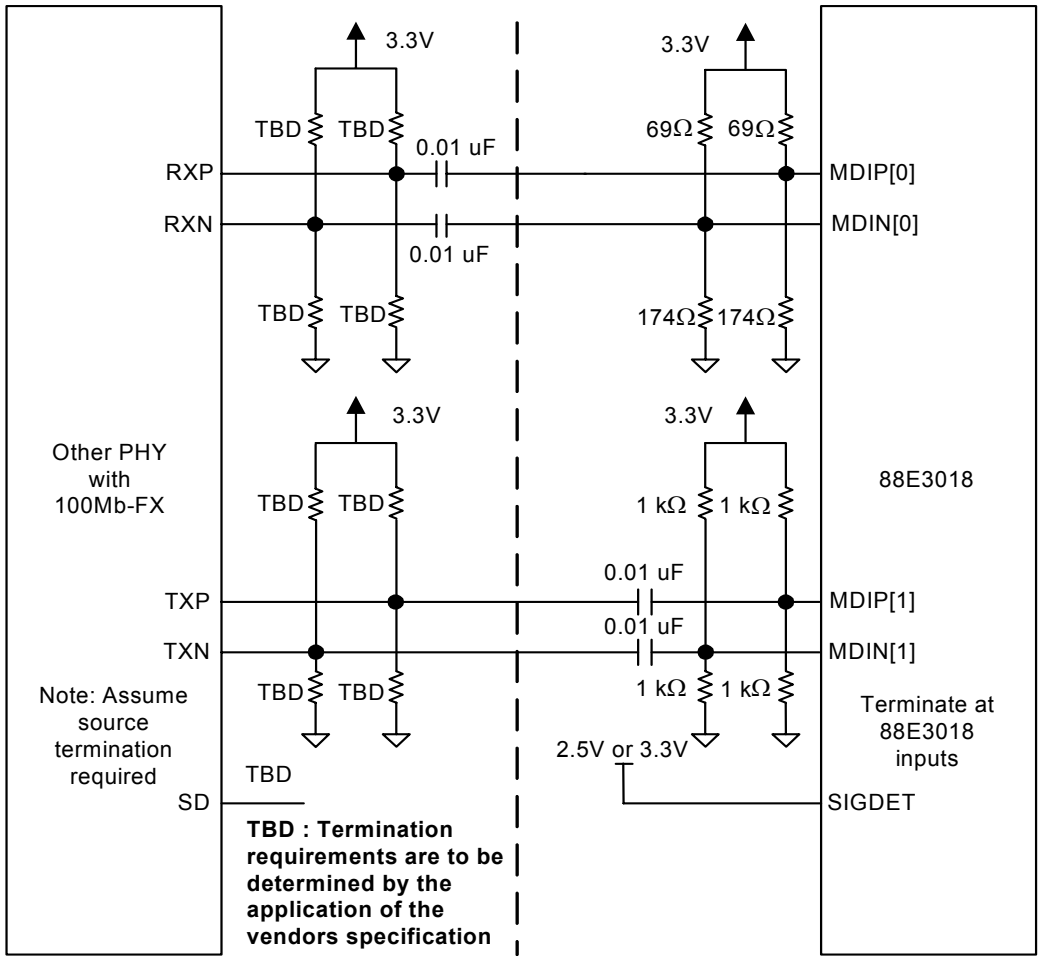
6.4 88E3018 to 88E3015 Backplane Connection - 100BASE-FX Interface

Figure 36: 88E3018 to 88E3015 Backplane Connection - 100BASE-FX Interface



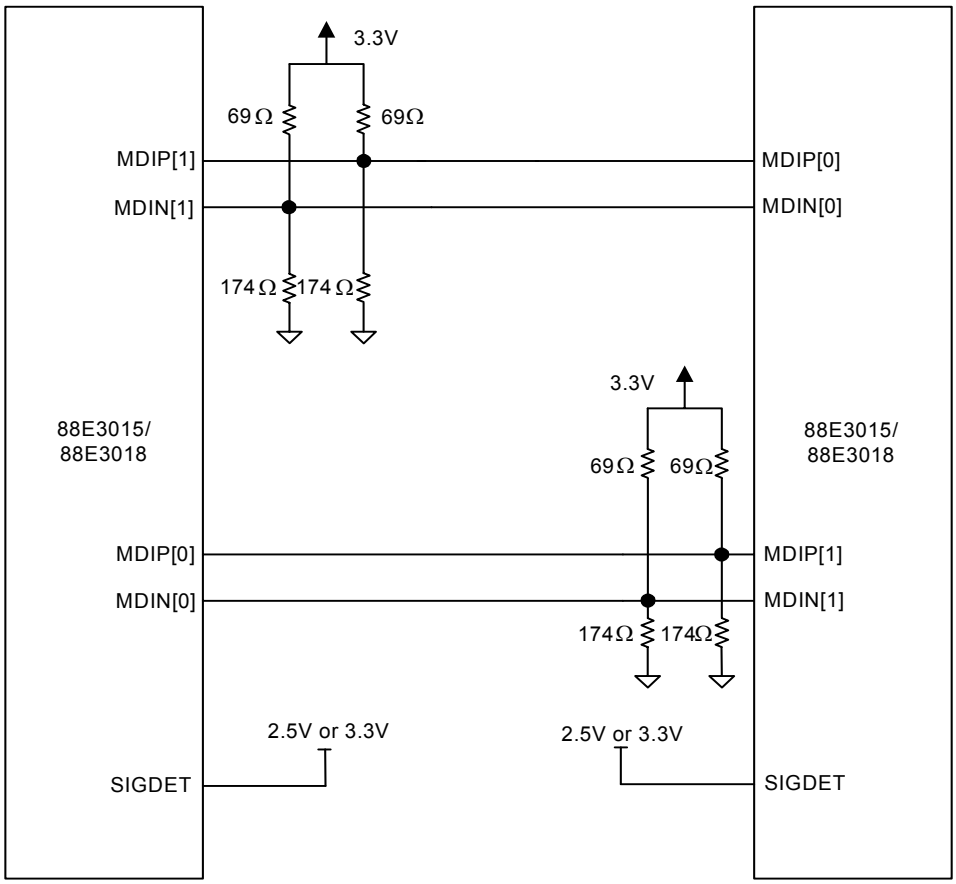
6.5 88E3018 to Another Vendor's PHY - 100BASE-FX Interface through a Backplane

Figure 37: 88E3018 to Another Vendor's PHY - 100BASE-FX Interface through a Backplane



6.6 Marvell® PHY to Marvell PHY Direct Connection

Figure 38: Marvell® PHY to Marvell PHY Direct Connection



Section 7. Order Information

7.1 Ordering Part Numbers and Package Markings

Figure 39 shows the ordering part numbering scheme for the 88E3015/88E3018 device. Contact Marvell® FAEs or sales representatives for complete ordering information.

Figure 39: Sample Part Number

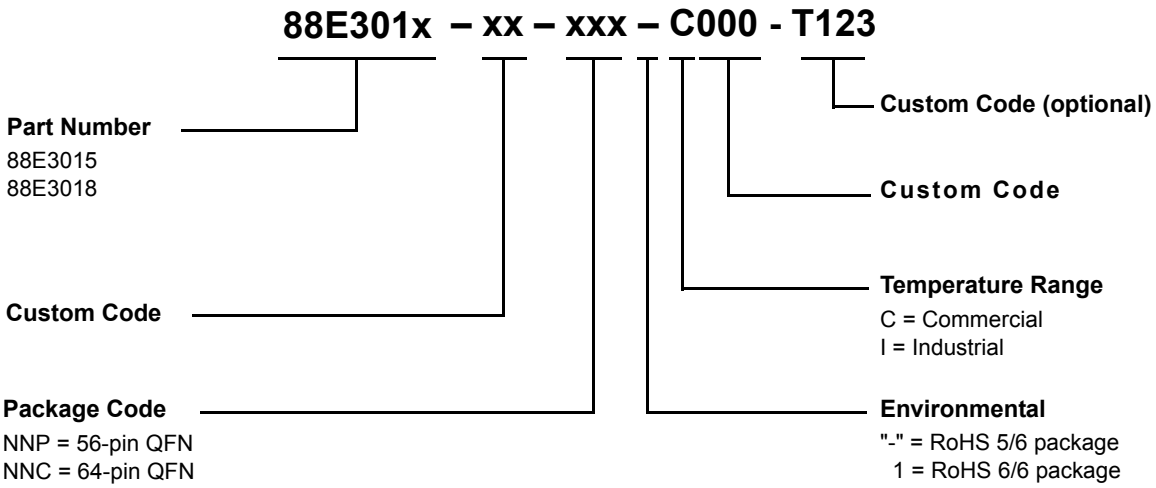


Table 63: 88E3015/88E3018 Part Order Options - RoHS 5/6 Compliant Package

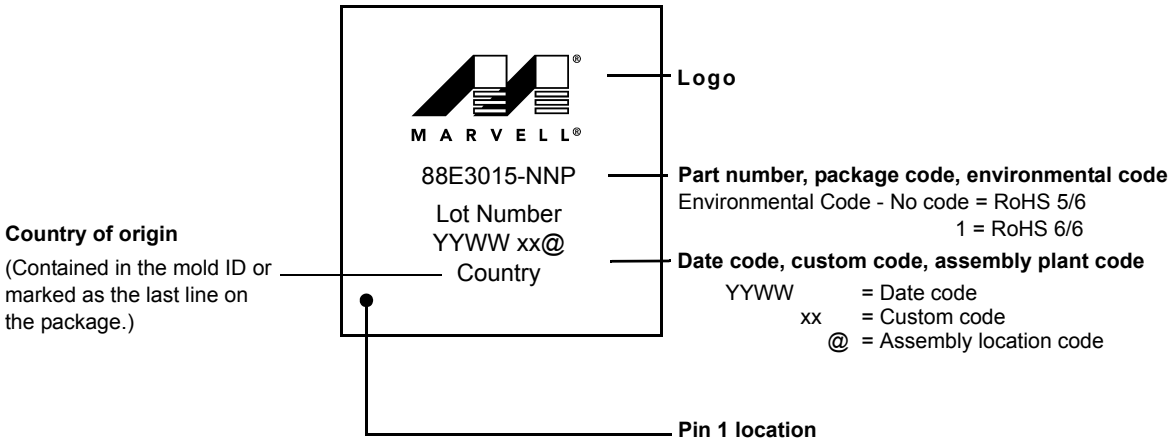
Package Type	Part Order Number
88E3015 56-pin QFN - Commercial	88E3015-XX-NNP-C000
88E3018 64-pin QFN - Commercial	88E3018-XX-NNC-C000

Table 64: 88E3015/88E3018 Part Order Options - RoHS 6/6 Compliant Package

Package Type	Part Order Number
88E3015 56-pin QFN - Commercial	88E3015-XX-NNP1C000
88E3018 64-pin QFN - Commercial	88E3018-XX-NNC1C000
88E3018 64-pin QFN - Industrial	88E3018-XX-NNC1I000

Figure 40 is an example of the package marking and pin 1 location for the 88E3015 56-pin QFN commercial RoHS 5/6 compliant package.

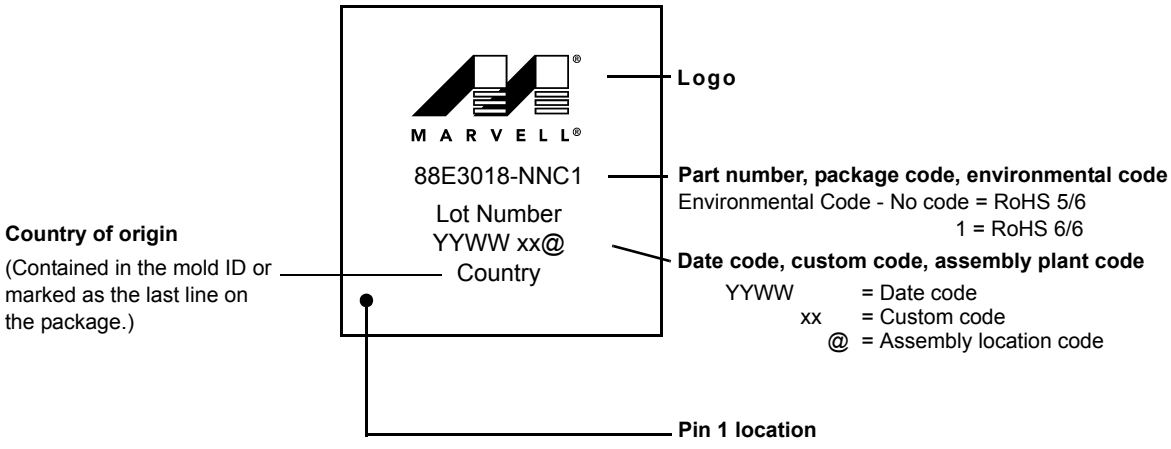
Figure 40: 88E3015 56-pin QFN Commercial RoHS 5/6 Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 41 is an example of the package marking and pin 1 location for the 88E3018 64-pin QFN commercial RoHS 6/6 compliant package.

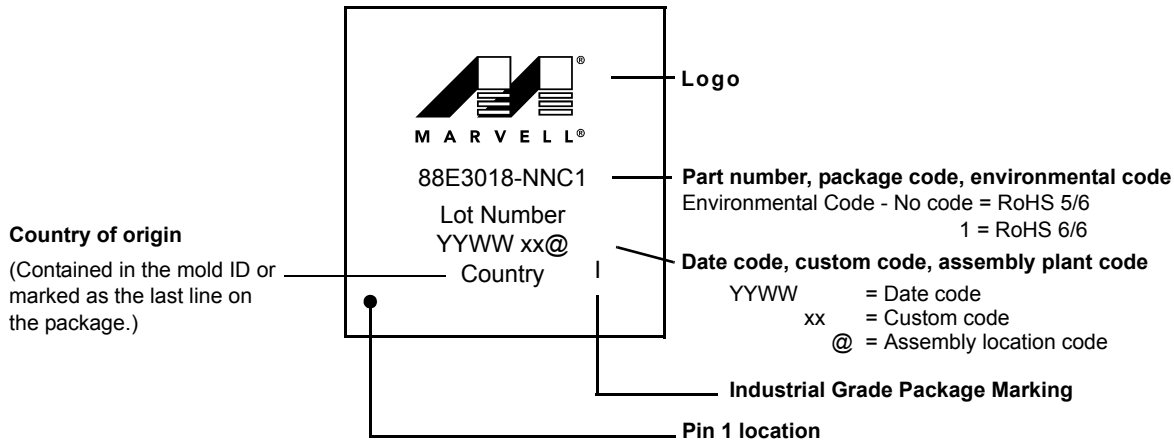
Figure 41: 88E3018 64-pin QFN Commercial RoHS 6/6 Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 42 is an example of the package marking and pin 1 location for the 88E3018 64-pin QFN industrial RoHS 6/6 compliant package.

Figure 42: 88E3018 64-pin QFN Industrial RoHS 6/6 Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

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