GigaBit Logic

10G003
10G003M

T-43-23

Dual AO/AOI Gate 4-Wide 5,4,3,2 / 2-Wide 3,2
800 ps Propagation Delay / 1.4 GHz
10G PicoLogic™ Family

FEATURES

- Dual AND/NAND gate operation
- 150 ps output rise and fall times
- Active low output enable control ($\overline{OE}$)
- ECL and 10G PicoLogic compatible I/O
- Temperature and voltage compensated design
- On-chip VBBS threshold reference voltage supply
- -55/+125°C operation (10G003M)
- Wire-OR output capability
- On chip threshold reference voltage supply (VBBS)
- Available in 40 pin C-leaded or leadless chip carrier or die form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

- Logic functions including AND/NAND
- Precision gating/strobing
- Data distribution
- Digital multiplexing
- High speed level translator (10G, ECL, TTL/CMOS)

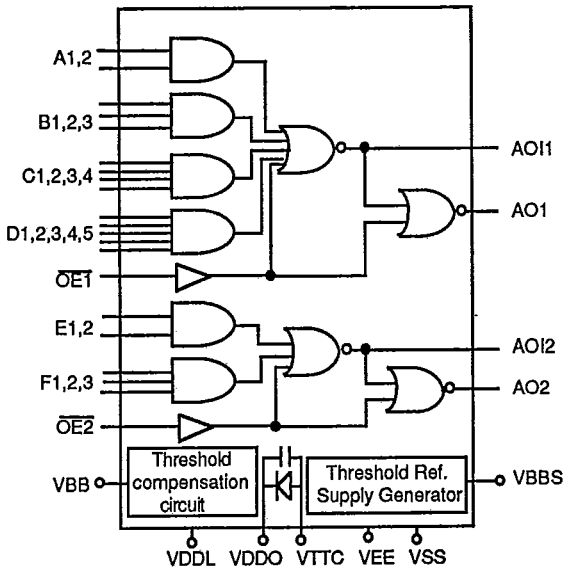
FUNCTIONAL DESCRIPTION

The 10G003 is an ultra fast dual AO/AOI gate capable of processing input signals from D.C. to 1.5 GHz. Maximum propagation delay at room temperature is 800 ps, three times shorter than equivalent ECL AO/AOI gates. The 10G003 features an output enable pin ($\overline{OE}$) to provide the capability for wired-OR bus connection.

For compatibility with other high speed logic families, the 10G003 features the Picologic™ family standard VBB input. This input allows the 10G003's threshold voltage to be controlled by the driving logic family. Therefore, mismatches in threshold level due to temperature and power supply variations can be compensated, providing high system noise immunity. An on-chip threshold voltage output (pin VBBS) is also provided. VBBS must be strapped to the VBB input when PicoLogic™ is used to drive the 10G003.

The 10G003 is a member of GigaBit's PicoLogic™ family of GaAs digital integrated circuits, and is fabricated using GigaBit's high volume GaAs MESFET process technology.

LOGIC DIAGRAM



10G003/10G003M ORDERING INFORMATION

PACKAGE TYPE	10G003(0°C/85°C) 1.4 GHz	10G003M (-55/125°C) 1.2 GHz
C-Leaded CC	10G003 - 2 C	10G003M - 2C
Leadless CC	10G003 - 2 L	10G003M - 2L
Die	10G003 - 2 X	10G003M - 2X

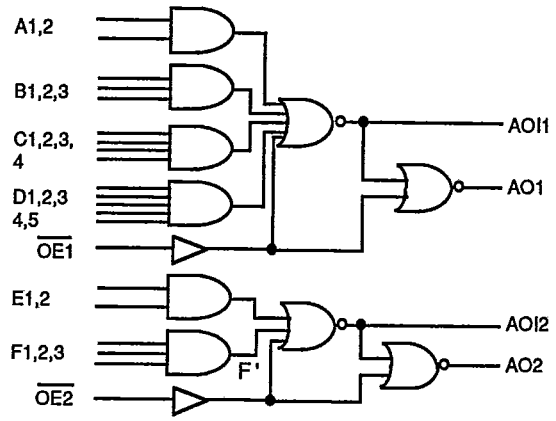
GigaBit Logic

10G003
10G003M

T-43-23

1

10G003 Operation



F' = Output of the 3-input AND gate

TRUTH TABLE (2-Wide 3,2 AO/AOI)					
$\overline{OE}$	E1	E2	F'	AO2	AOI2
H	X	X	X	O	O
L	X	X	1	1	O
L	X	X	O	E1•E2	$\overline{E1•E2}$

Boolean Equations:

$AOI1 = [\overline{A1•A2} \cdot \overline{B1•B2•B3} \cdot \overline{C1•C2•C3•C4} \cdot \overline{D1•D2•D3•D4•D5}] \cdot \overline{OE1}$

$AO1 = [A1•A2 + B1•B2•B3 + C1•C2•C3•C4 + D1•D2•D3•D4•D5] \cdot \overline{OE1}$

$AOI2 = [\overline{E1•E2} \cdot \overline{F1•F2•F3}] \cdot \overline{OE2}$

$AO2 = [E1•E2 + F1•F2•F3] \cdot \overline{OE2}$

The operation of the 2-Wide 3,2 portion of the dual AO/AOI gate is described in the truth table above. All outputs can be forced low by bringing OE input high. If $\overline{OE}$ is low and F' is 1 (i.e. F1=F2=F3=1), AO2 is 1 and AOI2 is 0, independently of E1 and E2. If $\overline{OE}$ is low and F' is 0 (i.e. F1=0 or F2=0 or F3=0), AO2 is the AND function for E1 and E2, and AOI2 is the NAND fuction for E1 AND E2.

Pin Descriptions

An....Fn	Data Inputs
$\overline{OE1}$	Output enable for 5 - 4 - 3 - 2 AO/AOI
$\overline{OE2}$	Output enable for 3 - 2 AO/AOI
AO1	5 - 4 - 3 - 2 AND - OR Output
AOI1	5 - 4 - 3 - 2 ANR - OR - INVERT Output
AO2	3 - 2 AND - OR Output
AOI2	3 - 2 AND - OR - INVERT Output
VDDO	Output driver ground pin (0 V)
VDDL	Internal logic ground connection (0V)
VSS	-3.4V power supply
VEE	-5.2V power supply
VTTC	The AC return pin for the package internal VDDO decoupling capacitor. VTTC is typically tied to VTT (nominally -2.0V)
VDCH	Output driver high level clamp voltage. When not used, VDCH should be connected to VDDO. When driving ECL, VDCH may be used to limit VOH. Consult Application Note 4 for detail.
VBB	Reference input to the 10G003's input threshold tracking circuit. Connect to the VBB supplied from ECL when driving the 10G003 from ECL. Connect to the VBBS pin when the 10G003 is driven from PicoLogic. This pin cannot be left unconnected.
VBBS	PicoLogic threshold reference output voltage. Connect to VBB when driving from PicoLogic.

GigaBit Logic

10G003
10G003M

T-43-23

DC CHARACTERISTICS

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

Symbol	Parameter	10G003 (0 to 85°C)			10G003M (-55 to +125°C)			Units
		Min	Typ	Max	Min	Typ	Max	
VIH	Input voltage high				- 0.8			V
VIL	Input voltage low						- 1.8	V
I IN1	Input current ($\overline{OE1}$,$\overline{OE2}$)			1000			1000	µA
IIN2	Input current (all others)		150			150	750	µA
VBBS	Threshold reference voltage		-1.2			-1.2		V
ISS	Vss power supply current		170	270		170	300	mA
IEE	Vee power supply current		25	40		25	45	mA
PD	Power dissipation		700	1130		700	1250	mW

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Notes 1, 2)

VSS= -3.5V to -3.3V, VEE= -5.5V to -5.1V, VDDL=VDDO=Gnd., unless otherwise indicated

SYMBOL	PARAMETER	10G003-2							10G003M-2							UNITS
		Tc= 0°C		Tc= 25°C			Tc= 85°C		Tc= -55°C		Tc= 25°C			Tc= 125°C		
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
1/(2T)	Operating Frequency	1.4		1.4	1.5		1.4		1.4		1.4	1.5		1.2		GHz
Tpd1	Input to AOI Output propagation delay	375	725	425	550	725	450	800	450	775	425	550	725	475	850	ps
Tpd2	Input to AO Output propagation delay	450	800	450	650	800	475	850	475	850	450	650	800	500	900	ps
Toe1	$\overline{OE}$ to Output High to low delay	350	600	350	475	600	375	675	375	650	350	475	600	425	725	ps
Toe2	$\overline{OE}$ to Output Low to High delay	350	600	350	475	600	375	675	375	650	350	475	600	425	725	ps
T r,f	Output rise and fall time		200		150	200		225		225		150	200		245	ps

NOTES:

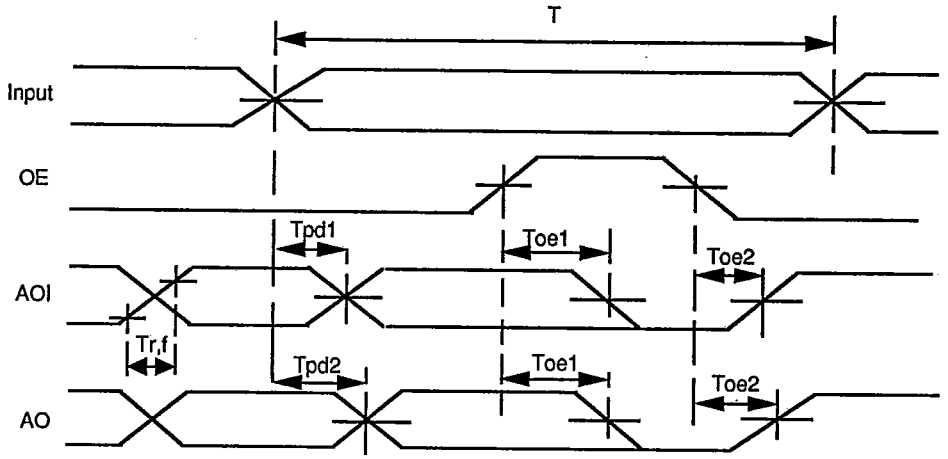
1. Test conditions (unless otherwise noted): VBB = -1.2V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VDCH = VDDO, VIH = -0.7V, VIL = -1.7V, VOH ≥ -0.7V, VOL ≤ -1.7V. Input signal rise and fall times <150ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

GigaBit Logic

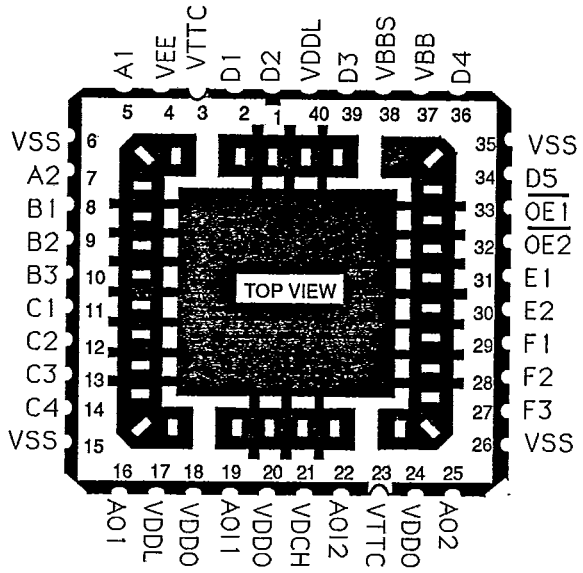
10G003
10G003M

1

SWITCHING WAVEFORMS



PIN FUNCTIONS - TYPE "L" AND "C" PACKAGES



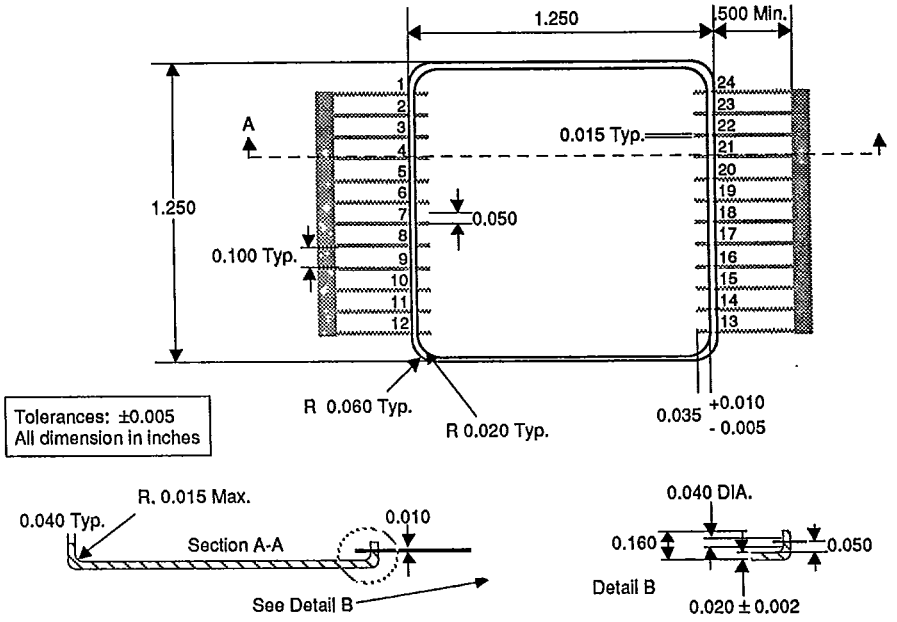
GigaBit Logic

24 PIN HYBRID 18 PIN PACKAGE

T-90-20

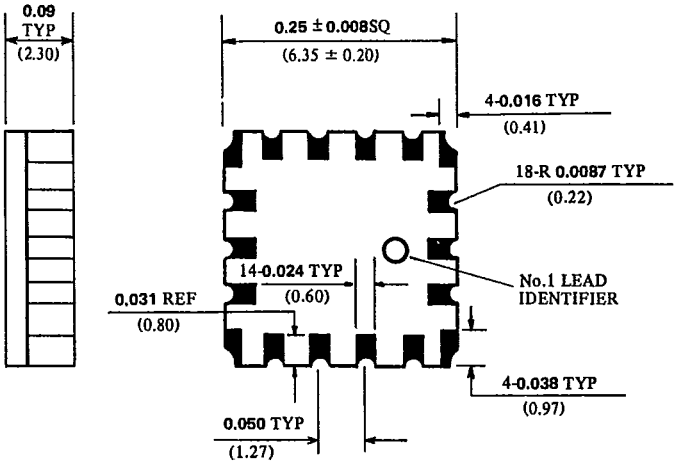
24 PIN HYBRID PACKAGE

Type H



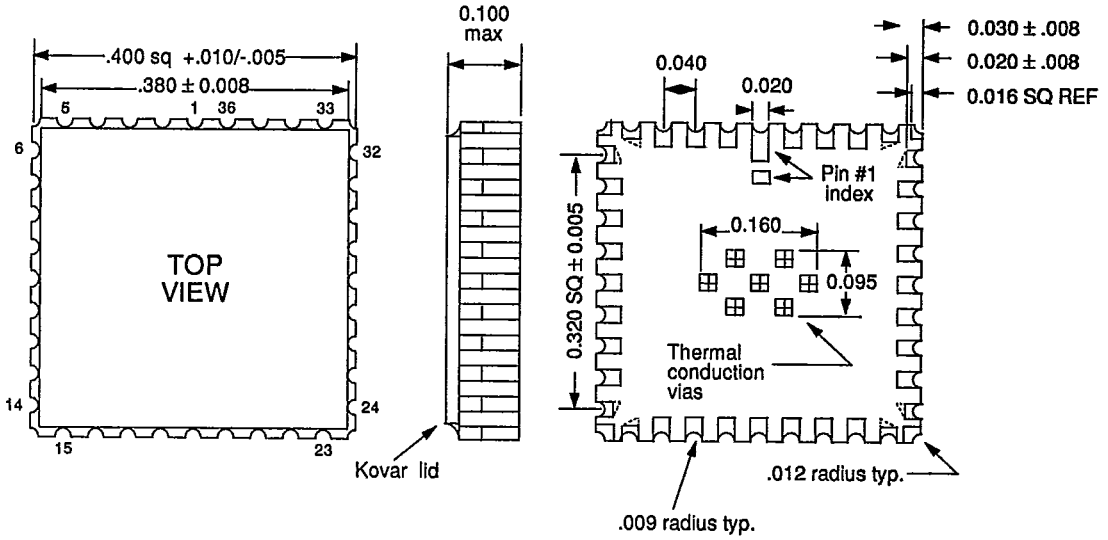
18 PIN LEADLESS CHIP CARRIER

TYPE L1



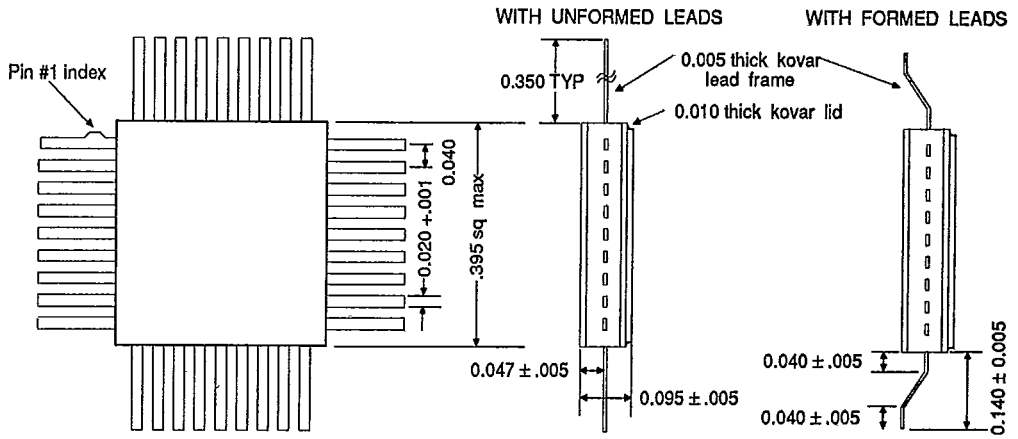
All dimensions shown in **inches** and (millimeters)

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Pin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



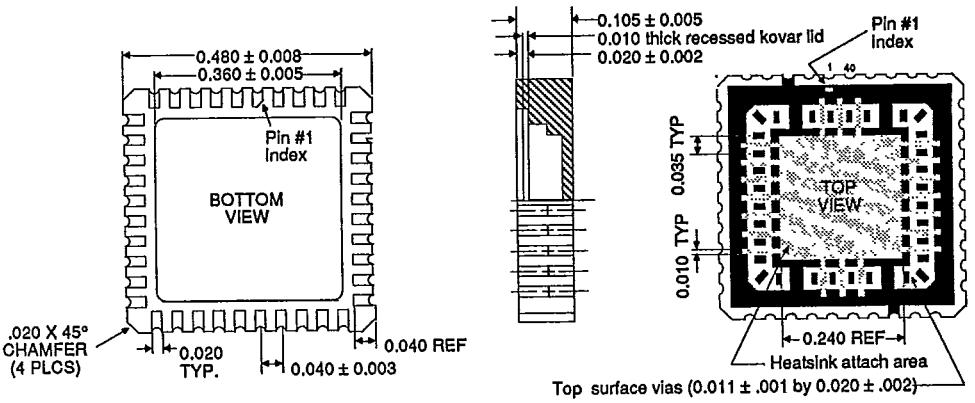
11

T-90-20

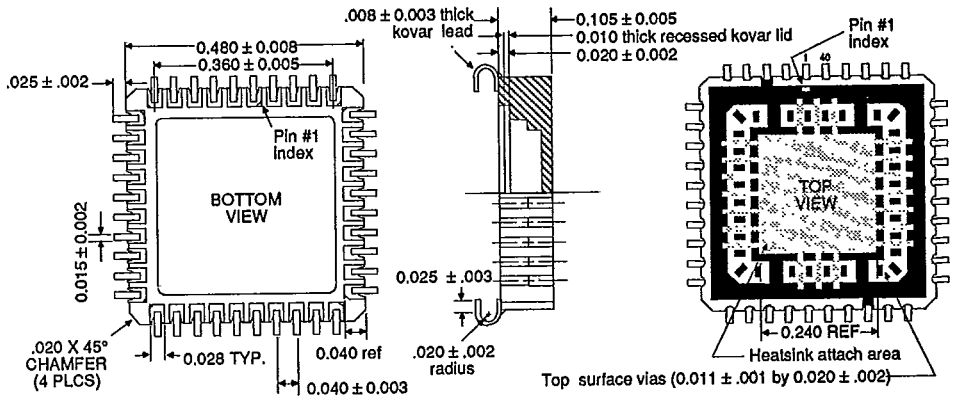
GigaBit Logic

40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L



40 PIN LEADED CHIP CARRIER
TYPE C

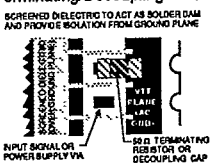


NOTES:

(1) Footprint is JEDEC standard outline.
(2) Top surface vias (for terminating resistors and decoupling capacitors) are not available on pins 3,4,17, 18, 23,24,37 and 38.
(3) Top surface metal (not including vias) and pins 3 and 23 are fixed at VTT potential.
(4) Recommended top surface chip resistors are0.040 long by 0.020 wide by 0.010 thick typ, 100 mw min. nominal power rating (Mini-Systems MSR-21 or equivalent.)
(5) Recommended top surface chip capacitors are 0.040 long by 0.030 wide by 0.020 thick typ, 25V VDCW, 1000 pf, min. (Johanson R09 case or equivalent).
(6) Recommended heatsinks are GBL P/Ns 90GHS-40-A and 90GHS-40-B.
(7) Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789-4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width.

TOP SURFACE LEGEND:
Metalized Ceramic.....
Screened Dielectric.....
Bare Ceramic.....

Top Surface Terminating/Decoupling Detail

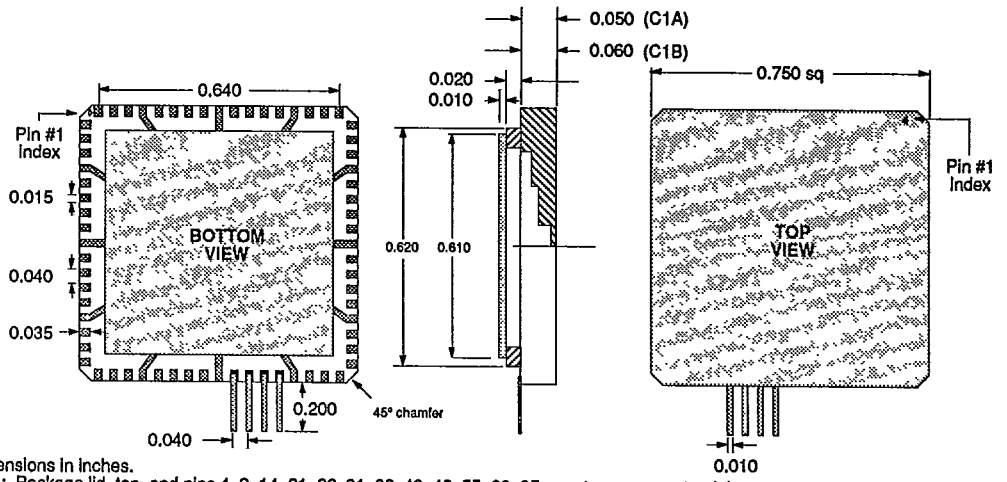


GigaBit Logic

68 & 132 PIN PACKAGES

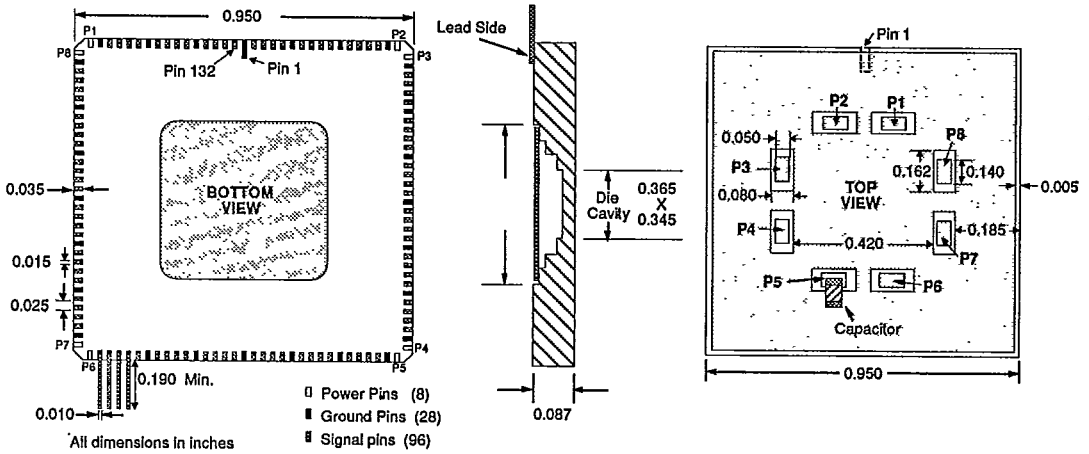
T-90-20

68 PIN LEADED CHIP CARRIER
TYPE C1



(1) All dimensions in inches.
(2) a. C1A: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
b. C1B: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).

132 PIN LEADED CHIP CARRIER
TYPE C3



11