PRODUCT SPECIFICATION T-49-19-07

Z86E21

CMOS Z8® OTP MICROCONTROLLER

FEATURES

- 8-bit CMOS microcontroller, 40- or 44-pin package
- 4.5 to 5.5 Voltage operating range
- Low Power consumption - 275 mW (max)
- Fast instruction pointer - 1.0 microseconds @ 12 MHz
- Two standby modes - STOP and HALT
- 32 input/output lines
- Full-Duplex UART
- All digital inputs are TTL levels
- Auto latches
- High voltage protection on high voltage inputs
- RAM and EPROM protect
- 8 Kbytes of EPROM
- 256 bytes of RAM (236 for general purpose)
- Two programmable 8-bit Counter/Timers each with 6-bit programmable prescaler.
- Six vectored, priority interrupts from eight different sources.
- Clock speeds 12 and 16 MHz
- On-chip oscillator that accepts a crystal, ceramic resonator, LC or external clock drive.

GENERAL DESCRIPTION

The Z86E21 microcontroller (MCU) introduces the next level of sophistication to single-chip architecture. The Z86E21 is a member of the Z8 single-chip microcontroller family with 8 Kbytes of EPROM and 236 bytes of general purpose RAM.

The Z86E21 is a pin compatible, One-Time-Programmable (OTP) version of the Z86C21. The Z86E21 contains 8 Kbytes of EPROM memory in place of the 8 Kbyte of ROM on the Z86C21.

The MCU is housed in a 40-pin DIP, 44-pin Leaded Chip-Carrier, or a 44-pin Quad Flat Pack, and is manufactured in CMOS technology. The ROMless pin option is available on the 44-pin versions only. The MCU can address both external memory and preprogrammed ROM which enables this Z8 microcomputer to be used in high volume applications or where code flexibility is required.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86E21 architecture is based on Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

The device applications demand powerful I/O capabilities. The Z86E21 fulfills this with 32-pin dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

GENERAL DESCRIPTION (Continued)

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory and 236 General-Purpose registers.

To unburden the program from coping with real-time problems such as counting/timing and serial data communication, the Z86E21 offers two on-chip counter/timers with a large number of user selectable modes, and an asynchronous receiver/transmitter (UART) (Figure 1).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only); /N//S (NORMAL and SYSTEM are both active Low).

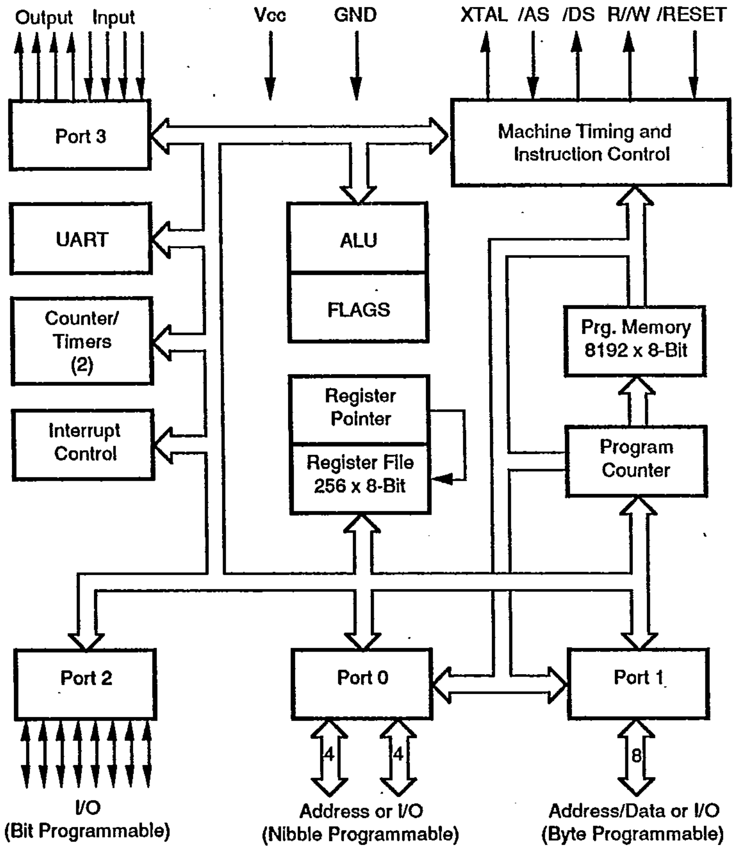


Figure 1. Functional Block Diagram

PIN DESCRIPTION
Standard Mode

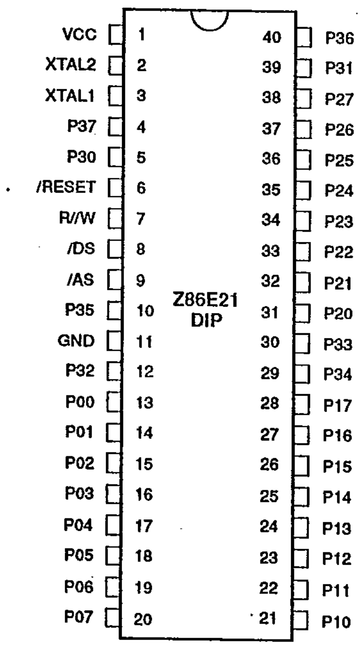


Figure 2. 40-Pin Dual-In-Line Pin Assignments

Table 1. 40-Pin Dual-In-Line Pin Identification (Standard Mode)

Pin #	Symbol	Function	Direction
1	V_{cc}	Power Supply	Input
2	XTAL1	Crystal, Oscillator Clock	Output
3	XTAL2	Crystal, Oscillator Clock	Input
4	P37	Port 3 pin 7	Output
5	P30	Port 3 pin 0	Input
6	/RESET	Reset	Input
7	R/W	Read/Write	Output
8	/DS	Data Strobe	Output
9	/AS	Address Strobe	Output
10	P35	Port 3 pin 5	Output
11	GND	Ground, GND	Input
12	P32	Port 3 pin 2	Input
13-20	P00-P07	Port 0 pin 0,1,2,3,4,5,6,7	In/Output
21-28	P10-P17	Port 1 pin 0,1,2,3,4,5,6,7	In/Output
29	P34	Port 3 pin 4	Output
30	P33	Port 3 pin 3	Input
31-38	P20-P27	Port 2 pin 0,1,2,3,4,5,6,7	In/Output
39	P31	Port 3 pin 1	Input
40	P36	Port 3 pin 6	Output

PIN DESCRIPTION (Continued)
Standard Mode

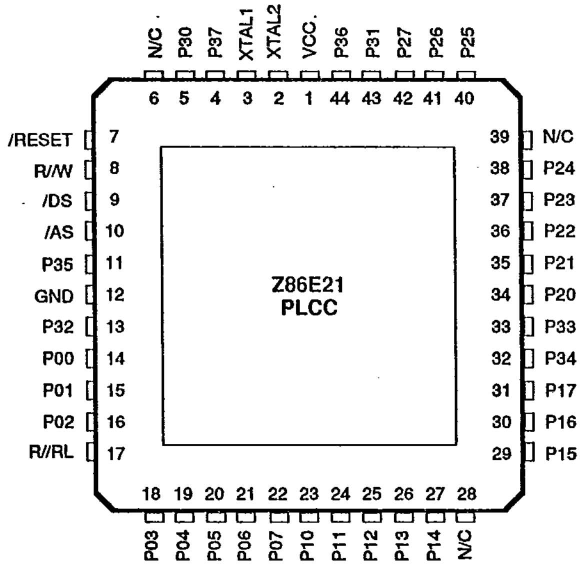


Figure 3. 44-Pin Leaded Chip Carrier Pin Assignments

Table 2. 44-Pin Leaded Chip Carrier Pin Identification (Standard Mode)

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input	14-16	P00-P02	Port 0 pin 0,1,2	In/Output
2	XTAL1	Crystal, Oscillator Clock	Output	17	R//RL	ROM/ROMless control	Input
3	XTAL2	Crystal, Oscillator Clock	Input	18-22	P03-P07	Port 0 pin 3,4,5,6,7	In/Output
4	P37	Port 3 pin 7	Output	23-27	P10-P14	Port 1 pin 0,1,2,3,4	In/Output
5	P30	Port 3 pin 0	Input	28	N/C	Not Connected	Input
6	N/C	Not Connected	Input	29-31	P15-P17	Port 1 pin 5,6,7	In/Output
7	/RESET	Reset	Input	32	P34	Port 3 pin 4	Output
8	R//W	Read/Write	Output	33	P33	Port 3 pin 3	Input
9	/DS	Data Strobe	Output	34-38	P20-P24	Port 2 pin 0,1,2,3,4	In/Output
10	/AS	Address Strobe	Output	39	N/C	Not Connected	Input
11	P35	Port 3 pin 5	Output	40-42	P25-P27	Port 2 pin 5,6,7	In/Output
12	GND	Ground, GND	Input	43	P31	Port 3 pin 1	Input
13	P32	Port 3 pin 2	Input	44	P36	Port 3 pin 6	Output

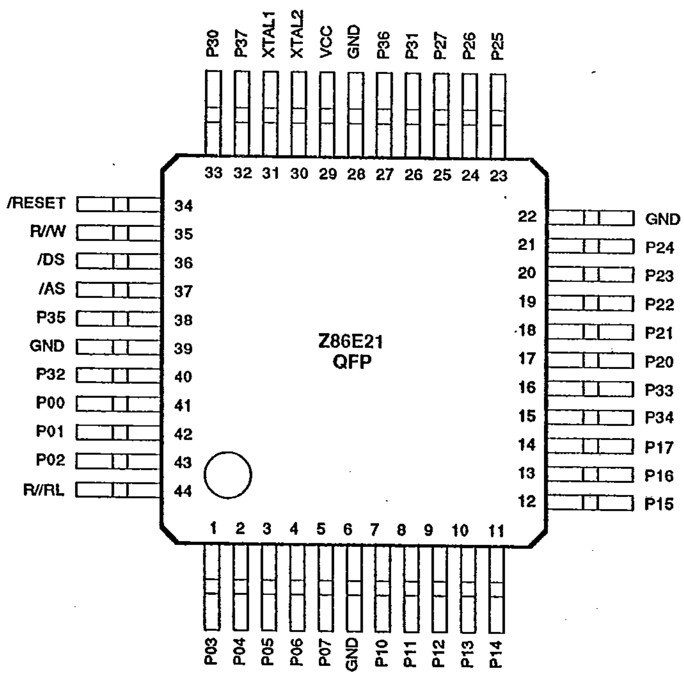


Figure 4. 44-Pin Quad Flat Pack Pin Assignments

Table 3. 44-Pin Quad Flat Pack Pin Identification (Standard Mode)

Pin #	Symbol	Function	Direction
1-5	P03-P07	Port 0 pin 3,4,5,6,7	In/Output
6	GND	Ground, GND	Input
7-14	P10-P17	Port 1 pin 0,1,2,3,4,5,6,7	In/Output
15	P34	Port 3 pin 4	Output
16	P33	Port 3 pin 3	Input
17-21	P20-P24	Port 2 pin 0,1,2,3,4	In/Output
22	GND	Ground, GND	Input
23-25	P25-P27	Port 2 pin 5,6,7	In/Output
26	P31	Port 3 pin 1	Input
27	P36	Port 3 pin 6	Output
28	GND	Ground, GND	Input
29	V_{cc}	Power Supply	Input
30	XTAL1	Crystal, Oscillator Clock	Output
31	XTAL2	Crystal, Oscillator Clock	Input
32	P37	Port 3 pin 7	Output
33	P30	Port 3 pin 0	Input
34	/RESET	Reset	Input
35	R//W	Read/Write	Output
36	/DS	Data Strobe	Output
37	/AS	Address Strobe	Output
38	P35	Port 3 pin 5	Output
39	GND	Ground, GND	Input
40	P32	Port 3 pin 2	Input
41-43	P00-P02	Port 0 pin 0,1,2	In/Output
44	R//RL	ROM/ROMless control	Input

PIN DESCRIPTION (Continued)
EPROM Mode

T-49-19-07

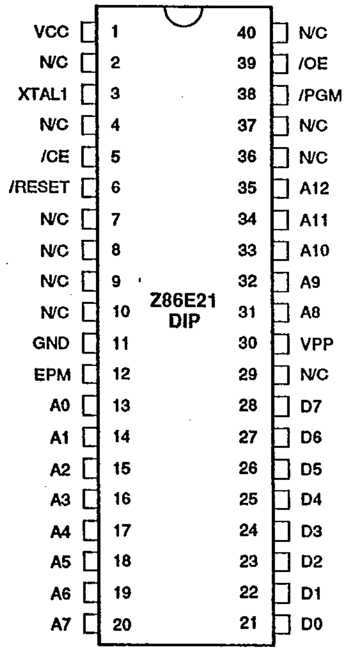


Figure 5. 40-Pin Dual-In-Line Pin Assignments

Table 4. 40-Pin Dual-In-Line Pin Identification (EPROM Mode)

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input	13-20	A0-A7	Address 0,1,2,3,4,5,6,7	Input
2	N/C	Not Connected	Input	21-28	D0-D7	Data 0,1,2,3,4,5,6,7	In/Output
3	XTAL1	Crystal, Oscillator Clock	Input	29	N/C	Not Connected	Input
4	N/C	Not Connected	Input	30	V_{PP}	Prog Voltage	Input
5	/CE	Chip Enable	Input	31-35	A8-A12	Address 8,9,10,11,12	Input
6	/RESET	Reset	Input	36-37	N/C	Not Connected	Input
7-10	N/C	Not Connected	Input	38	/PGM	Prog Mode	Input
11	GND	Ground, GND	Input	39	/OE	Output Enable	Input
12	EPM	EPROM Prog Mode	Input	40	N/C	Not Connected	Input

T-49-19-07

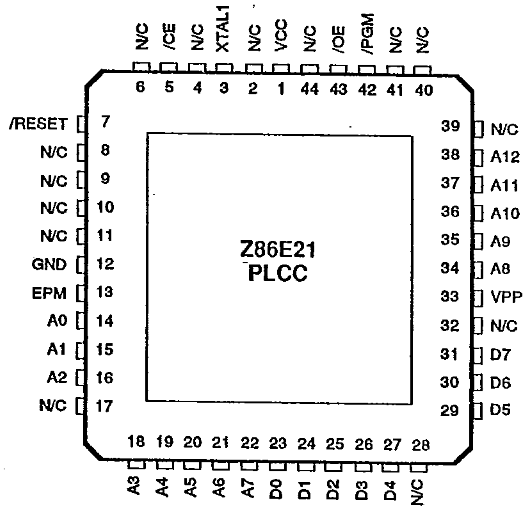


Figure 6. 44-Pin Leaded Chip Carrier Pin Assignments

Table 5. 44-Pin Leaded Chip Carrier Pin Identification (EPROM Mode)

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	N/C	Not Connected	Input
3	XTAL1	Crystal, Oscillator Clock	Input
4	N/C	Not Connected	Input
5	/CE	Chip Enable	Input
6	N/C	Not Connected	Input
7	/RESET	Reset	Input
8-11	N/C	Not Connected	Input
12	GND	Ground, GND	Input
13	EPM	EPROM Prog Mode	Input
14-16	A0-A2	Address 0,1,2	Input
17	N/C	Not Connected	Input

Pin #	Symbol	Function	Direction
18-22	A3-A7	Address 3,4,5,6,7	Input
23-27	D0-D4	Data 0,1,2,3,4	In/Output
28	N/C	Not Connected	Input
29-31	D5-D7	Data 5,6,7	In/Output
32	N/C	Not Connected	Input
33	V_{PP}	Prog Voltage	Input
34-38	A8-A12	Address 8,9,10,11,12	Input
39-41	N/C	Not Connected	Input
42	/PGM	Prog Mode	Input
43	/OE	Output Enable	Input
44	N/C	Not Connected	Input

PIN DESCRIPTION (Continued)
EPROM Mode

T-49-19-07

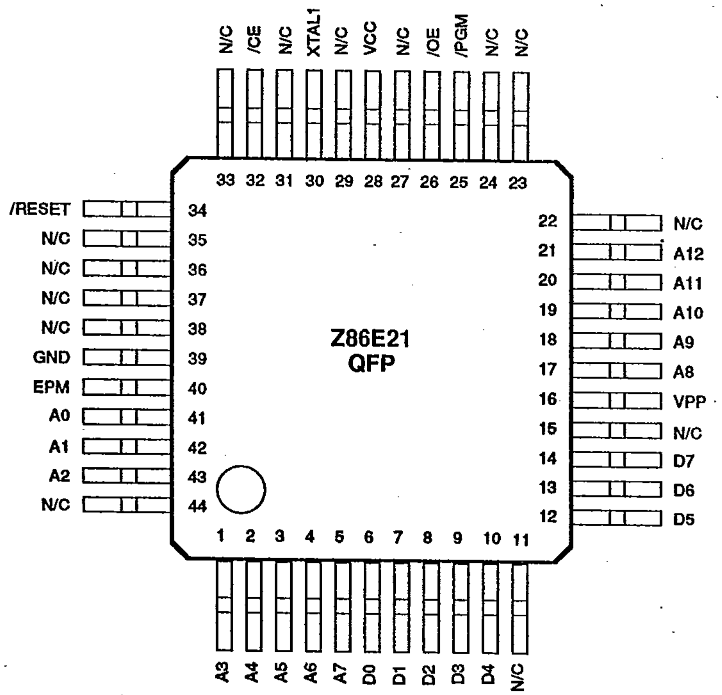


Figure 7. 44-Pin Quad Flat Pack Pin Assignments

Table 6. 44-Pin Quad Flat Pack Pin Identification (EPROM Mode)

Pin #	Symbol	Function	Direction
1-5	A3-A7	Address 3,4,5,6,7	Input
6-10	D0-D4	Data 0,1,2,3,4	In/Output
11	N/C	Not Connected	Input
12-14	D5-D7	Data 5,6,7	In/Output
15	N/C	Not Connected	Input
16	V_{PP}	Prog Voltage	Input
17-21	A8-A12	Address 8,9,10,11,12	Input
22-24	N/C	Not Connected	Input
25	/PGM	Prog Mode	Input
26	/OE	Output Enable	Input
27	N/C	Not Connected	Input
28	V_{CC}	Power Supply	Input
29	N/C	Not Connected	Input
30	XTAL1	Crystal, Oscillator Clock	Input
31	N/C	Not Connected	Input
32	/CE	Chip Enable	Input
33	N/C	Not Connected	Input
34	/RESET	Reset	Input
35-38	N/C	Not Connected	Input
39	GND	Ground, GND	Input
40	EPM	EPROM Prog Mode	Input
41-43	A0-A2	Address 0,1,2	Input
44	N/C	Not Connected	Input

PIN FUNCTIONS

ROMless. (input, active Low). This pin when connected to GND disables the internal ROM and forces the device to function as a Z86C91 ROMless Z8 (note that, when left unconnected or pulled high to Vcc, the part will function as a normal Z86E21 EPROM version). This pin is only available on the 44-pin version of the Z86E21.

/DS. (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS. (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is via Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1, XTAL2. *Crystal 1, Crystal 2* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R/W. (output, write Low). The Read/Write signal is low when the MCU is writing to the external program or data memory.

/RESET. (input, active-Low). To avoid asynchronous and noisy reset problems, the Z86E21 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the 5th clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active low while /AS cycles at a rate of TpC/2. When /RESET is deactivated, program execution begins at location 000C (HEX). Reset time must be held low for 50 mS, or until Vcc is stable, whichever is longer.

Port 0 P00-P07. Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P04-P07. The lower nibble must have the same direction as the upper nibble to be under handshake control. For the ROMless option, Port 0 comes up as A15-A8 Address lines after /RESET.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibbles) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register. In ROMless mode, after a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode (Figure 8).

Port 1 P10-P17. Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports. For Z86E21, these eight I/O lines can be programmed as Input or Output lines or are configured under software control as an address/data port for interfacing external memory. When used as an I/O port, Port 1 can be placed under handshake control. In this configuration, Port 3 lines, P33 and P34, are used as the handshake controls RDY1 and /DAV1.

Memory locations greater than 8192 are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in high-impedance state along with Port 0, /AS, /DS and R//W, allowing the MCU to share common resources in multiprocessor and DMA applications. Data transfers are controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus request output (Figure 9).

PIN FUNCTIONS (Continued)

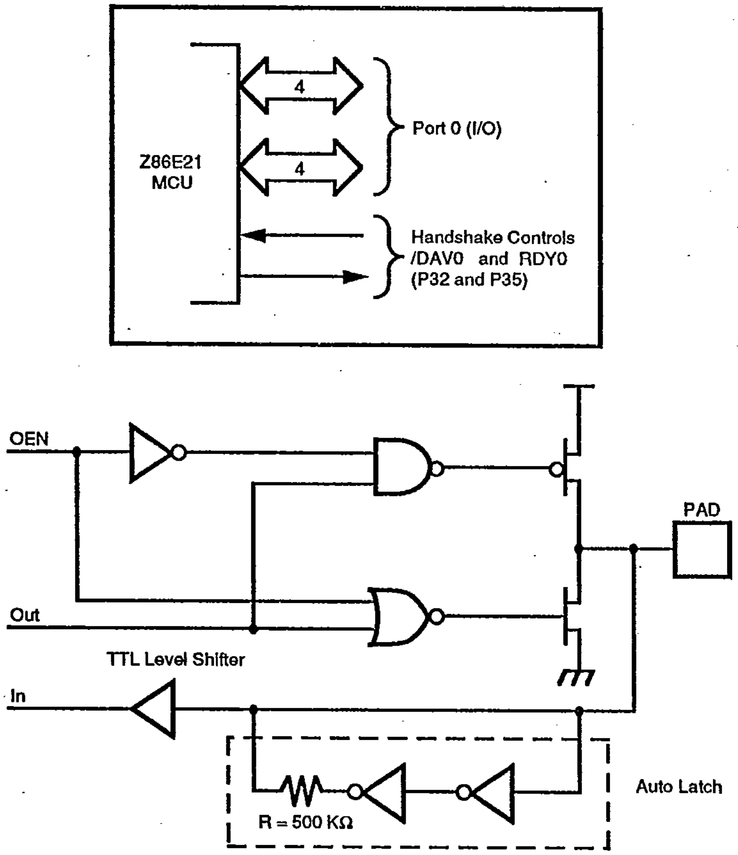
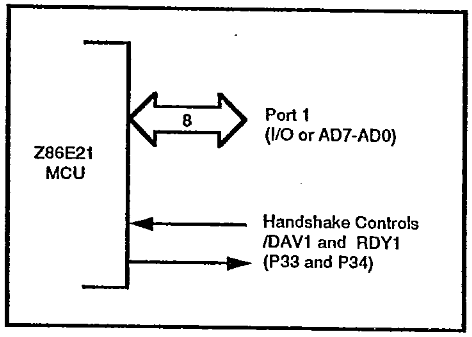


Figure 8. Port 0 Configuration

T-49-19-07



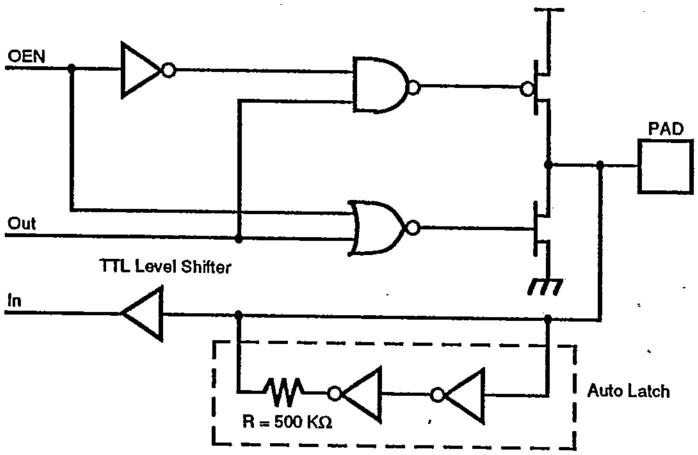


Figure 9. Port 1 Configuration

PIN FUNCTIONS (Continued)

Port 2 P20-P27. Port 2 is an 8-bit, bit programmable, bidirectional, CMOS compatible port. Each of these eight I/O lines can be independently programmed as an input or output, or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 can be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines, P31 and P36, is dictated by the direction (input or output) assigned to P27 (Figure 10 and Table 7).

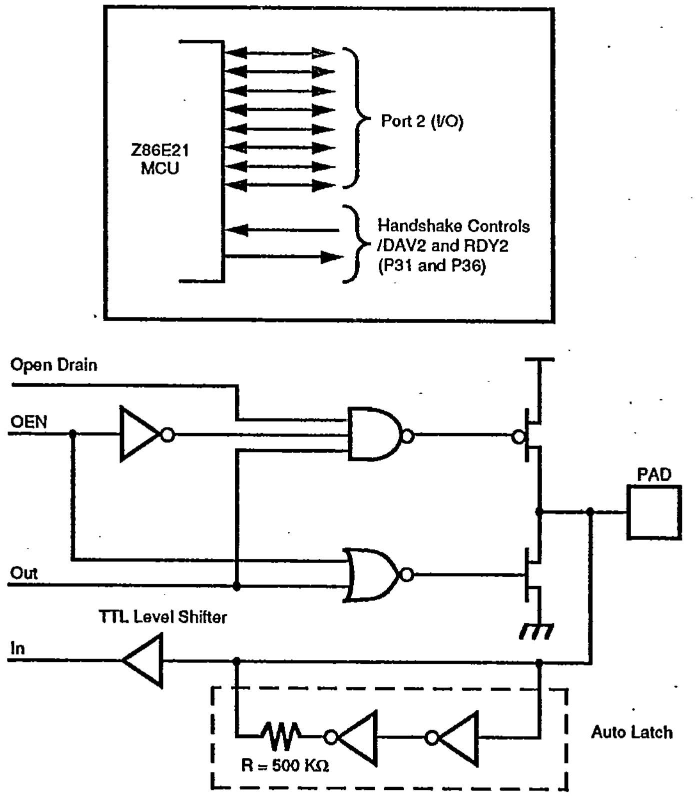


Figure 10. Port 2 Configuration

Port 3 P30-P37. Port 3 is an 8-bit, CMOS compatible four fixed input and four fixed output port. These 8 I/O lines have four-fixed (P33-P30) input and four fixed (P37-P34) output ports. Port 3, when used as serial I/O, is programmed as serial in and serial out, respectively (Figure 11).

T-49-19-07

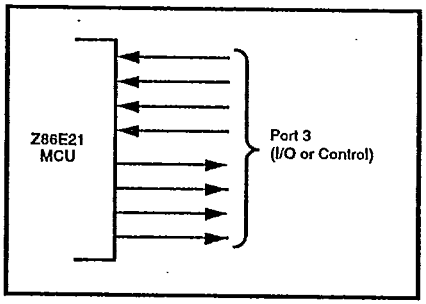


Figure 11. Port 3 Configuration

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ0-IRQ3); timer input and output signals (T_{IN} and T_{OUT}), Data Memory Select (/DM) and EPROM control signals (P30=/CE, P31=/OE, P32=EPM and P33=V_{PP}).

Table 7. Port 3 Pin Assignments

Pin	I/O	CTC1	Int.	P0 HS	P1 HS	P2 HS	UART	Ext	EPROM
P30	IN		IRQ3				Serial In		CE
P31	IN	T_{IN}	IRQ2			D/R			OE
P32	IN		IRQ0	D/R					EPM
P33	IN		IRQ1		D/R				V_{PP}
P34	OUT				R/D			DM	
P35	OUT			R/D					
P36	OUT	T_{OUT}				R/D			
P37	OUT						Serial Out		

Notes:
HS = Handshake Signals
D = Data Available
R = Ready

PIN FUNCTIONS (Continued)

Port 3 lines P30 and P37, are programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/Timer 0.

The Z86E21 automatically adds a start bit and two stop bits to transmitted data (Figure 12). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, 8 data bits, and at least one stop bit. If parity is on, bit-7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

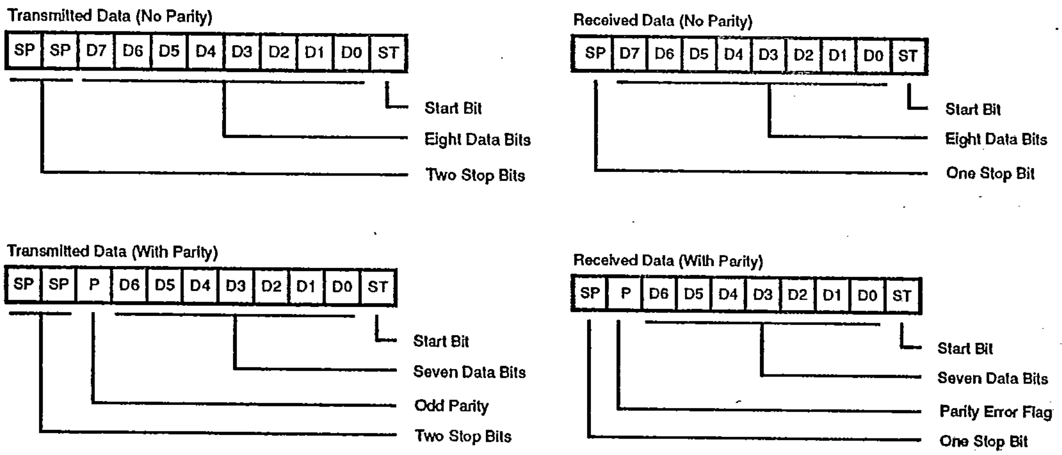


Figure 12. Serial Data Formats

Auto-Latch. The auto-latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not driven by any source.

Note: P30-P33 inputs differ from the Z86C21 because there is no clamping diode to V_{CC} due to the EPROM high voltage detection circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode

ADDRESS SPACE

Program Memory. The Z86E21 can address 56 Kbytes of external program memory (Figure 13). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 13 to byte 8191 consists of on-chip EPROM. At addresses 8192 and above, the Z86E21 executes external program memory fetches. In ROMless mode, the Z86E21 can address up to 64K bytes of program memory. Program execution begins at external location 000C (HEX) after a reset.

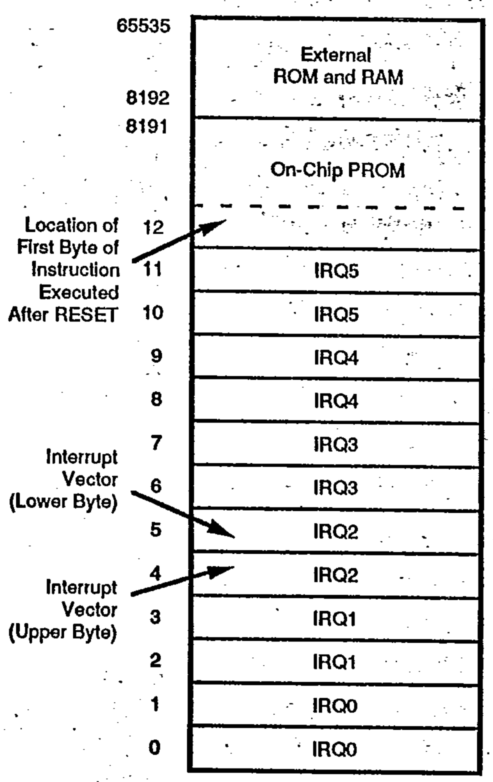


Figure 13. Program Memory Configuration

Data Memory (/DM). The EPROM version can address up to 56 Kbytes of external data memory space beginning at location 8192. The ROMless version can address up to 64 Kbytes of external data memory. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 14). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active low) memory.

Register File. The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control and status registers (Figure 15). The instructions can access registers directly or indirectly via an 8-bit address field. The Z86E21 also allows short 4-bit register addressing using the Register Pointer (Figure 16). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

T-49-19-07

Stack. The Z86E21 has a 16-bit Stack Pointer (R254-R255) used for external stacks that reside anywhere in the data memory for the ROMless mode, but only from 8192 to 65535 in the EPROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). The high byte of the Stack Pointer (SPH Bits 8-15) can be use as a general purpose register when using internal stack only.

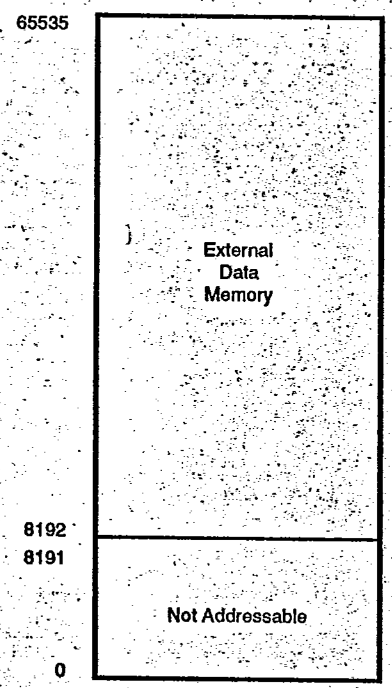


Figure 14. Data Memory Configuration

ADDRESS SPACE (Continued)

LOCATION		IDENTIFIERS
255	Stack Pointer (Bits 7-0)	SPL
254	Stack Pointer (Bits 15-8)	SPH
253	Register Pointer	RP
252	Program Control Flags	FLAGS
251	Interrupt Mask Register	IMR
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	T0 Prescaler	PRE0
244	Timer/Counter 0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter 1	T1
241	Timer Mode	TMR
240	Serial I/O	SIO
239 – 4	General-Purpose Registers	
3	Port 3	P3
2	Port 2	P2
1	Port1	P1
0	Port 0	P0

Figure 15. Register File

T-49-19-07

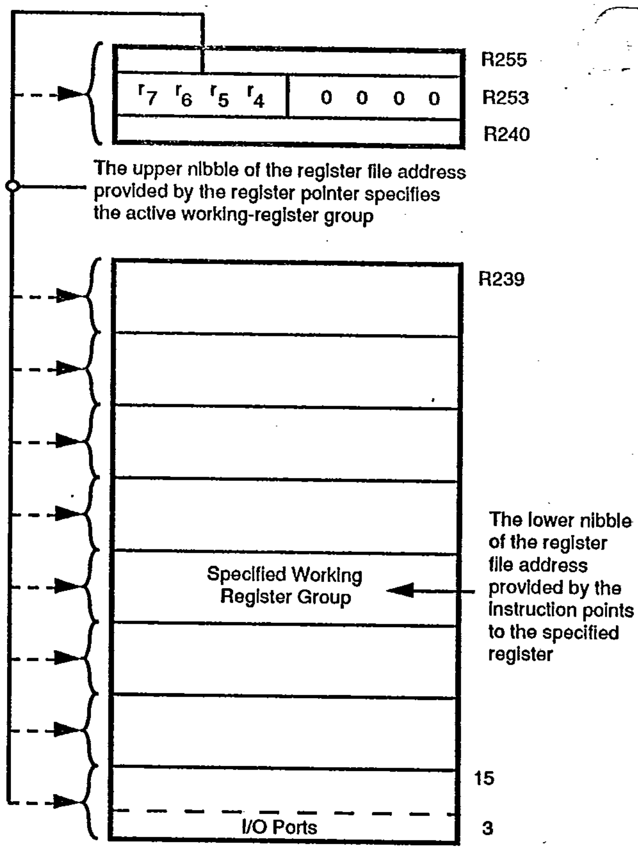


Figure 16. Register Pointer

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 17).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescalers reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter is programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as a timer output (T_{OUT}) through which T0, T1, or the internal clock can be output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

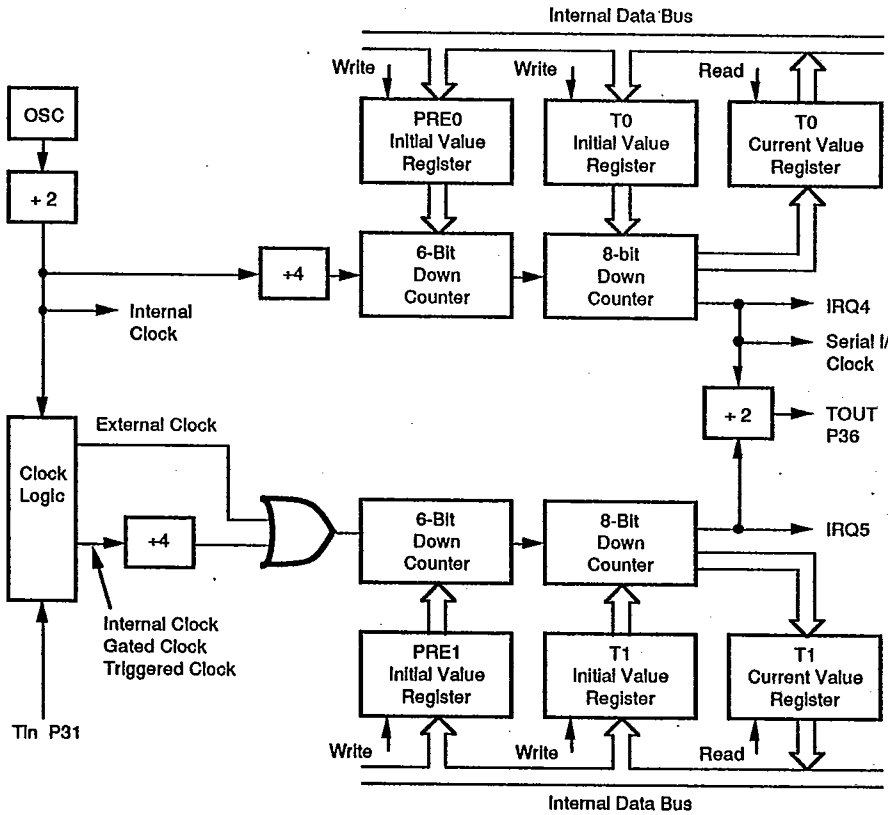


Figure 17. Counter/Timers Block Diagram

Interrupts. The Z86E21 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The 8 sources are divided as follows: four sources are claimed by Port 3 lines P30-P33, one in Serial Out, one in Serial In, and two in the counter/timers (Figure 18). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register.

All Z86E21 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialed interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

T-49-19-07

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

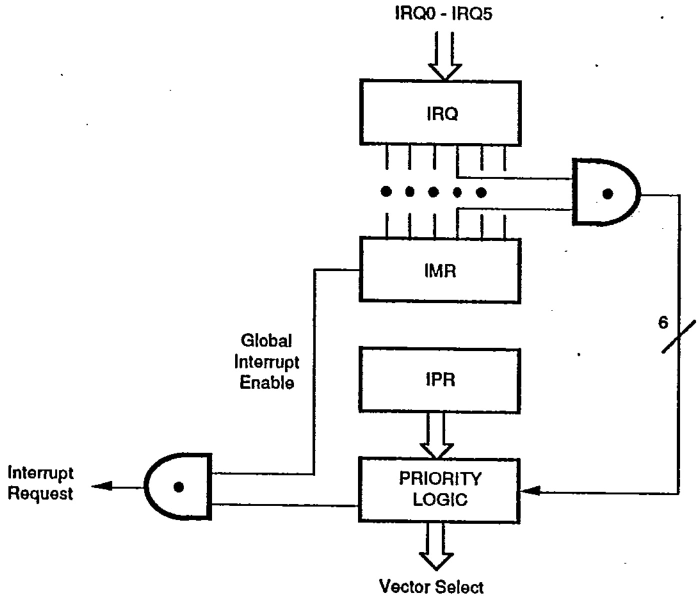


Figure 18. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86E21 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1=Input, XTAL2=Output). The crystal should be AT cut, 1 MHz to 16 MHz max; series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 100 pF) from each pin to ground (Figure 19).

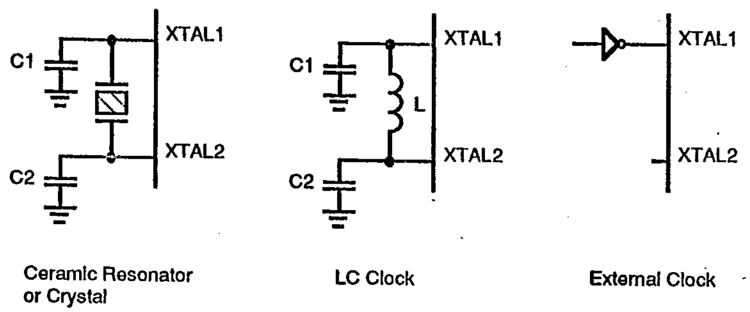


Figure 19. Oscillator Configuration

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated.

STOP. This instruction turns off the internal clock and external crystal oscillation, and reduces the standby current to 10 microamperes or less. The Stop mode is terminated by a reset, which cause the processor to restart the application program at address 000C (HEX).

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=OFFH) immediately before the appropriate sleep instruction. i.e.:

```
FF  NOP    ; clear the pipeline
6F  STOP   ; enter STOP mode
     or
FF  NOP    ; clear the pipeline
7F  HALT   ; enter HALT mode
```

PROGRAMMING

Z86E21 User Modes

The Z86E21 uses separate AC timing cycles for the different User Modes available. Table 8 shows the Z86E21 User Modes. Table 9 shows the timing of the programming waveforms.

User MODE 1 EPROM Read
The Z86E21 EPROM read cycle is provided so that the user may read the Z86E21 as a standard 2764A EPROM. This is accomplished by driving the /EPM pin (P32) to V_H and activating /CE and /OE. /PGM remains inactive. This mode is not valid after execution of an EPROM protect cycle. Timing for the EPROM read cycle is shown in Figure 20.

User MODE 2 EPROM Program
The Z86E21 Program function conforms to the Intelligent programming algorithm. The device is programmed with V_{CC} at 6.0V and V_{PP} = 12.5V. Programming pulses are applied in 1 msec increments to a maximum of 25 pulses before proper verification. After verification, a programming pulse of three times the duration of the cycles necessary to program the device is issued to insure proper programming. After all addresses are programmed, a final data comparison is executed and the programming cycle is complete. Timing for the Z86E21 programming cycle is shown in Figure 21.

User MODE 3 EPROM Verify

The Program Verify cycle is used as part of the Intelligent programming algorithm to insure data integrity under worst-case conditions. It differs from the EPROM read cycle in that V_{PP} is active and V_{CC} must be driven to 6.0V. Timing is shown in Figure 21.

User MODES 4 AND 5 EPROM and RAM Protect

To extend program security, EPROM and RAM protect cycles are provided for the Z86E21. Execution of the EPROM protect cycle prohibits proper execution of the EPROM Read, EPROM Verify, and EPROM programming cycles. Execution of the RAM protect cycle disables accesses to the upper 128 bytes of register memory (excluding mode and configuration registers), but first the user's program must set bit-6 of the IMR (R251). Timing is shown in Figure 22.

User MODE 6 4K/8K Size Selection

The Z86E21 allows the user to select the internal ROM size. This feature is useful in that once programmed, the Z86E21 knows at which address boundary to "go external." The Z8 distinguishes internal and external fetches using the data strobe (/DS). If programmed for 4K ROM, fetch cycles include /DS beginning at location 4096 (indicating an external memory fetch). If programmed for 8K ROM, /DS remains inactive until location 8192 is reached. Once the 4K ROM size option is selected, the upper 4K of address space is unusable in the Z86E21.

The timing of the 4K/8K size selection cycle is similar to the EPROM and RAM protect cycles. Note that the 4K/8K size selection cycle requires that address 03 be indicated on the address bus during execution. Timing is shown in Figure 22.

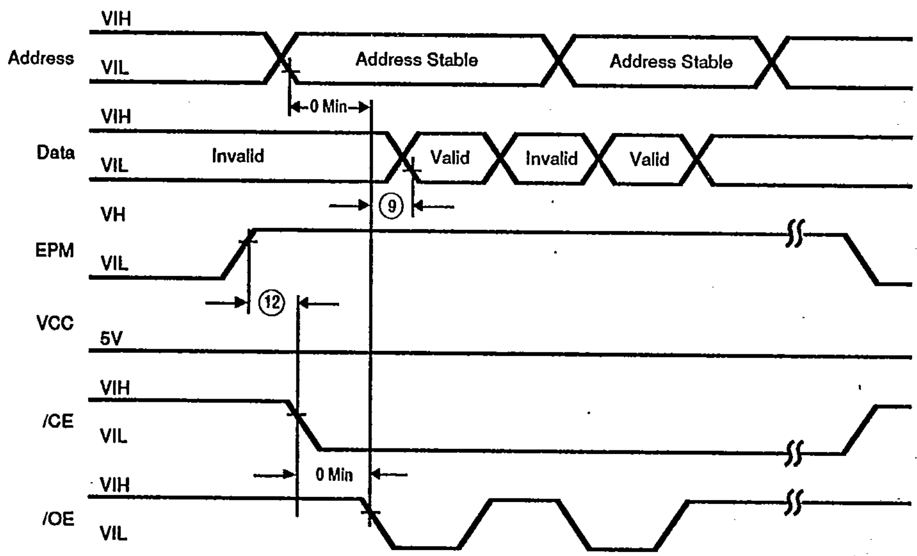
Table 8. OTP Programming Table

Mode	V_{PP}	EPM	CE	OE	PGM	V_{CC}	ADDR	Data
1. EPROM Read	X	V_H	V_{IL}	V_{IL}	V_{IH}	5.0	ADDR	DATA OUT
2. Program	V_{PP}	X	V_{IL}	V_{IH}	V_{IL}	6.0	ADDR	DATA IN
3. Program Verify	V_{PP}	X	V_{IL}	V_{IL}	V_{IH}	6.0	ADDR	DATA OUT
4. EPROM Protect	V_{PP}	V_H	V_H	V_{IH}	V_{IL}	6.0	X	X
5. RAM Protect	V_{PP}	X	V_H	V_{IH}	V_{IL}	6.0	X	X
6. 4K/8K Size Selection*	V_{PP}	V_H	V_H	V_H	V_{IL}	6.0	03	X

Notes:
V_{PP} = 12.5 ± 0.5 V
V_{CC} = 6.0 during programming
V_H = 12.5 ± 0.5 V
X = irrelevant
V_{IH} = 5.0 V
V_{IL} = 0 V
* If not programmed, the EPROM size is 8K.

Table 9. Timing of Programming Waveforms

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95	1.05	ms
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85	78.75	ms
12	EPM Setup Time	2		µs
13	/OE Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width		78.75	ms



Note:
VPP is Irrelevant
PGM is at VIH

Figure 20. Programming Waveform (User Mode 1)

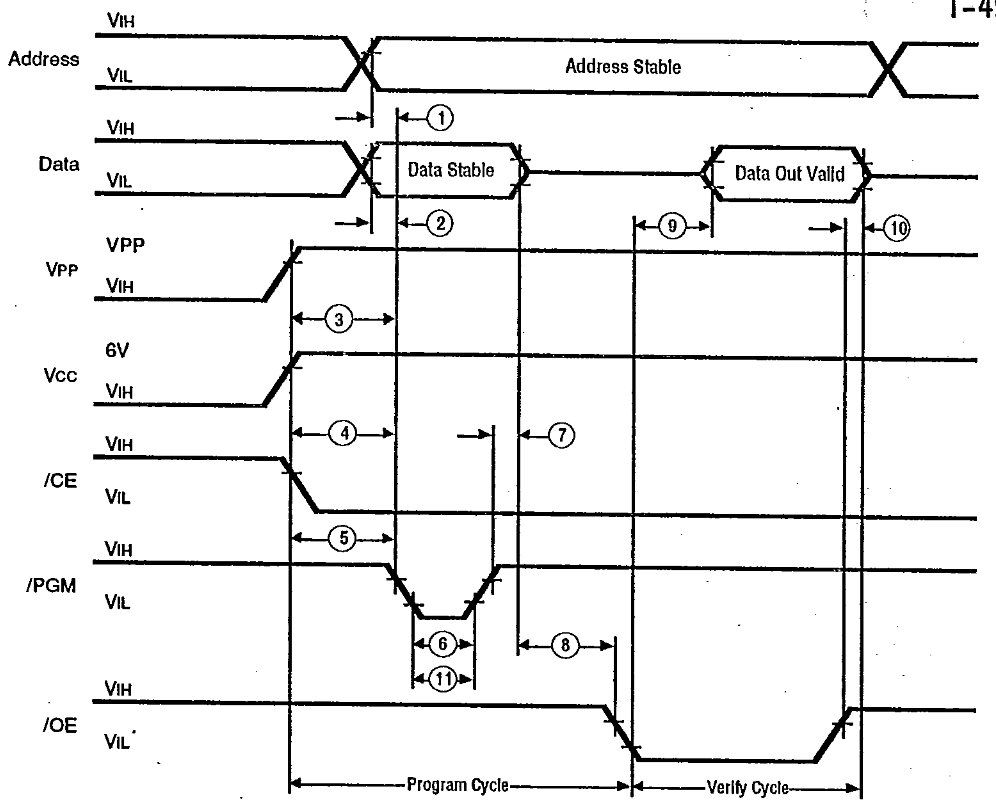


Figure 21. Programming Waveform (User Mode 2, 3)

T-49-19-07

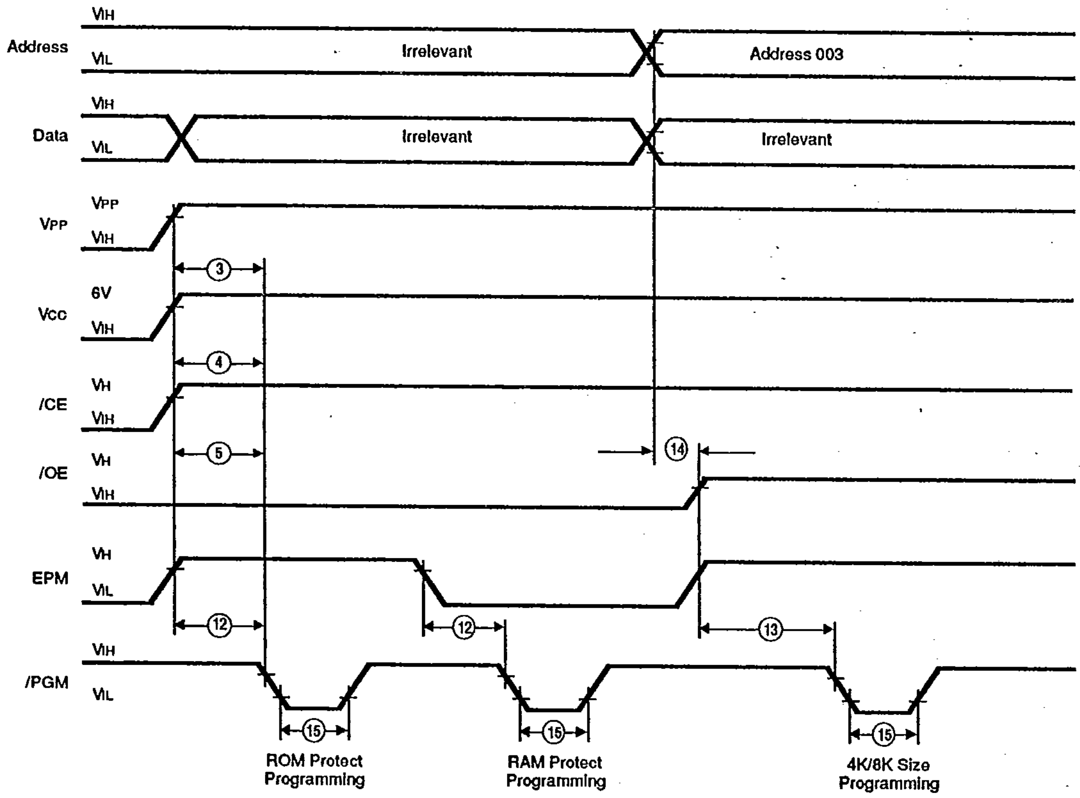


Figure 22. Programming Waveform (User Mode 4,5,6)

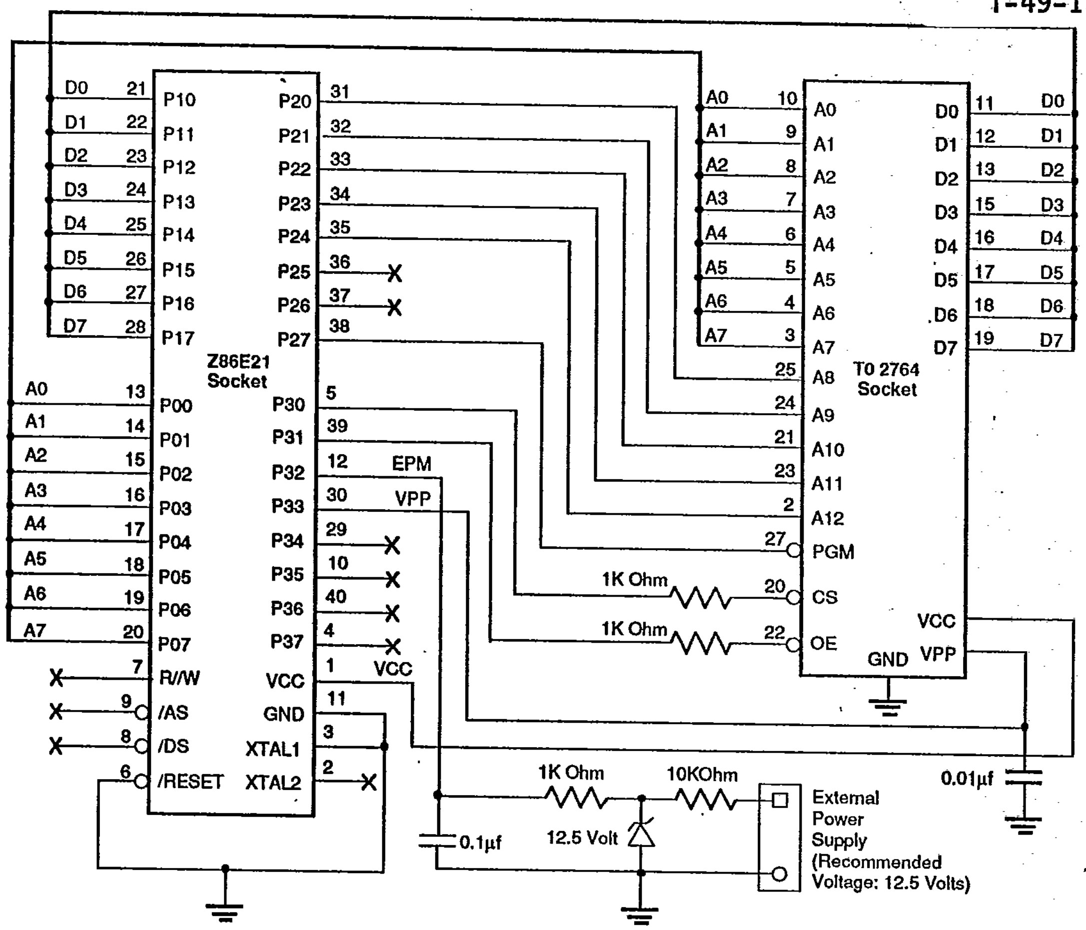


Figure 23. Z86E21 Z8 OTP Programming Adapter

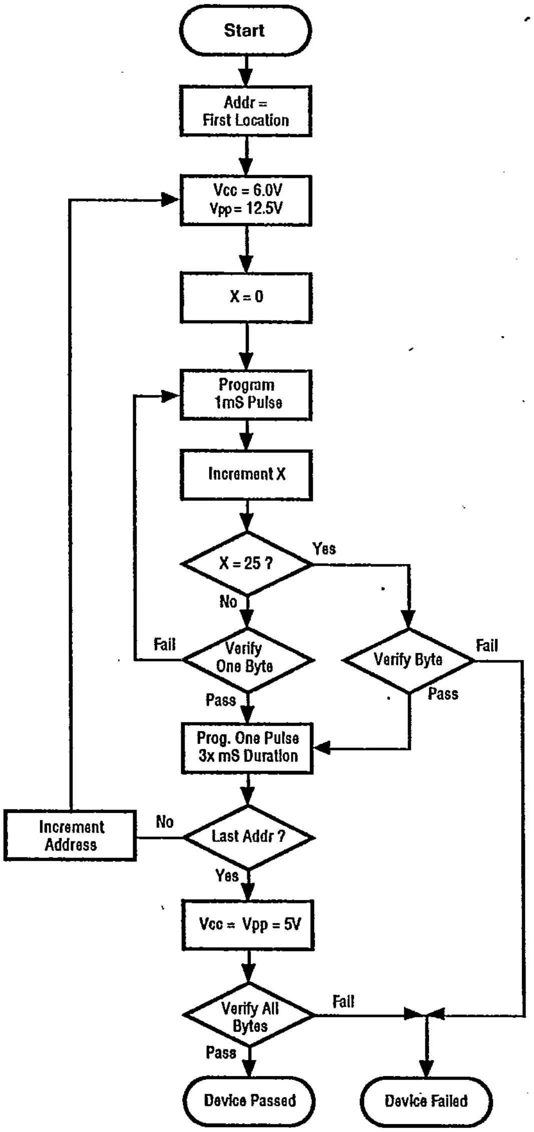


Figure 24. Intelligent Programming Flowchart

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	-0.3	+7.0	V
T_{STG}	Storage Temp	-65	+150	C
T_A	Oper Ambient Temp		†	C

Notes:
* Voltages on all pins with respect to GND.
  13.0 V Maximum on P30-P33.

† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 25).

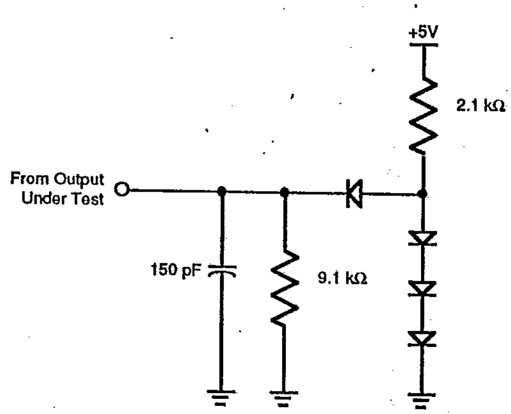


Figure 25. Test Load Diagram

DC CHARACTERISTICS

Sym	Parameter	T_A = 0°C to 70°C Min	Max	T_A = -40°C to105°C Min	Max	Typical at 25°C	Units	Conditions
	Max Input Voltage		7		7		V	I_{IN} 250 μA
	Max Input Voltage		13		13		V	P30-P33 Only
V_{CH}	Clock Input High Voltage	3.8	V_{CC}	3.8	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	-0.03	0.8	-0.03	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}	2.0	V_{CC}		V	
V_{IL}	Input Low Voltage	-0.3	0.8	-0.3	0.8		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = -2.0 mA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OL} = +2.0 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}	3.8	V_{CC}		V	
V_{RI}	Reset Input Low Voltage	-0.03	0.8	-0.03	0.8		V	
I_{IL}	Input Leakage	-10	10	-10	10		μA	0V V_{IN} +5.25V
I_{OL}	Output Leakage	-10	10	-10	10		μA	0V V_{IN} +5.25V
I_{IR}	Reset Input Current		-50		-50		μA	V_{CC}= +5.25V, V_{RL} = 0V
I_{CC}	Supply Current		50		50	25	mA	@ 12 MHz
			60		60	35	mA	@ 16 MHz
I_{CC1}	Standby Current		15		15	5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz
			20		20	10	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 16 MHz
I_{CC2}	Standby Current		20		20	5	μA	STOP Mode V_{IN} = 0V, V_{CC} @ 12 MHz
			20		20	5	μA	STOP Mode V_{IN} = 0V, V_{CC} @ 16 MHz

Notes:
I_{CC2} requires loading TMR (%F1H) with any value prior to STOP execution.
Use this sequence:

```
LD TMR,#00
NOP
STOP
```

AC CHARACTERISTICS

External I/O or Memory Read or Write Timing Diagram

T-49-19-07

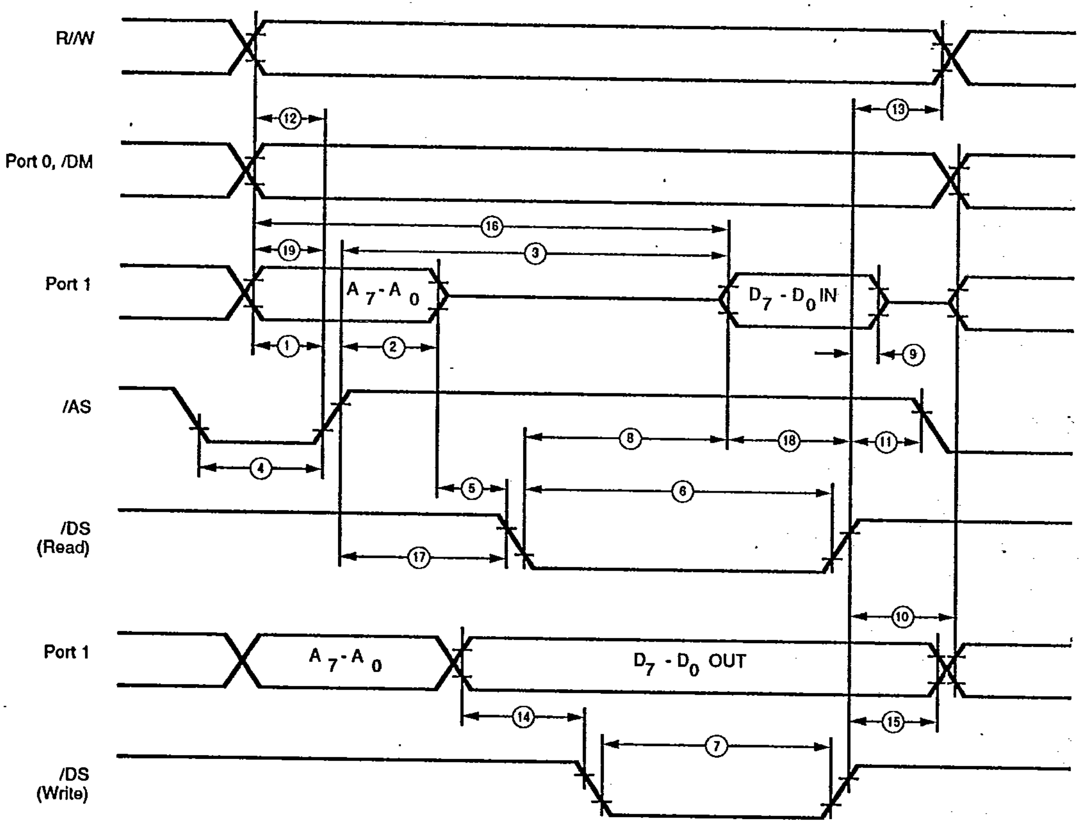


Figure 26. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS
External I/O or Memory Read and Write Timing Table

No	Symbol	Parameter	T_A = 0°C to 70°C 12 MHz Min	Max	16 MHz Min	Max	T_A = -40°C to 105°C 12 MHz Min	Max	16 MHz Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	35		20		35		25		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	45		30		45		35		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid		220		180		250		180	ns	[1,2,3]
4	TwAS	/AS Low Width	55		35		55		40		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	185		135		185		135		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	110		80		110		80		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid		130		75		130		75	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	0		0		0		0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	45		35		65		50		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	55		30		45		35		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	30		20		33		25		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R/W Not Valid	35		30		50		35		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	35		25		35		25		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	35		30		55		35		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		255		200		310		230	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	55		40		65		45		ns	[2,3]
18	TdDI(DS)	Data Input Setup to /DS Rise	75		60		75		60		ns	[1,2,3]
19	TdDM(AS)	/DM Valid to /AS Fall Delay	50		30		50		30		ns	[2,3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.

Standard Test Load

All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40TpC + 0.32
2	TdAS(A)	0.59TpC - 3.25
3	TdAS(DR)	2.38TpC + 6.14
4	TwAS	0.66TpC - 1.65
6	TwDSR	2.33TpC - 10.56
7	TwDSW	1.27TpC + 1.67
8	TdDSR(DR)	1.97TpC - 42.5
10	TdDS(A)	0.8TpC
11	TdDS(AS)	0.59TpC - 3.14
12	TdR/W(AS)	0.4TpC
13	TdDS(R/W)	0.8TpC - 15
14	TdDW(DSW)	0.4TpC
15	TdDS(DW)	0.88TpC - 19
16	TdA(DR)	4TpC - 20
17	TdAS(DS)	0.91TpC - 10.7
18	TsDI(DS)	0.8TpC - 10
19	TdDM(AS)	0.9TpC - 26.3

AC CHARACTERISTICS
Additional Timing Diagram

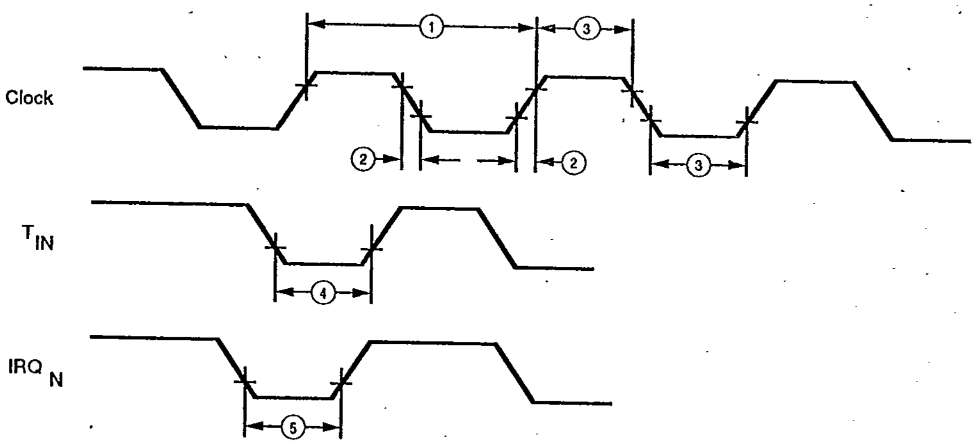


Figure 27. Additional Timing

AC CHARACTERISTICS
Additional Timing Table

No	Symbol	Parameter	T_A = 0°C to 70°C 12 MHz Min	Max	16 MHz Min	Max	T_A = -40°C to 105°C 12 MHz Min	Max	16 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	83	1000	62.5	1000	83	1000	62.5	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		15		10		15		10	ns	[1]
3	TwC	Input Clock Width	37		21		37		21		ns	[1]
4	TwTinL	Timer Input Low Width	75		50		75		50		ns	[2]
5	TwTinH	Timer Input High Width	3TpC		3TpC		3TpC		3TpC			[2]
6	TpTin	Timer Input Period	8TpC		8TpC		8TpC		8TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		100		100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		50		70		50		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	3TpC		3TpC		3TpC		3TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	3TpC		3TpC		3TpC		3TpC			[2,3]

Notes:
[1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request via Port 3.
[4] Interrupt request via Port 3 (P31-P33).
[5] Interrupt request via Port 30.

AC CHARACTERISTICS
Handshake Timing Diagrams

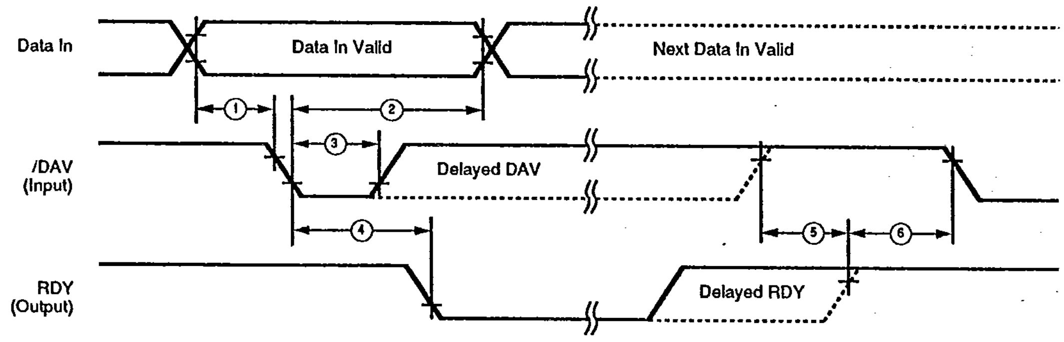


Figure 28. Input Handshake Timing

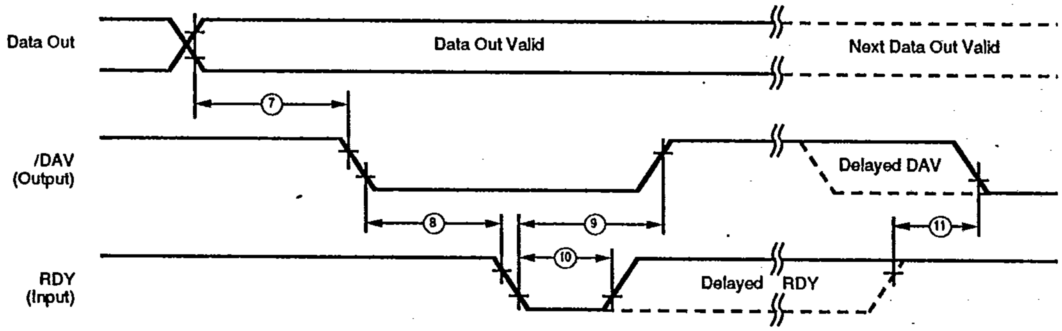


Figure 29. Output Handshake Timing

AC CHARACTERISTICS
Handshake Timing Table

No	Symbol	Parameter	T_A = 0°C to 70°C 12 MHz Min	Max	16 MHz Min	Max	T_A = -40°C to 105°C 12 MHz Min	Max	16 MHz Min	Max	Notes Data Direction
1	TsDI(DAV)	Data In Setup Time	0		0		0		0		
2	ThDI(DAV)	Data In Hold Time	145		145		145		145		IN
3	TwDAV	Data Available Width	110		110		110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay		115		115		115		115	IN
6	TdDO(DAV)	RDY Rise to DAV Fall Delay	0		0		0		0		IN
7	TcLDAVO(RDY)	Data Out to DAV Fall Delay		TpC		TpC		TpC		TpC	OUT
8	TcLDAVO(RDY)	DAV Fall to RDY Fall Delay	0		0		0		0		OUT
9	TdRDYO(DAV)	RDY Fall to DAV Rise Delay		115		115		115		115	OUT
10	TwRDY	RDY Width	110		110		110		110		OUT
11	TdRDYOd(DAV)	RDY Rise to DAV Fall Delay		115		115		115		115	OUT

Z8 CONTROL REGISTER DIAGRAMS

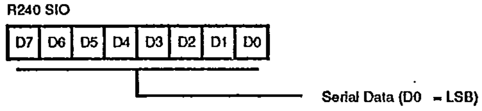


Figure 30. Serial I/O Register (F0H: Read/Write)

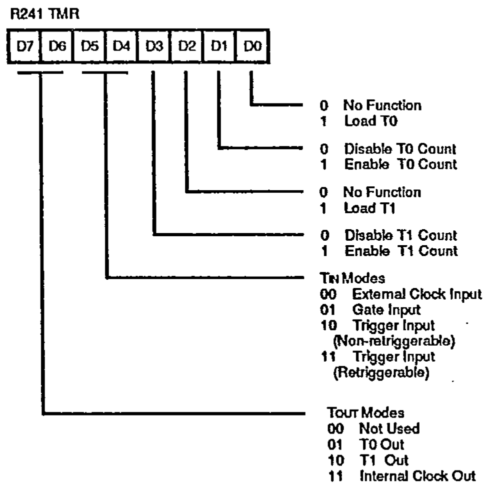


Figure 31. Timer Mode Register (F1H: Read/Write)

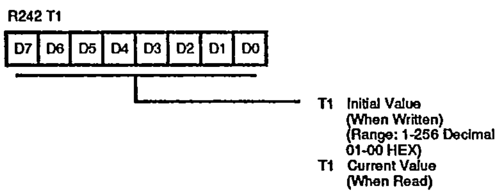


Figure 32. Counter/Timer 1 Register (F2H: Read/Write)

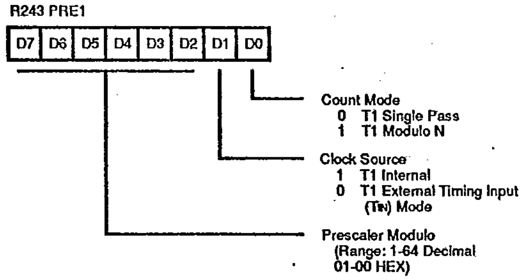


Figure 33. Prescaler 1 Register (F3H: Write Only)

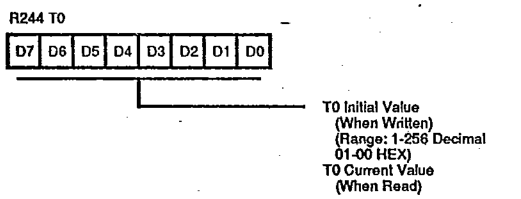


Figure 34. Counter/Timer 0 Register (F4H: Read/Write)

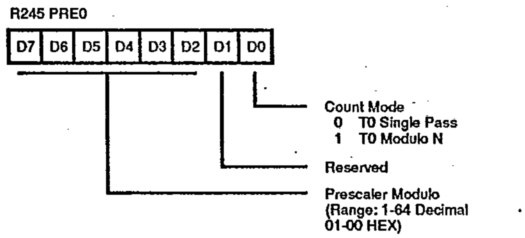


Figure 35. Prescaler 0 Register (F5H: Write Only)

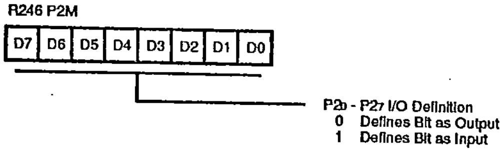


Figure 36. Port 2 Mode Register (F6H: Write Only)

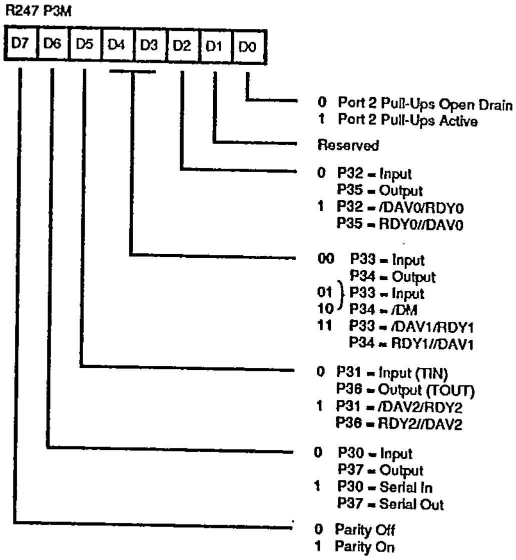


Figure 37. Port 3 Mode Register (F7H: Write Only)

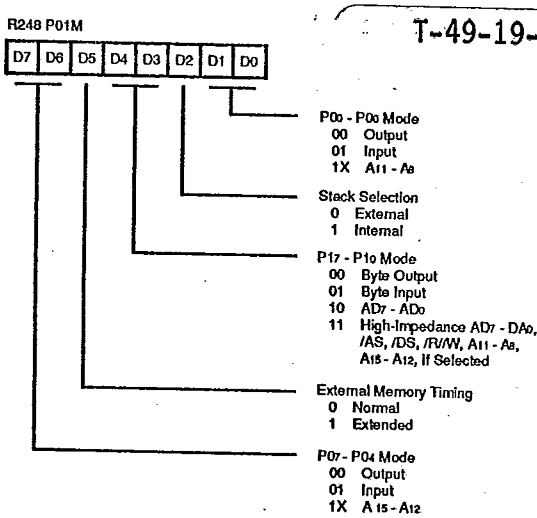


Figure 38. Port 0 and 1 Mode Register (F8H: Write Only)

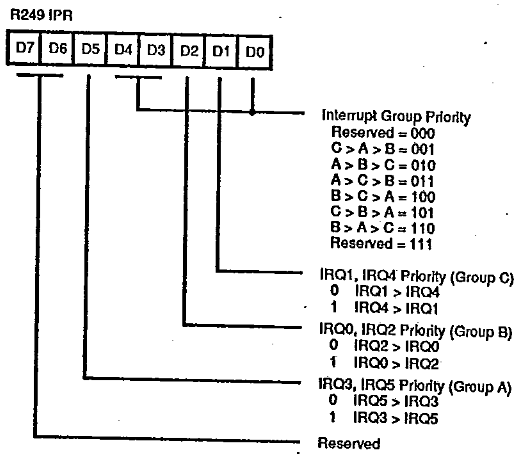


Figure 39. Interrupt Priority Register (F9H: Write Only)

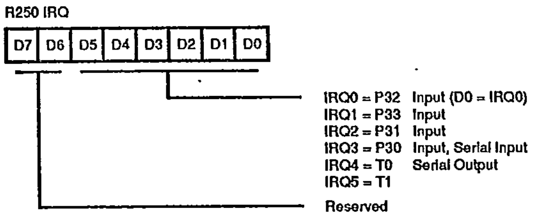


Figure 40. Interrupt Request Register (FAH: Read/Write)

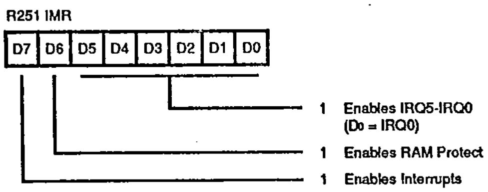


Figure 41. Interrupt Mask Register (FBH: Read/Write)

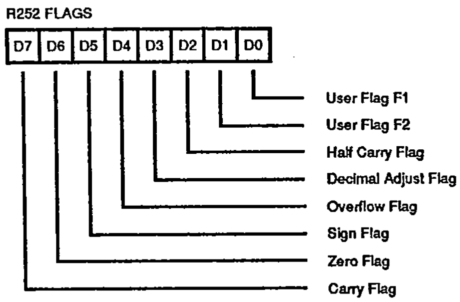


Figure 42. Flag Register (FCH: Read/Write)

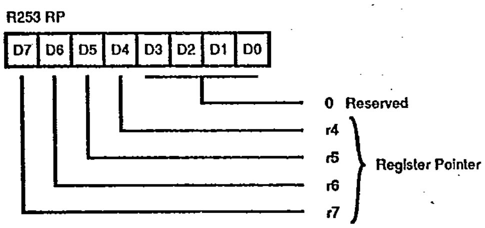


Figure 43. Register Pointer Register (FDH: Read/Write)

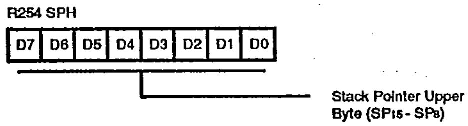


Figure 44. Stack Pointer Register (FEH: Read/Write)

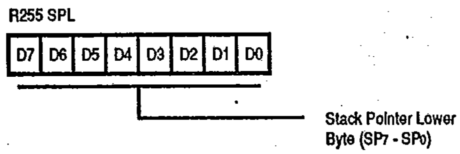


Figure 45. Stack Pointer Register (FFH: Read/Write)

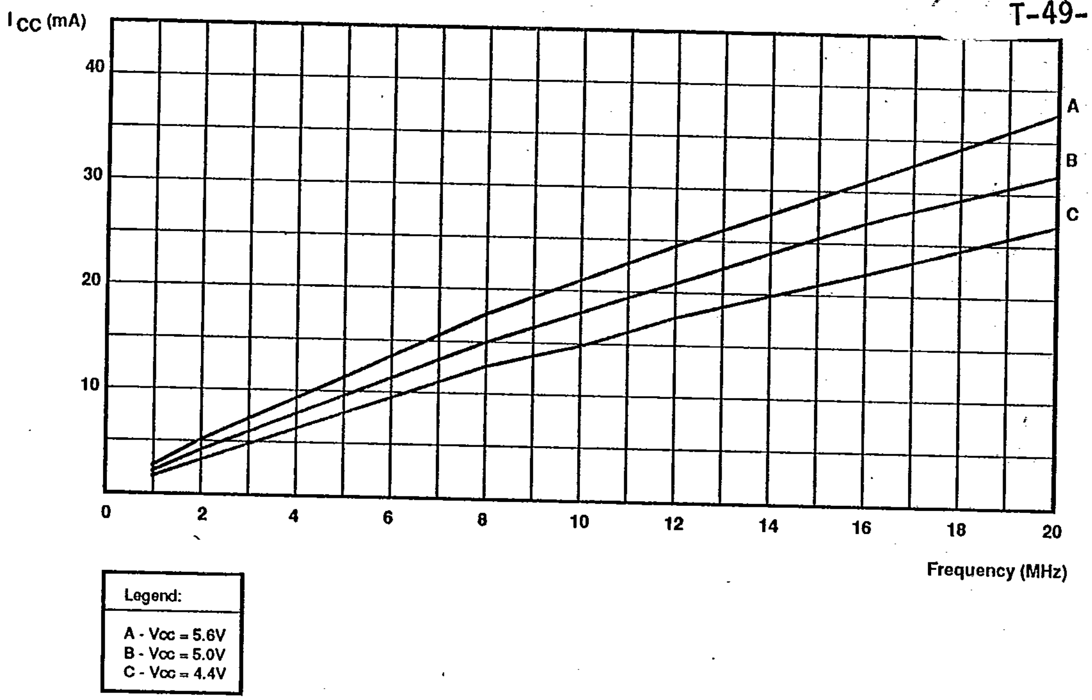


Figure 46. Typical I_{cc} vs Frequency

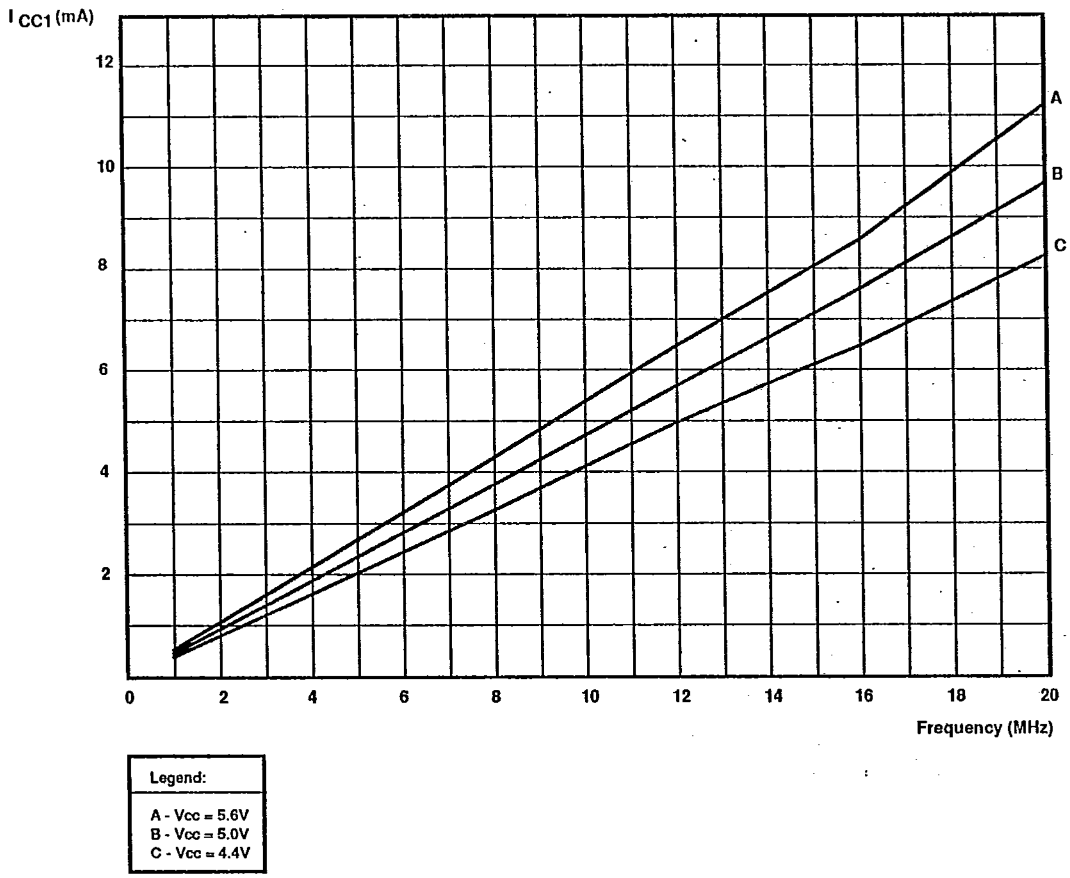


Figure 47. Typical I_{CC1} vs Frequency

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flages are indicated by:

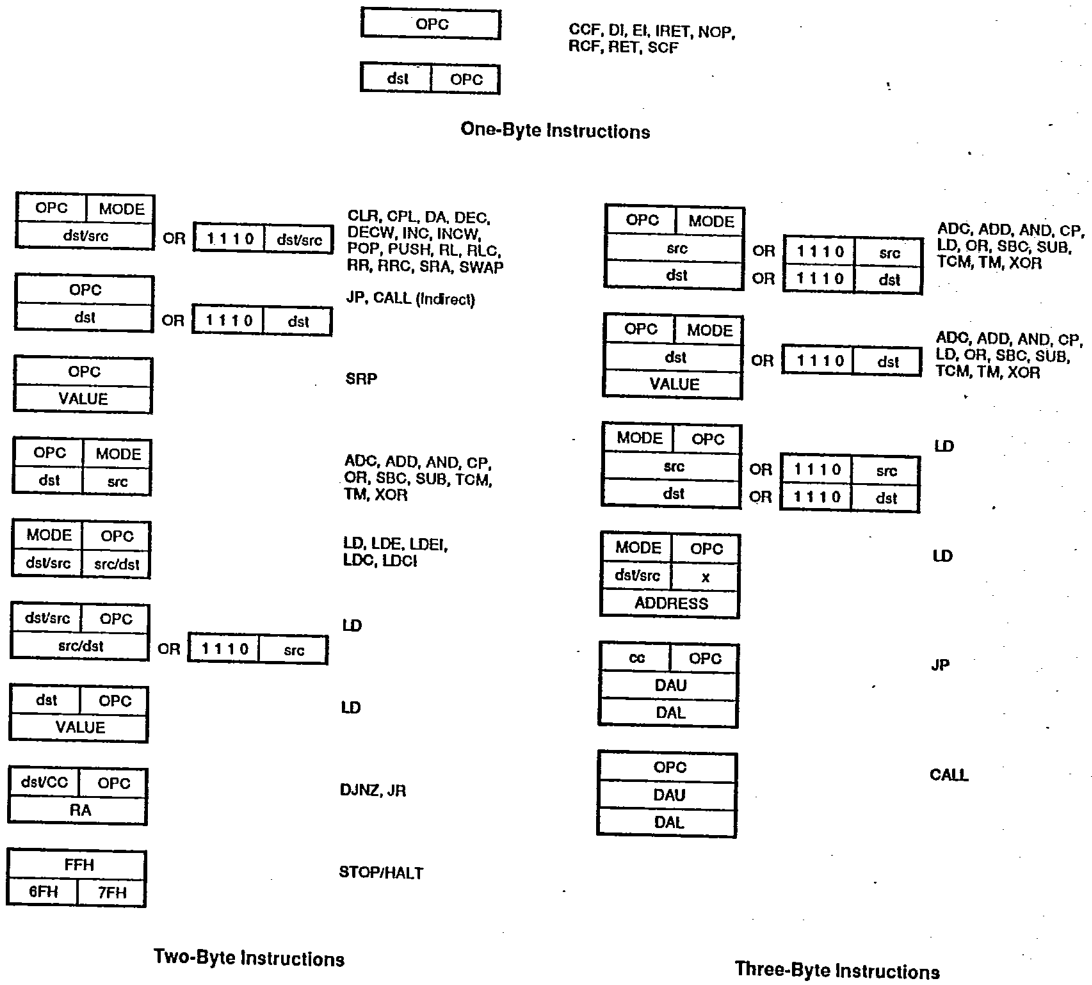
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

T-49-19-07

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000		Never True	

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "←". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

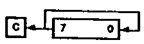
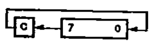
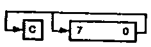
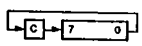
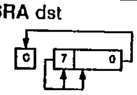
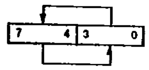
INSTRUCTION SUMMARY (Continued)

T-49-19-07

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst, src dst←dst + src +C	†		1[ ]	* * * * 0 *
ADD dst, src dst←dst + src	†		0[ ]	* * * * 0 *
AND dst, src dst←dst AND src	†		5[ ]	- * * 0 - -
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	- - - - - -
CCF C←NOT C			EF	* - - - - -
CLR dst dst←0	R IR		B0 B1	- - - - - -
COM dst dst←NOT dst	R IR		60 61	- * * 0 - -
CP dst, src dst - src	†		A[ ]	* * * * - -
DA dst dst←DA dst	R IR		40 41	* * * X - -
DEC dst dst←dst - 1	R IR		00 01	- * * * - -
DECW dst dst←dst - 1	RR IR		80 81	- * * * - -
DI IMR(7)←0			8F	- - - - - -
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128	RA		rA r = 0 - F	- - - - - -
EI IMR(7)←1			9F	- - - - - -
HALT			7F	- - - - - -

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
INC dst dst←dst + 1	r R IR		rE r = 0 - F 20 21	- * * * - -
INCW dst dst←dst + 1	RR IR		A0 A1	- * * * - -
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	* * * * * *
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 - F 30	- - - - - -
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c = 0 - F	- - - - - -
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	- - - - - -
LDC dst, src	r	Irr	C2	- - - - - -
LDCI dst, src dst←src r←r +1; rr←rr + 1	Ir	Irr	C3	- - - - - -

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP - 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

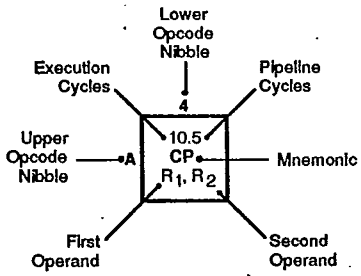
Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex) across; Upper Nibble (Hex) down.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2												6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1												6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r2, Irr1	18.0 **LDCI** Ir2, Irr1	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2				3				2					3	1	

Bytes per Instruction



Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_2 = Dst address
R_1 or r_2 = Src address

Sequence:
Opcode, First Operand,
Second Operand

Note: The blank are not defined.

* 2-byte instruction appears as a 3-byte instruction