



512Kx16 SRAM MODULE ADVANCED*

FEATURES

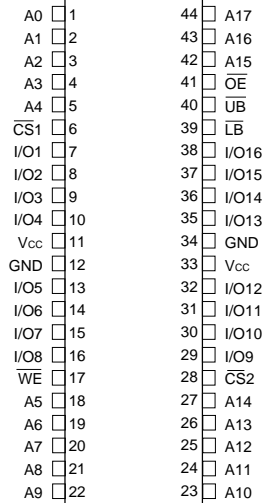
- Access Times 17, 20, 25, 35ns
- MIL-STD-883 Compliant Devices Available
- Packaging
 - 44 pin Ceramic SOJ (Package 102)
 - 44 lead Ceramic Flatpack (Package 209)
- Organized as two banks of 256Kx16
- Data Byte Control:
 - Lower Byte (\overline{LB}) = I/O1-8
 - Upper Byte (\overline{UB}) = I/O9-16
- Data I/O Compatible with 3.3V devices
- 2V Minimum Data Retention for battery back up operation
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply (3.3V parts also available)
- Low Power CMOS
- TTL Compatible Inputs and Outputs

* This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.

PIN CONFIGURATION FOR WS512K16-XXX

44 CSOJ
44 FLATPACK

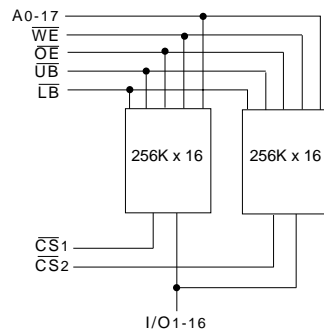
TOP VIEW



PIN DESCRIPTION

A0-17	Address Inputs
\overline{LB}	Lower-Byte Control (I/O1-8)
\overline{UB}	Upper-Byte Control (I/O9-16)
I/O1-16	Data Input/Output
$\overline{CS1-2}$	Chip Select
\overline{OE}	Output Enable
\overline{WE}	Write Enable
Vcc	+5.0V Power
GND	Ground
NC	No Connection

BLOCK DIAGRAM





TRUTH TABLE

CS ₁	CS ₂	WE	OE	LB	UB	Mode	Data I/O		Power
							I/O ₁₋₈	I/O ₉₋₁₆	
H	H	X	X	X	X	Not Select	High Z	High Z	Standby
L	H	H	H	X	X	Output Disable	High Z	High Z	Active
H	L								
L	H	X	X	H	H				
H	L								
H	L	H	L	L	H	Read	Data Out	High Z	Active
L	H			H	L		High Z	Data Out	
L	L			L	L		Data Out	Data Out	
H	L	L	X	L	H	Write	Data In	High Z	Active
L	H			H	L		High Z	Data In	
L	L			L	L		Data In	Data In	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

CAPACITANCE
(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C _{IN}	V _{IN} = 0V, f = 1.0MHz	25	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V, f = 1.0MHz	25	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS
(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	Min		Max		Units
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}			10		µA
Output Leakage Current	I _{LO}	CS = V _{IH} , OE = V _{IH} , V _{OUT} = GND to V _{CC}			10		µA
Operating Supply Current	I _{CC}	CS = V _{IL} , OE = V _{IH} , f = 5MHz, V _{CC} = 5.5			290		mA
Standby Current	I _{SB}	CS = V _{IH} , OE = V _{IH} , f = 5MHz, V _{CC} = 5.5			30		mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA, V _{CC} = 4.5			0.4		V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA, V _{CC} = 4.5	2.4				V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS
(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min			Units
				Typ	Max	
Data Retention Supply Voltage	V _{DR}	CS ≥ V _{CC} - 0.2V	2.0		5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 3V		2.0	12.0*	mA

* Also available in Low Power version. Please call factory for information.



AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle										
Read Cycle Time	t _{RC}	17		20		25		35		ns
Address Access Time	t _{AA}		17		20		25		35	ns
Output Hold from Address Change	t _{OH}	0		0		0		0		ns
Chip Select Access Time	t _{ACS}		17		20		25		35	ns
Output Enable to Output Valid	t _{OE}		10		12		15		20	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	2		5		5		5		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		9		10		12		15	ns
Output Disable to Output in High Z	t _{OHZ} ¹		9		10		12		15	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ Access Time	t _{BA}		10		12		14		17	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ Enable to Low Z Output	t _{BLZ} ¹	0		0		0		0		ns
$\overline{\text{LB}}, \overline{\text{UB}}$ Disable to High Z Output	t _{BHZ} ¹		9		10		12		15	ns

1. This parameter is guaranteed by design but not tested.

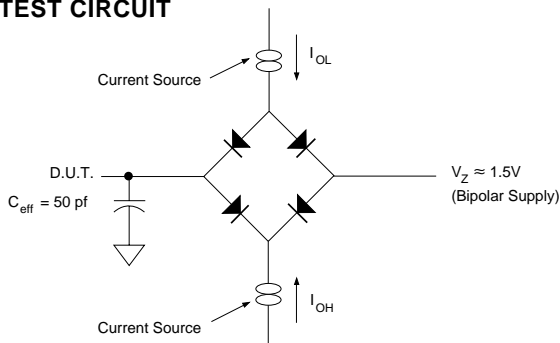
AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle										
Write Cycle Time	t _{WC}	17		20		25		35		ns
Chip Select to End of Write	t _{CW}	14		17		20		25		ns
Address Valid to End of Write	t _{AW}	14		17		20		25		ns
Data Valid to End of Write	t _{DW}	10		12		15		20		ns
Write Pulse Width	t _{WP}	14		17		20		25		ns
Address Setup Time	t _{AS}	0		0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		0		ns
Output Active from End of Write	t _{OW} ¹	0		0		0		0		ns
Write Enable to Output in High Z	t _{WHZ} ¹		9		10		10		15	ns
Data Hold Time	t _{DH}	0		0		0		0		ns
$\overline{\text{LB}}, \overline{\text{UB}}$ Valid to End of Write	t _{BW}	14		17		20		25		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT



AC TEST CONDITIONS

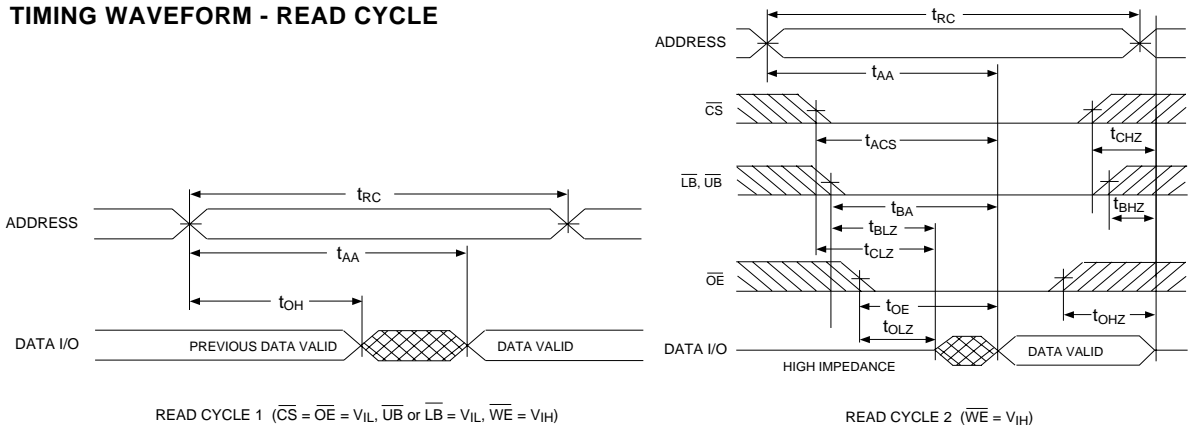
Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

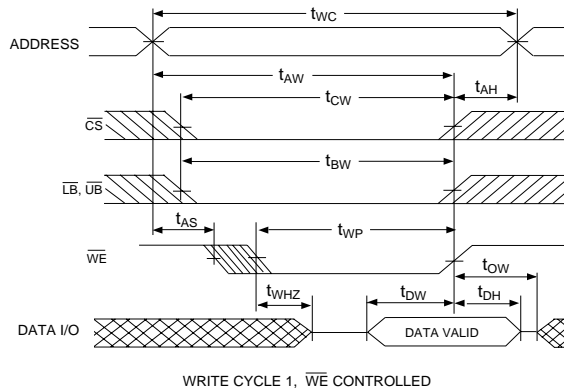
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



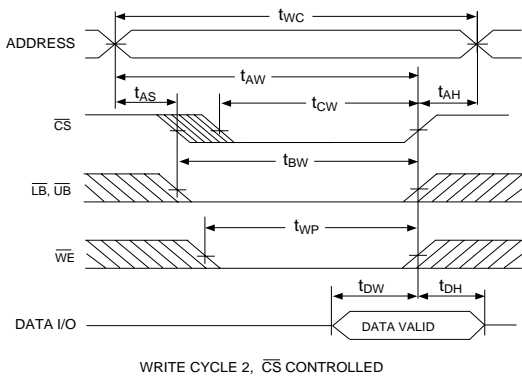
TIMING WAVEFORM - READ CYCLE



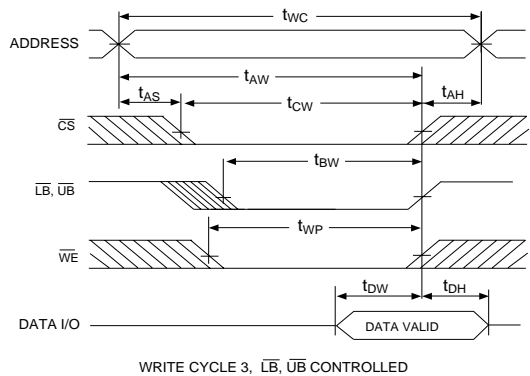
WRITE CYCLE - \overline{WE} CONTROLLED



WRITE CYCLE - \overline{CS} CONTROLLED

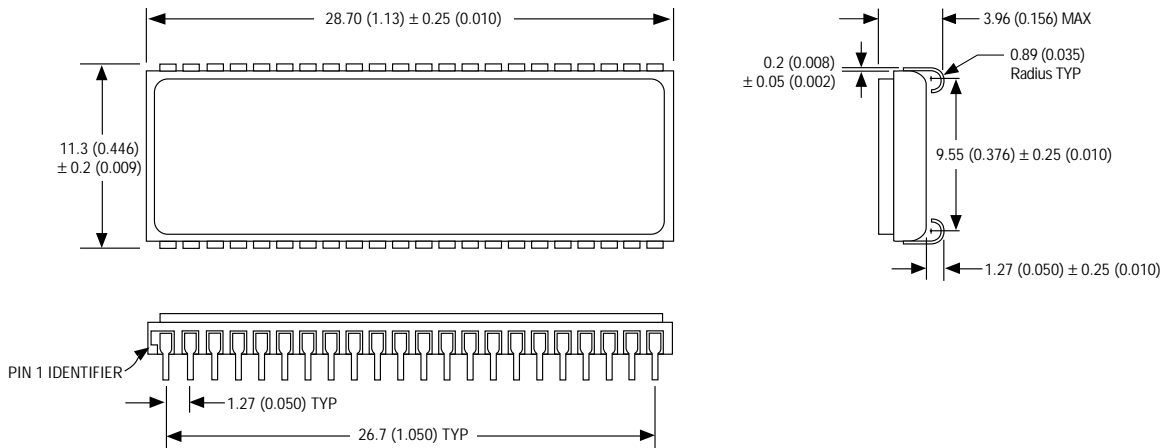


WRITE CYCLE - \overline{LB} , \overline{UB} CONTROLLED



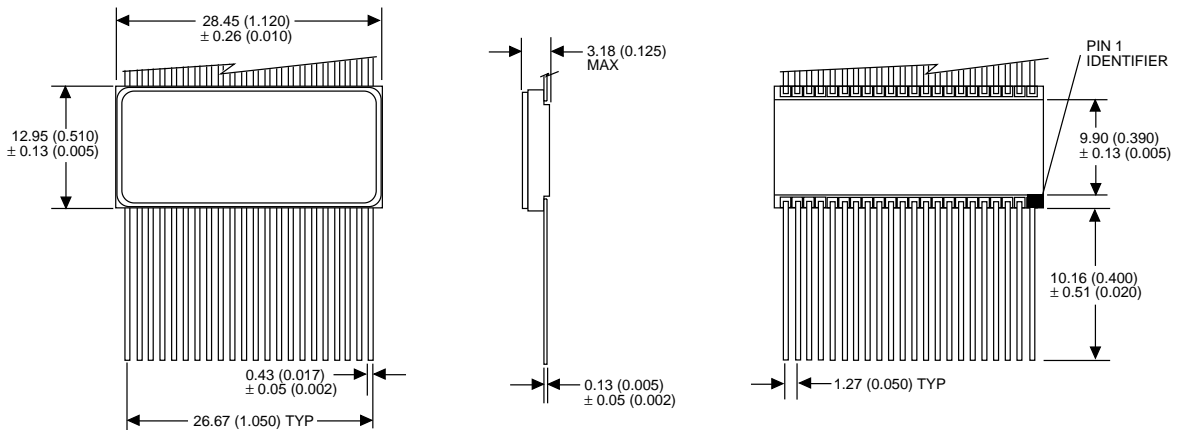


PACKAGE 102: 44 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 209: 44 LEAD, CERAMIC FLAT PACK



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ORDERING INFORMATION

W S 512K16 - XX X X X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

DEVICE GRADE:

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE:

DL = 44 Lead Ceramic SOJ (Package 102)

FL = 44 Lead Ceramic Flatpack (Package 209)

ACCESS TIME (ns)

ORGANIZATION, two banks of 256K x 16

SRAM

WHITE MICROELECTRONICS