



# 7GHz, 1:2 CML FANOUT BUFFER/TRANSLATOR WITH INTERNAL I/O TERMINATION

Precision Edge®  
SY58011U

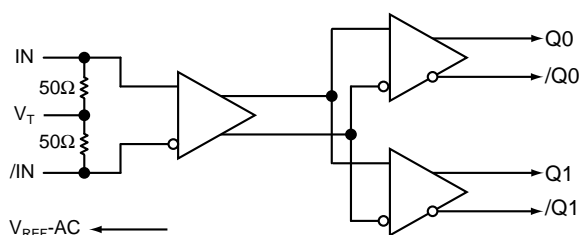
## FEATURES

- Precision 1:2, 400mV CML fanout buffer
- Guaranteed AC performance over temperature/voltage:
  - > 7GHz  $f_{MAX}$  clock
  - < 60ps  $t_r / t_f$  times
  - < 250ps  $t_{pd}$
  - < 15ps max. skew
- Low jitter performance:
  - < 10ps<sub>pp</sub> total jitter (clock)
  - < 1ps<sub>RMS</sub> random jitter (data)
  - < 10ps<sub>pp</sub> deterministic jitter (data)
- Accepts an input signal as low as 100mV
- Unique input termination and  $V_T$  pin accepts DC-coupled and AC-coupled differential inputs: LVPECL, LVDS, and CML
- 50Ω source terminated CML outputs
- Power supply 2.5V ±5% and 3.3V ±10%
- Industrial temperature range: -40°C to +85°C
- Available in 16-pin (3mm × 3mm) MLF® package

## APPLICATIONS

- All SONET and GigE clock distribution
- Fibre Channel clock and data distribution
- Backplanes
- Data distribution: OC-48, OC-48+FEC, XAUI
- High-end, low skew, multiprocessor synchronous clock distribution

## FUNCTIONAL BLOCK DIAGRAM



Precision Edge®

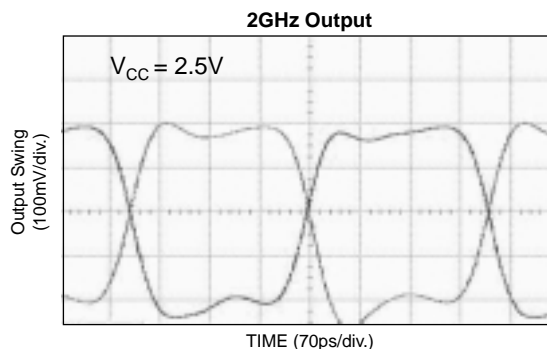
## DESCRIPTION

The SY58011U is a 2.5V/3.3V precision, high-speed, fully differential 1:2 CML fanout buffer. Optimized to provide two identical output copies with less than 15ps of skew and less than 10ps<sub>(pk-pk)</sub> total jitter, the SY58011U can process clock signals as fast as 7GHz or data patterns up to 10.7Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS, or CML differential signals, (AC-coupled or DC-coupled) as small as 100mV without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an on-board output reference voltage ( $V_{REF-AC}$ ) is provided to bias the  $V_T$  pin. The outputs are compatible with 400mV typical swing into 50Ω loads, with extremely fast rise/fall times guaranteed to be less than 60ps.

The SY58011U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). For applications that require LVPECL outputs, consider the SY58012U or SY58013U 1:2 fanout buffer with 800mV and 400mV output swing, respectively. The SY58011U is part of Micrel's high-speed, Precision Edge™ product line. Data sheets and support documentation can be found on Micrel's web site at [www.micrel.com](http://www.micrel.com).

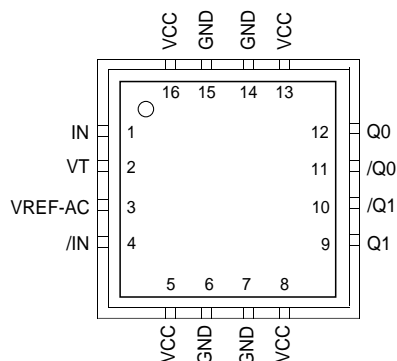
## TYPICAL PERFORMANCE



2GHz with 100mV Input

Precision Edge is a registered trademark of Micrel, Inc.  
MicroLeadFrame and MLF are registered trademarks of Amkor Technology, Inc.

**PACKAGE/ORDERING INFORMATION**



**16-Pin MLF<sup>®</sup> (MLF-16)**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58011UMI	MLF-16	Industrial	011U	Sn-Pb
SY58011UMITR <sup>(2)</sup>	MLF-16	Industrial	011U	Sn-Pb
SY58011UMG <sup>(3)</sup>	MLF-16	Industrial	011U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY58011UMGTR <sup>(2, 3)</sup>	MLF-16	Industrial	011U with Pb-Free bar-line indicator	Pb-Free NiPdAu

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

**PIN DESCRIPTION**

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair is the signal to be buffered. Each pin of this pair internally terminates with 50Ω to the $V_T$ pin. Note that this input will default to an indeterminate state if left open. See “Input Interface Applications” section.
2	VT	Input Termination Center-Tap: Each input terminates to this pin. The $V_T$ pin provides a center-tap for each input (IN, /IN) to a termination network for maximum interface flexibility. See “Input Interface Applications” section.
3	VREF-AC	Reference Output Voltage: This output biases to $V_{CC} - 1.2\text{V}$ . It is used when AC-coupling the inputs (IN, /IN). Connect $V_{REF-AC}$ directly to the $V_T$ pin. Bypass with 0.01μF low ESR capacitor to $V_{CC}$ . Maximum current source or sink is 0.5mA. See “Input Interface Applications” section.
5, 8, 13, 16	VCC	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors as close to the $V_{CC}$ pins as possible.
6, 7, 14, 15	GND, (Exposed Pad)	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
12, 11, 9, 10	Q0, /Q0, Q1, /Q1	CML Differential Output Pairs: Differential buffered output copy of the input signal. The output swing is typically 400mV. Unused output pairs may be left floating with no impact on jitter. See “CML Output Termination” section.

**Absolute Maximum Ratings**(Note 1)

Power Supply Voltage ( $V_{CC}$ ) ..... -0.5V to +4.0V  
 Input Voltage ( $V_{IN}$ ) ..... -0.5V to  $V_{CC}$   
 CML Output Voltage ( $V_{OUT}$ ) .....  $V_{CC}-1.0V$  to  $V_{CC}+0.5V$   
 Current ( $V_T$ )  
     Source or sink current on  $V_T$  pin .....  $\pm 100mA$   
 Input Current  
     Source or sink current on IN, /IN .....  $\pm 50mA$   
 Current ( $V_{REF}$ )  
     Source or sink current on  $V_{REF-AC}$ , **Note 4** .....  $\pm 1.5mA$   
 Lead Temperature Soldering, (20 seconds) ..... 260°C  
 Storage Temperature Range ( $T_{STORE}$ ) .... -65°C to +150°C

**Operating Ratings**(Note 2)

Supply Voltage ( $V_{CC}$ ) ..... +2.375V to +3.60V  
 Operating Temperature Range ( $T_A$ ) ..... -40°C to +85°C  
 Package Thermal Resistance, **Note 3**  
     MLF® ( $\theta_{JA}$ )  
         Still-Air ..... 60°C/W  
         500lfpm ..... 54°C/W  
     MLF® ( $\psi_{JB}$ ) ..... 33°C/W

**DC ELECTRICAL CHARACTERISTICS**(Note 5)

$T_A = -40^\circ C$  to  $+85^\circ C$

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CC}$	Power Supply Voltage		2.375		3.60	V
$I_{CC}$	Power Supply Current	Max. $V_{CC}$ , no load		75	95	mA
$V_{IH}$	Input HIGH Voltage	IN, /IN	$V_{CC}-1.2$		$V_{CC}$	V
$V_{IL}$	Input LOW Voltage	IN, /IN	0		$V_{IH}-0.1$	V
$V_{IN}$	Input Voltage Swing	see Figure 1a.	0.1		1.7	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing	see Figure 1b.	0.2		3.4	V
$R_{IN}$	Into $V_T$ Resistance		40	50	60	$\Omega$
$V_{REF-AC}$	Output Reference Voltage		$V_{CC}-1.3$	$V_{CC}-1.2$	$V_{CC}-1.1$	V
IN to $V_T$					1.28	V

**CML DC ELECTRICAL CHARACTERISTICS**(Note 5)

$V_{CC} = 3.3V \pm 10\%$  or  $2.5V \pm 5\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ;  $R_L = 100\Omega$  across each output pair, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage	Q0, /Q0, Q1, /Q1	$V_{CC}-0.020$	$V_{CC}-0.010$	$V_{CC}$	V
$V_{OUT}$	Output Voltage Swing	Q0, /Q0, Q1, /Q1; see Figure 1a	325	400		mV
$V_{DIFF\_OUT}$	Differential Output Voltage Swing	Q0, /Q0, Q1, /Q1; see Figure 1b	650	800		mV
$R_{OUT}$	Output Source Impedance	Q0, /Q0, Q1, /Q1	40	50	60	$\Omega$

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (gnd) on the pcb.
4. Due to the limited drive capability, use for input of the same package only.
5. The circuit is designed to meet the dc specifications shown in the above table after thermal equilibrium has been established.

### AC ELECTRICAL CHARACTERISTICS (Note 7)

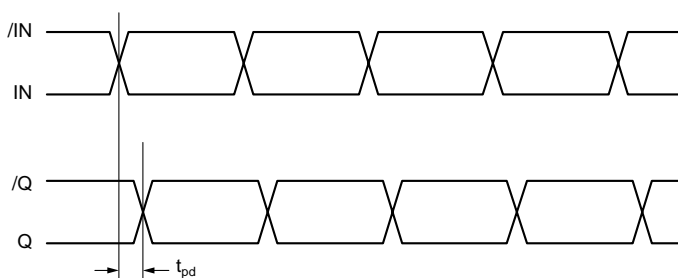
$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ;  $R_L = 100\Omega$  across each output pair, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Operating Frequency	NRZ Data		10.7		Gbps
		$V_{OUT} \geq 200mV$ Clock	7	8		GHz
$t_{pd}$	Propagation Delay	$V_{IN} \geq 100mV$	100	170	250	ps
$t_{CHAN}$	Channel-to-Channel Skew	<b>Note 8</b>		3	15	ps
$t_{SKEW}$	Part-to-Part Skew	<b>Note 9</b>			100	ps
$t_{JITTER}$	Data Random Jitter (RJ) Deterministic Jitter (DJ)	<b>Note 10</b> <b>Note 11</b>			1 10	$\mu s_{RMS}$ $\mu s_{PP}$
	Clock Cycle-to-Cycle Jitter Total Jitter (TJ)	<b>Note 12</b> <b>Note 13</b>			1 10	$\mu s_{RMS}$ $\mu s_{PP}$
$t_r, t_f$	Output Rise/Fall Time	20% to 80% at full output swing	20	40	60	ps

**Notes:**

- High frequency AC electricals are guaranteed by design and characterization.
- Skew is measured between outputs of the same bank under identical transitions.
- Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
- RJ is measured with a K28.7 comma detect character pattern, measured at 10.7Gbps and 2.5Gbps/3.2Gbps.
- DJ is measured at 10.7Gbps and 2.5Gbps/3.2Gbps with both K28.5 and  $2^{23}-1$  PRBS pattern
- Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles,  $T_n - T_{n-1}$  where T is the time between rising edges of the output signal.
- Total jitter definition: With an ideal clock input of frequency  $\leq f_{MAX}$ , no more than one output edge in  $10^{12}$  output edges will deviate by more than the specified peak-to-peak jitter value.

### TIMING DIAGRAM



### SINGLE-ENDED AND DIFFERENTIAL SWINGS

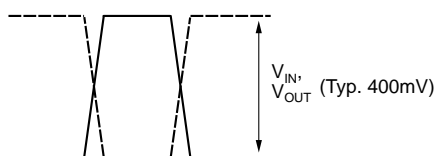


Figure 1a. Single-Ended Voltage Swing

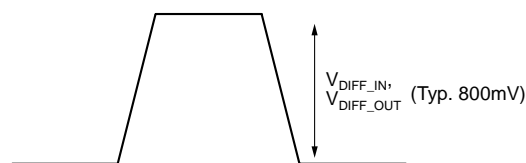
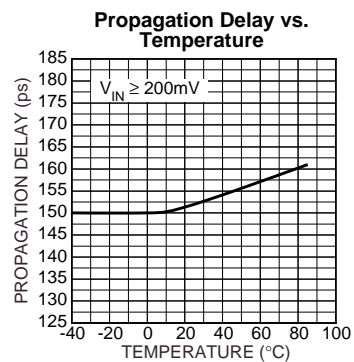
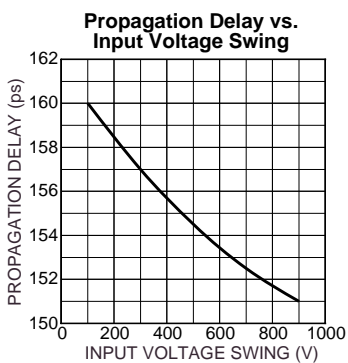
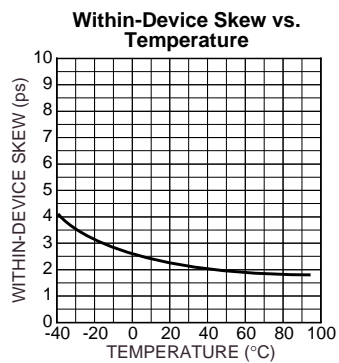
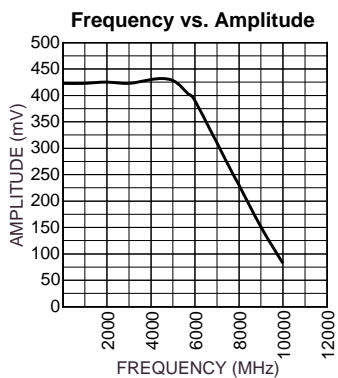


Figure 1b. Differential Voltage Swing

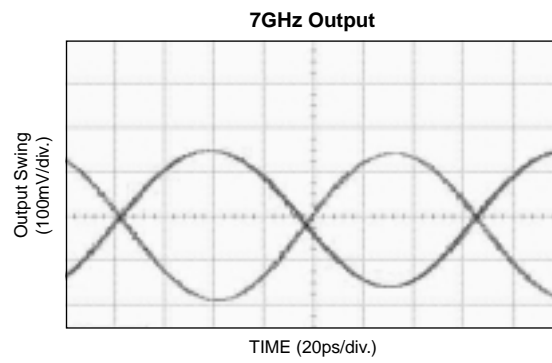
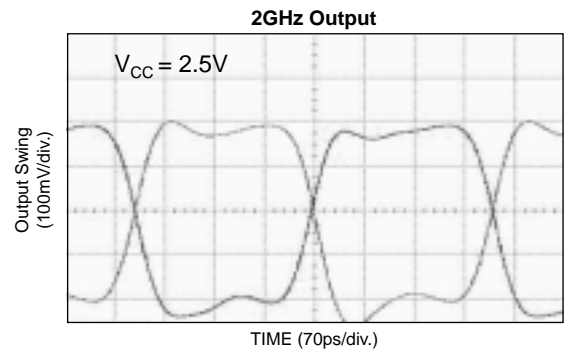
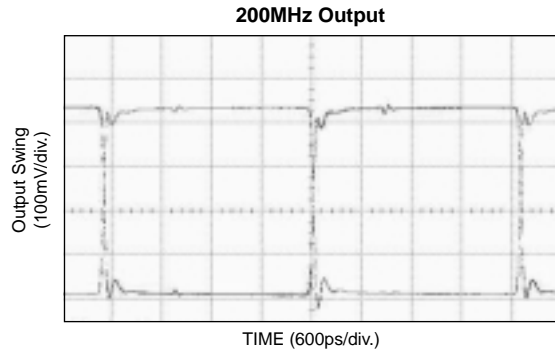
**TYPICAL OPERATING CHARACTERISTICS**

$V_{CC} = 3.3V$ ,  $GND = 0$ ,  $V_{IN} = 100mV$ ,  $T_A = 25^\circ C$ , unless otherwise stated.

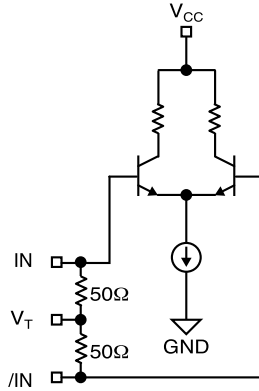


## FUNCTIONAL CHARACTERISTICS

$V_{CC} = 2.5V$ ,  $GND = 0$ ,  $V_{IN} = 100mV$ ,  $T_A = 25^\circ C$ , unless otherwise stated.

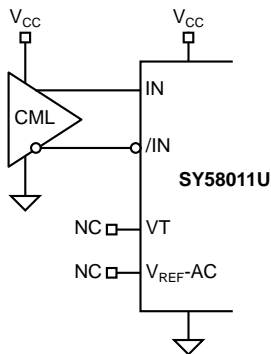


**INPUT STAGE**

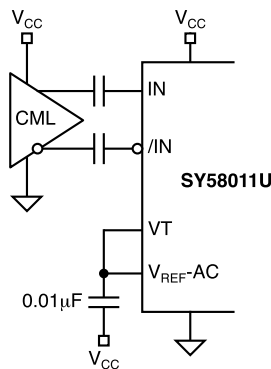


**Figure 2. Simplified Differential Input Buffer**

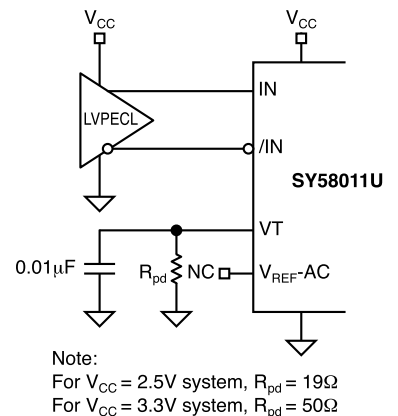
**INPUT INTERFACE APPLICATIONS**



**Figure 3a. DC-Coupled CML Input Interface**  
(option: may connect  $V_T$  to  $V_{CC}$ )

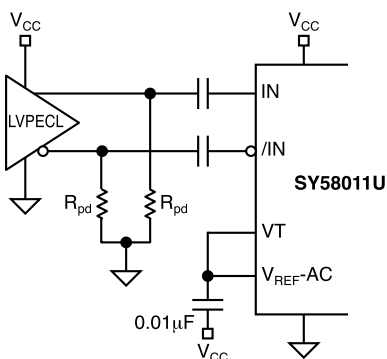


**Figure 3b. AC-Coupled CML Input Interface**



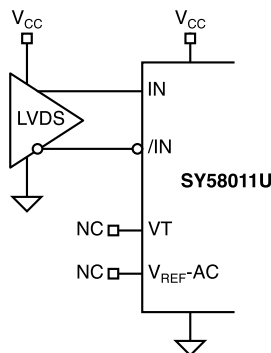
Note:  
For  $V_{CC} = 2.5V$  system,  $R_{pd} = 19\Omega$   
For  $V_{CC} = 3.3V$  system,  $R_{pd} = 50\Omega$

**Figure 3c. LVPECL Input Interface**



Note:  
 $R_{pd} = 100\Omega$  for a 3.3V system  
 $R_{pd} = 50\Omega$  for a 2.5V system

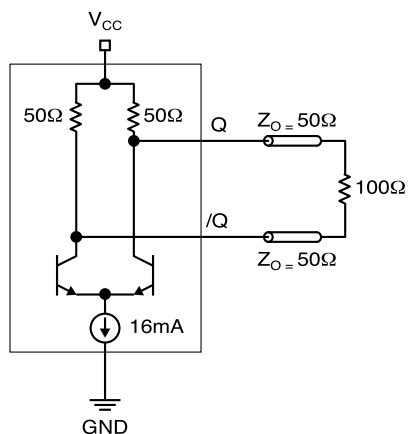
**Figure 3d. AC-Coupled LVPECL Input Interface**



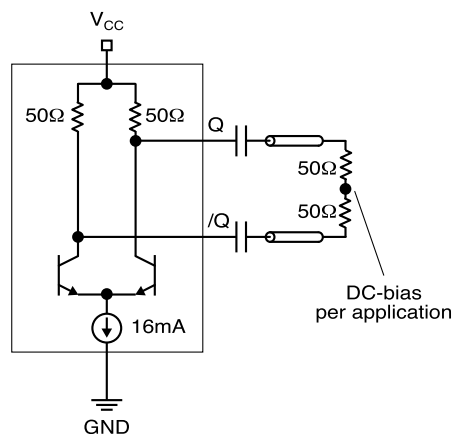
**Figure 3e. LVDS Input Interface**

## CML OUTPUT TERMINATION

Figure 4 and Figure 5 illustrates how to terminate a CML configuration. All outputs of the SY58011 are 50Ω with a 16mA current source.



**Figure 4. CML DC-Coupled Termination**



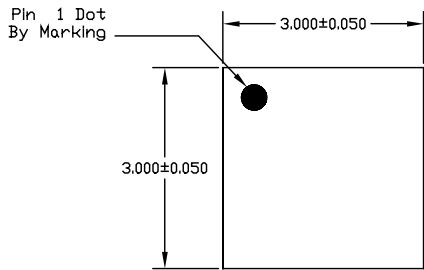
**Figure 5. CML AC-Coupled Termination**

## RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

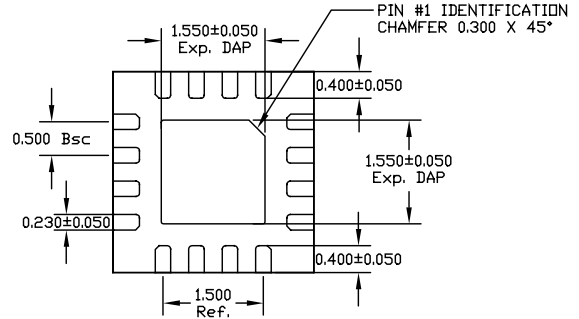
Part Number	Function	Data Sheet Link
SY58011U	7GHz, 1:2 CML Fanout Buffer/Translator with Internal I/O Termination	<a href="http://www.micrel.com/product-info/products/sy58011u.shtml">http://www.micrel.com/product-info/products/sy58011u.shtml</a>
SY58012U	5GHz, 1:2 LVPECL Fanout Buffer/Translator with Internal Input Termination	<a href="http://www.micrel.com/product-info/products/sy58012u.shtml">http://www.micrel.com/product-info/products/sy58012u.shtml</a>
SY58013U	6GHz, 1:2 Fanout Buffer/Translator with 400mV LVPECL Outputs and Internal Input Termination	<a href="http://www.micrel.com/product-info/products/sy58013u.shtml">http://www.micrel.com/product-info/products/sy58013u.shtml</a>
	16-MLF™ Manufacturing Guidelines Exposed Pad Application Note	<a href="http://www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf">www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf</a>
	HBW Solutions	<a href="http://www.micrel.com/product-info/as/solutions.shtml">http://www.micrel.com/product-info/as/solutions.shtml</a>



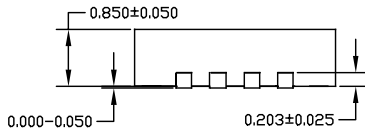
**16-PIN *MicroLeadFrame*<sup>®</sup> (MLF-16)**



TOP VIEW



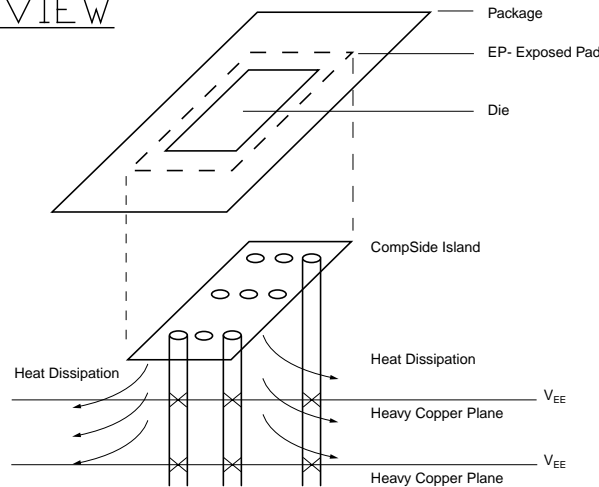
BOTTOM VIEW



SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



**PCB Thermal Consideration for 16-Pin MLF<sup>®</sup> Package  
(Always solder, or equivalent, the exposed pad to the PCB)**

**Package Notes:**

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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