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SSC 8830 PROSENSOR™

SENSOR TO MICROPROCESSOR A/D INTERFACE

PRELIMINARY INFORMATION

Features

- Interfaces Any of a Wide Range of Sensors, including Piezo-Electric and Piezo-Resistive Sensors, to a Standard Microprocessor
- Provides 5V Power Supply Regulation
- Low Current CMOS
- Choice of Two Adjustable Gain Ranges
- Accepts Single Ended or Differential Input
- Power Down Mode
- Low Battery Voltage Indication
- 16-Pin DIP or SOIC
- Usable With 3 Digit or 4 Digit Displays

Applications

- Accelerometers
- Pressure Transducers
- Strain Gauges
- Tire Pressure Displays
- Oil Pressure Sensing
- A/C Climate Control
- Low Cost/High Resolution A/D Converters for Microprocessors

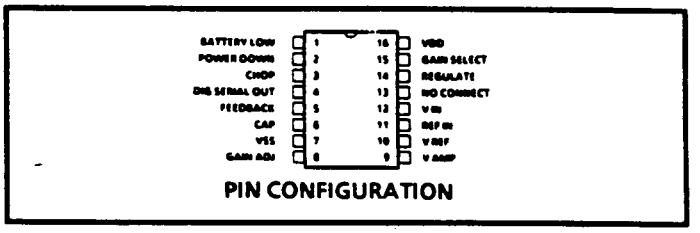
General Description

The SSC 8830 PROSENSOR™ Sensor to Microprocessor A/D Interface accepts a low voltage input from a sensing device, amplifies and digitizes it, and serially outputs a digital pulse stream to a processor or micro-controller.

The SSC 8830 PROSENSOR™ consists of a differential input, chopper stabilized amplifier with adjustable gain and a 5V regulator. The SSC 8830 PROSENSOR™ is fabricated using low power CMOS technology.

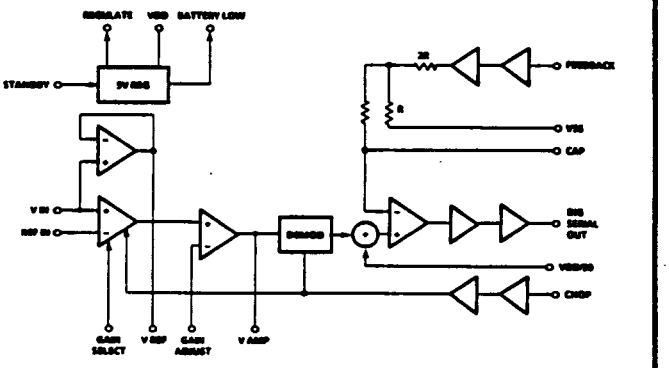
Functional Description

The SSC 8830 PROSENSOR™ accepts a differential or single ended low voltage input from a sensor at the V IN pin and multiplies it by a sampling frequency presented at the CHOP input. This amplitude modulation eliminates the amplifier offset as a source of error. (For single ended inputs the REF IN voltage may be adjusted to compensate for any offset in the sensor itself.)

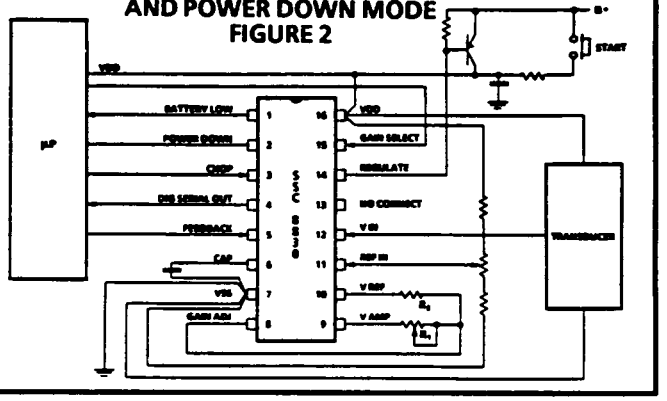


PIN CONFIGURATION

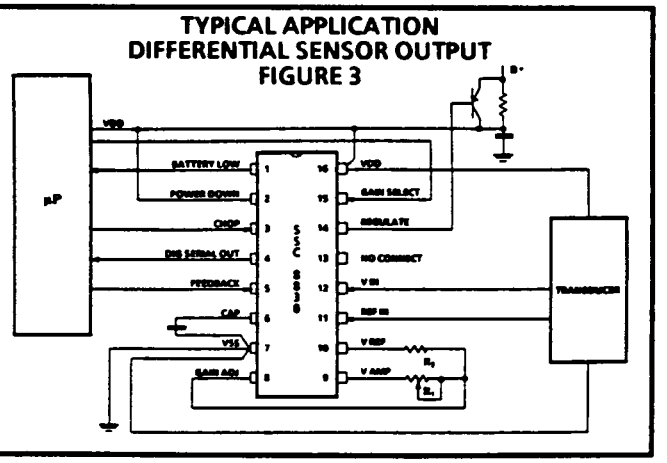
INTERNAL BLOCK DIAGRAM
FIGURE 1



TYPICAL APPLICATION
SINGLE ENDED SENSOR OUTPUT
AND POWER DOWN MODE
FIGURE 2



TYPICAL APPLICATION
DIFFERENTIAL SENSOR OUTPUT
FIGURE 3



Telephonics TLSI
An Instrument Systems Company

TLSI, Inc.
815 Broadhollow Road
Farmingdale, New York 11735
Phone: (516) 755-7005 • FAX: (516) 755-7626

The amplified input signal is then converted back to a dc voltage level and presented to a delta-sigma type analog-to-digital converter. A deliberate offset allows the input voltage range to include 0V. The resulting pulse stream is output to a processor or microcontroller via the DIGITAL SERIAL OUT pin.

The processor or microcontroller latches the pulse stream using the sampling clock that drives the CHOP input and returns the latched stream to the SSC 8830 PROSENSOR™ via the FEEDBACK pin. A low pass filter, composed of a resistor internal to the SSC 8830 and an external capacitor connected to the CAP pin, effectively integrates the pulse stream, converting it to a voltage level. The SSC 8830 then compares this voltage level to the amplified input signal V IN, closing the loop.

The processor or microcontroller measures sense voltage by counting the number of logic '1' pulses over a fixed period of time. Accuracies of up to 10 bits are achievable with appropriate decimators.

Accuracy and resolution are dependent on the decimation ratio, which is a function of the sampling frequency and the length of the software counter used to accumulate pulses. Using a simple counter decimator (sinc decimator) of count length n results in a resolution of 1 in n. Increasing counter length increases resolution and reduces data rate. Increasing sample frequency reduces accuracy and increases data rate.

$$\text{Data Rate} = \frac{\text{Sample Freq.}}{n}$$

Higher accuracies can be achieved using decimators that weight incoming pulses based on their relative position within the gate time. The use of such decimators also improves signal to noise ratio, thereby increasing the useful resolution.

Selecting and Adjusting Gain

The gain of the first of two internal amplifier stages may be selected via a logical input applied to the GAIN SELECT pin. A high level selects a gain setting of 70. A low level selects a gain setting of 1.

The gain of the second amplifier stage may be adjusted from 1 to 40 by varying the external resistor values R_1 and R_2 (Refer to Fig. 2) according to the following formula:

$$G = 1 + \frac{R_1}{R_2}$$

The combined gain of the 2 stages may be given as:

$$A = S\left(1 + \frac{R_1}{R_2}\right)$$

where S = 1 or 70, depending on the state of the GAIN SELECT pin.

Interpreting the Output

The DIGITAL SERIAL OUT pin outputs a serial pulse stream suitable for input to a digital circuit or microprocessor which functions as a decimator. The ratio of the number of clock periods that the DIGITAL SERIAL OUT signal is high to the total number of clock periods between readings is the pulse density. The pulse density at the DIGITAL SERIAL OUT pin varies linearly with the sensor voltage presented to the PROSENSOR™'s V IN pin.

Pulse density is determined as follows:

$$\frac{\text{Number of Pulses}}{n} = 3\left[A\left(\frac{V_{IN} - V_{REF}}{V_{DD}}\right) + \frac{1}{50}\right]$$

PIN NO.	SIGNAL NAME	DESCRIPTION
1	BATTERY LOW	A high level at this output indicates a low supply voltage condition.
2	POWER DOWN	A low level presented to this input causes the SSC 8830 PROSENSOR™ to open circuit the REGULATE output pin, removing the VDD supply voltage. If this mode is not used, the POWER DOWN pin must be connected to VDD.
3	CHOP	This input is the required clock to the modulator/demodulator and is used to stabilize the offset of the internal differential amplifier. Connect the microprocessor sample clock to this pin.
4	DIGITAL SERIAL OUT	This output presents a pulse stream to a processor or microcontroller. The ratio of the number of clock periods that this output is high to the total number of clock periods between readings (pulse density) varies linearly with the sensor voltage presented to the PROSENSOR™'s V IN pin.
5	FEEDBACK	The amplifier feedback connection from a processor or microcontroller is made via this input.
6	CAP	A capacitor is connected from this pin to VSS to integrate the pulse stream from the processor or microcontroller so that it can be compared to the amplified sensor voltage by the SSC 8830. Capacitor value is a function of sampling frequency.
7	VSS	Negative terminal of power supply.
8	GAIN ADJUST	The ratio of external resistors connected between this pin and pins 9 and 10 adjusts the gain of the second of two internal amplifier stages. The gain of this stage may be adjusted from 1 to 40. (See SELECTING AND ADJUSTING GAIN.)
9	V AMP	An external resistor (or variable resistor) R_1 is connected from this pin to pin 8. (See Fig. 2.)
10	V REF	An external resistor (or variable resistor) R_2 is connected from this pin to pin 8. (See Fig. 2.)
11	REF IN	This pin is the negative input terminal of the differential amplifier. One terminal of the differential output of the sensing device or transducer is connected to this pin. For sensing devices with a single ended output, the REF IN pin should be connected to a voltage that represents the quiescent dc level of the sensing device.
12	V IN	This pin is the positive input terminal of the differential amplifier. One terminal of the differential output of the sensing device or transducer is connected to this pin. For sensing devices with a single ended output, connect the output to this pin.
13	NO CONNECT	This pin is not used.
14	REGULATE	This output drives the base of a PNP transistor to regulate the voltage at the VDD pin. In POWER DOWN mode, the SCC 8830 open circuits the REGULATE output pin.
15	GAIN SELECT	The gain of the first of two internal amplifier stages may be selected via a logic level applied to this input. A high level selects a gain setting of 70. A low level selects a gain setting of 1.
16	VDD	This voltage is regulated to 5V (nominal) via an external PNP transistor connected to the REGULATE pin of the SSC 8830. The voltage at the VDD pin is also available to supply companion circuitry, including a microprocessor.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those limits which, if exceeded, may cause damage to the device. Proper operation is not implied at these limits. Voltages are referenced to V_{ss} unless otherwise indicated.

Supply Voltage	+16V
Positive Voltage at any pin EXCEPT REGULATE, with respect to V_{ss}	V_{DD} + 0.3V
Positive Voltage at REGULATE pin, with respect to V_{ss}	+18V
Negative Voltage at any pin, with respect to V_{ss}	−0.3V
Input Current on any pin	±10 mA
Power Dissipation	500 mW
Storage Temperature	−65 °C to +150 °C
Lead Temperature (Soldering, 10 sec.)	245 °C

OPERATING CONDITIONS

Unregulated Supply Voltage, B+	+5.2V to +16.0V
Operating Temperature	−40 °C to +85 °C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, $T_{ambient}$ = −40°C to +85 °C, B+ = 5.2V to 16V

ANALOG

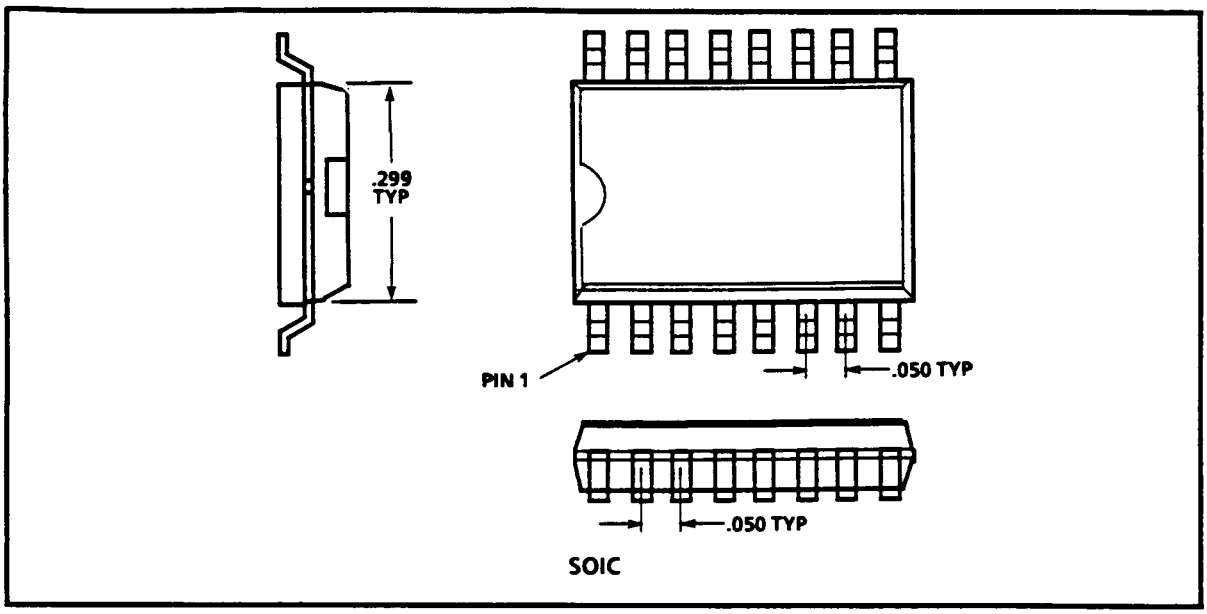
PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Common Mode Input Voltage	2		3	V	
Maximum Input Voltage, V_{IN} Pin		1.5		V	V_{DD} = 5V
Input Impedance, V_{IN} Pin	0.1	10		MOhm	
Output Current, V_{REF} Pin			0.5	mA	

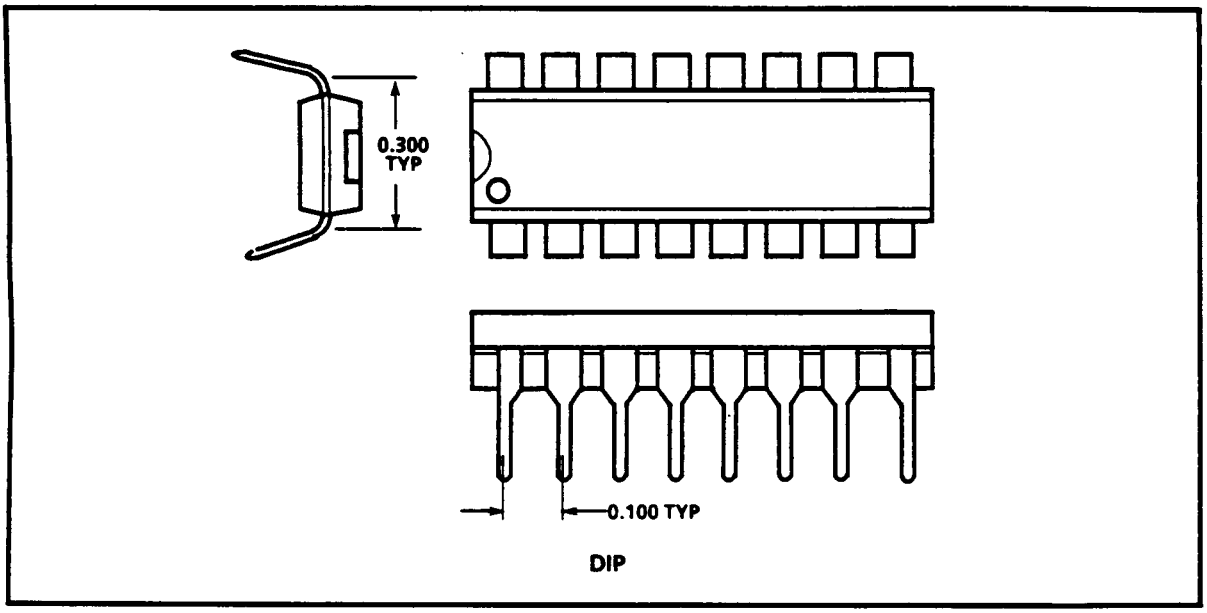
DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Unregulated Supply Voltage, B+	4.5		16.0	V	
Supply Current, I_{DD}		1.0	2.0	mA	V_{IN} = 0V
Regulated Supply Voltage, V_{DD}	4.0	5.0	6.0	V	
Sink Current, REGULATE Pin	5.0			mA	In circuit of Fig. 2.
Output Voltage, Digital Outputs					
V_{OH}	2.4			V	R_L = 10K; C_L = 75 pF.
V_{OL}			0.4	V	R_L = 10K; C_L = 75 pF.
Input Voltage, Digital Inputs					
V_{IH}	2.0			V	
V_{IL}			0.8	V	
Input Leakage Current (I_{LL}), CHOP			±1	µA	
Integrator Resistance		400		kOhm	@ 25 °C

AC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Sampling Frequency, CHOP	500		5000	Hz	





SSC 8830 PACKAGE CONFIGURATIONS

TLSI, Inc.
815 Broadhollow Road
Farmingdale, New York 11735
Phone: (516) 755-7005 • Fax: (516) 755-7626

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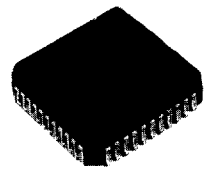
PACKAGES



DUAL IN-LINE PACKAGES (DIP)

PLASTIC DIP	8 through 24 (300 mil); 24 through 48 (600 mil); 64 (900 mil)
CERAMIC DIP, SIDE BRAZED	8 through 24 (300 mil); 24 through 48 (600 mil); 64 (900 mil)
CERDIP	8 through 24 (300 mil); 24 through 48 (600 mil)

SURFACE MOUNT PACKAGES

SOIC	8 through 16 (150 mil); 16 through 28 (300 mil)
PLCC	20 through 84
QUAD FLAT PACK	44 through 208
BUMPERED QFP	100 and up
CHIP CARRIER (LCC)	18 through 68
CERAMIC QFP	44 through 160 (EIJ); 132 through 164 (JEDEC)
CERFLAT	14 through 28
CERQUAD	20 through 68

PIN GRID ARRAYS

PLASTIC PGA	28 through 244
PGA	28 through 244

This is a partial list; consult factory for availability of other packages.
NOTE: Devices are available in anti-static tubes or trays, on tape & reel, or in die form.