1.0 INTRODUCTION TO OTI-053 DMA AND MEMORY CONTROLLER

OTI-053 integrates all the functions of a DMA controller and memory controller.

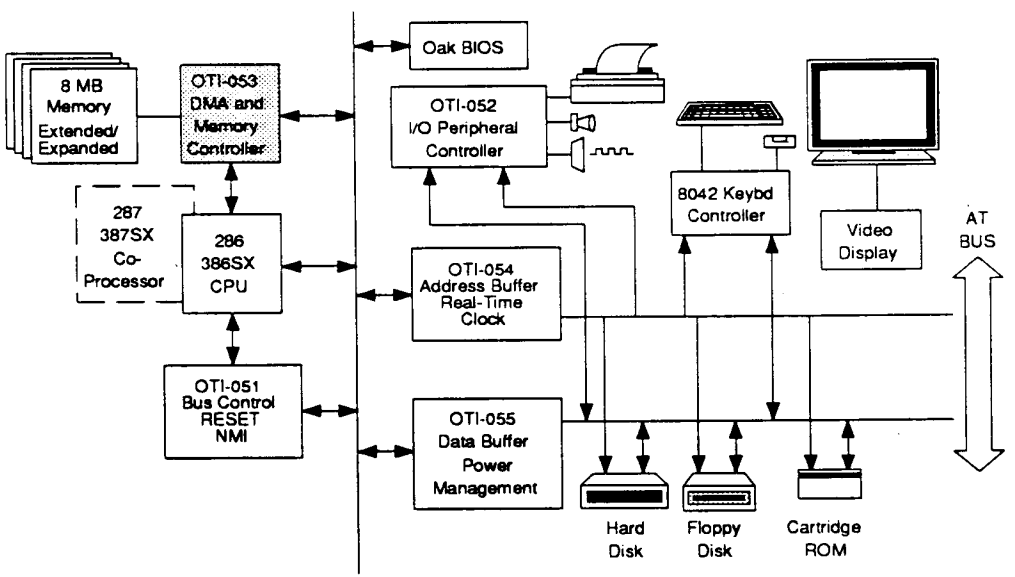
A summary of the special features provided by OTI-053 is listed below:

Memory Control:
- page mode and interleave mode for zero wait state cycles
- supports 60ns up to 120ns DRAMs
- system speed up to 20 MHz
- programmable wait states for slower speed DRAMs
- zero wait state ROM cycle with shadow RAM
- EMS 4.0
- supports 640 KB of system memory up to 8MB of total on-board memory including extended/expanded memory.
- supports 256K and 1M type DRAMs
- supports pseudo-SRAM for laptop model
- cartridge ROM support

DMA Control:
- supports fast and normal DMA mode with embedded 8237 at up to 10 MHz

Laptop Support:
- power saving scheme

System Block Diagram



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2.0 PIN-OUT ASSIGNMENT

Table 1. OTI-053 Pin Description

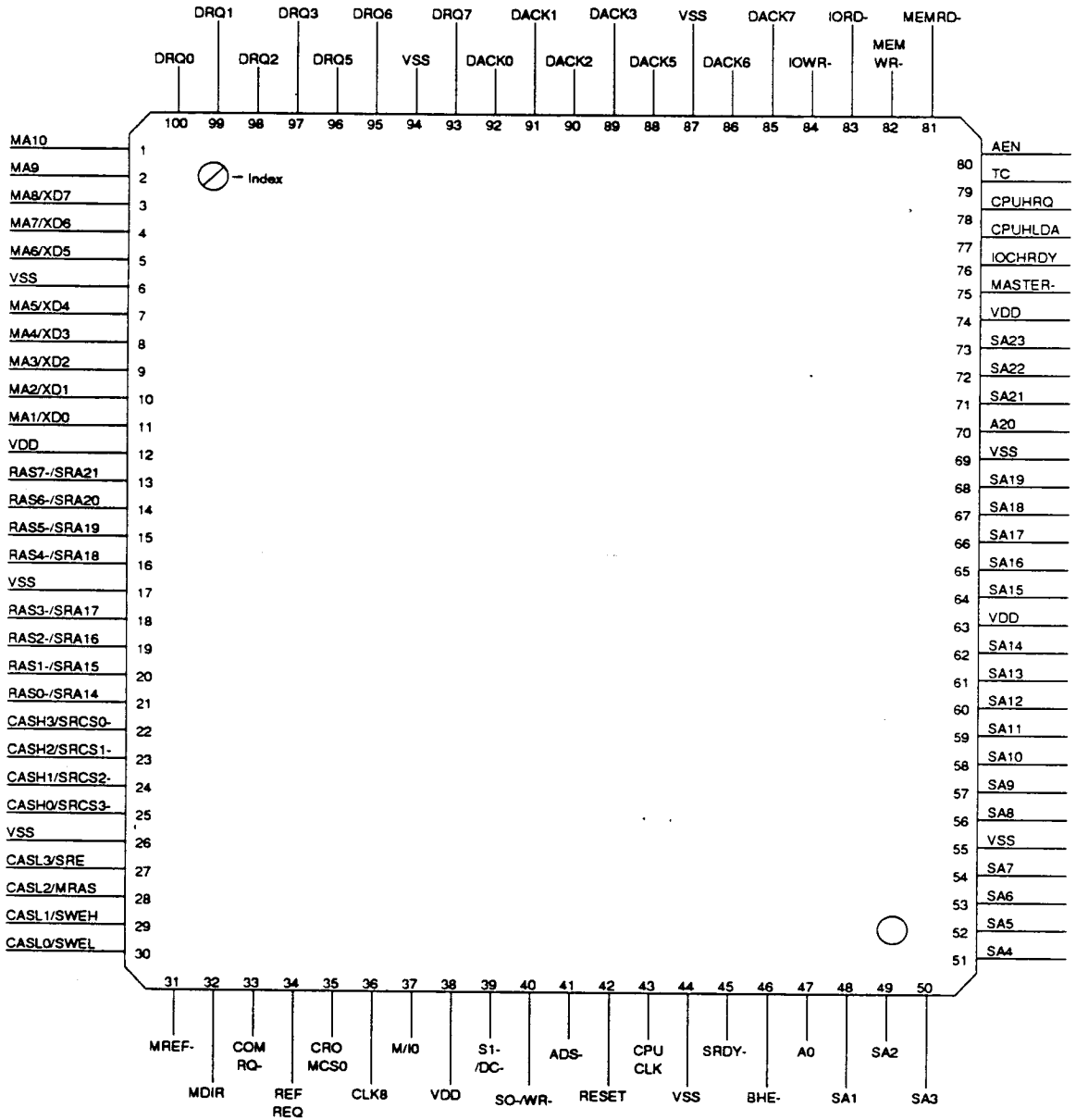
SYMBOL	PIN #	TYPE	NAME and FUNCTION
			***** SYSTEM INTERFACE *****
SA1-SA19 SA21-23	48-54,56-62,64-68 71-73	I/O	ADDRESS LINE (1-19,21-23): SA21-SA23 are the CPU address lines (unlatch).
A0	47	I/O	ADDRESS LINE 0: address line from OTI-051.
A20	70	I/O	ADDRESS LINE 20: address line 20 from OTI-051 gated by 8042 output and port 92(Hex) output.
S0-/WR- S1-/DC-	40 39	I	BUS CYCLE STATUS: These signals together with M/IO and COD/INTA- are used to decode different bus cycles.
M/IO-	37	I	MEMORY OR I/O CYCLE: is an input signal from the CPU indicating whether the present cycle is memory or I/O access.
SRDY-	45	I/O	SYSTEM READY: is an active low signal to acknowledge the CPU that the data transfer for system memory is complete.
BHE-	46	I/O	BYTE HIGH ENABLE: is an active low signal used to enable data onto the most significant half of the data bus (D15 - D8). It is an input line when the CPU is in control. OTI-051 starts driving this signal during the DMA and refresh time.
ADS-	41	I	ADDRESS STROBE: is an active low signal coming from 80386SX. This pin is also used to detect whether an 80286 or 80386SX is used.
CPUCLK	43	I	CPU CLOCK: is a 50% duty cycle input clock.
RESET	42	I	RESET: is an active high signal synchronized to the system clock to reset the system.
			***** DMA INTERFACE *****
DRQ0-3 DRQ5-7	100-97 96,95,93	I	DMA REQUEST (0-3,5-7): are asynchronous active high signal channel request inputs used by peripheral devices to obtain DMA service. DACK will acknowledge the recognition of a DRQ signal. These signals are compatible to the DRQ signals of 8237.
DACK0-3 DACK5-7	92-89 88,86,85	O	DMA ACKNOWLEDGE: are active low signals to notify the individual peripherals when one has been granted a DMA cycle. These signals are compatible to the DACK signals of 8237.
TC	79	O	TERMINAL COUNT: is an active high output pulse signal when the terminal count for any DMA channel is reached.
AEN	80	O	ADDRESS ENABLE: is an active high signal during the DMA cycle to degate the I/O devices from the I/O channel to allow DMA transfers to take place.
CPUHRQ	78	O	HOLD REQUEST: is an active high signal connected directly to HOLD of the CPU. This signal is used by the chip to request the bus from the CPU.
CPUHLDA	77	I	HOLD ACKNOWLEDGE: is an active high signal connected directly to HLDA of the CPU. This signal is used by the chip to determine if the bus request has been granted by the CPU.

Table 1. OTI-053 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
IOCHRDY	76	I	I/O CHANNEL READY: is an active high ready signal from an I/O channel. It is pulled low in active by a memory or I/O device to lengthen memory or I/O cycles. For every system clock cycle this signal is inactive, one wait state is added.
MASTER-	75	I	MASTER: this signal is used together with a DRQ line to gain control of the system.
IORD-	83	I/O	I/O READ COMMAND: active low command to instruct an I/O device to drive its data onto the data bus. This pin becomes an input during the MASTER mode.
IOWR-	84	I/O	I/O WRITE COMMAND: active low command to instruct the I/O device to read the data present on the data bus. This pin becomes an input during the MASTER mode.
MEMRD-	81	I/O	MEMORY READ COMMAND: active low signal to instruct the memory subsystem to drive its data onto the data bus. This pin becomes an input during the MASTER mode.
MEMWR-	82	I/O	MEMORY WRITE COMMAND: active low signal to instruct the memory subsystem to store the data present on the data bus. This pin becomes an input during the MASTER mode.
			***** MEMORY INTERFACE *****
REFREQ	34	I	MEMORY REFRESH REQUEST: is the memory request signal from 8253 Timer channel 1 which comes from OTI-052.
COMRQ-	33	I/O	COMMAND REQUEST: active low bidirectional signal. In the input phase, it receives a signal from OTI-051 indicating when to wake up from the SHUTDOWN mode. In the output phase, it requests the OTI-051 to generate the PC memory cycle. The signal is in the input phase when AEN is HIGH, and it is in the output phase during other times.
MREF-	31	I/O	MEMORY REFRESH: is an active low signal indicating that a refresh cycle is going on. It is forced low when D/SRAM- is low to enable the self-refresh feature of the pseudo-static RAM during the SHUTDOWN mode.
CLK8	36	I	8 MHZ CLOCK: is an 8 MHz 50% duty cycle clock input to the RAS pulse width counter as well as the memory refresh counter.
MDIR	32	O	MEMORY DIRECTION: is the status signal to memory write enable of memory devices and also the data direction transceiver between the CPU and system memory bus: MDIR = high ==> memory read MDIR = low ==> memory write MDIR is normally high. It becomes low when: 1. Non-DMA, system memory write cycle. 2. Non-DMA, CROM cycle. 3. DMA, system memory write cycle.
MA(1-10)	11-7,5-1	I/O	MEMORY ADDRESS (1-10): During memory cycles, it is a time multiplexed memory address bus for 1 M memory type (for 256K memory type MA(10) is not used). During the memory cycle, MA(1-10) is the row address output until 1 unit time delay has elapsed, and then the MA(1-10) starts outputting the column address. MA1-8 is multiplexed with XDATA during I/O cycles.
/XD7 - XD0	3-5,7-11	I/O	XDATA BUS: bi-directional data lines to/from the I/O channel bus. It is multiplexed with MA8-1 during I/O cycles.

Table 1. OTI-053 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
RAS0- - RAS7-	21-18,16-13	O	ROW ADDRESS STROBE (0 - 7): If D/SRAM- is high, they are active low control signals to the DRAM system memory to inform that a row address is present on the address bus. RAS0 and RAS1 are for the first memory bank, RAS2 and RAS3 are for the 2nd bank, RAS4 and RAS5 are for the third bank and RAS6 and RAS7 are for the last bank.
/SRA(14 - 17)	21-18	O	SRAM ADDRESS (14 - 17): If D/SRAM- is low, they are the four most significant addresses of the 128K x 8 pseudo-SRAM. SRA(14-17) are multiplexed with RAS(0-3)- using D/SRAM- as select.
/SRA(18 - 21)	16-13	O	SRAM ADDRESS (18 - 21): If D/SRAM- is low, they are inputs to the pseudo- SRAM address decoder for the Expanded/Extended Memory option. The combinations of SRA(18 - 21) are capable of selecting 128K x 8 pseudo-SRAM organized word wide for a total of 4M minus 256KB. Expanded/extended memory is not selected if SRA(18 - 21) are 1111. SRA(18-21) are multiplexed with RAS(4-7)- using D/SRAM- as select.
CASH3-0- CASL3-0-	22-25,27-30	O	COLUMN ADDRESS STROBE (High and Low): If D/SRAM- is high, they are active low control signals to the on-board DRAM system to inform that a column address is present on the address bus: - CASH- for odd byte [D(15-8)]. - CASL- for even byte [D(7-0)].
/SRCS(0 - 3)-	22-25	O	STATIC RAM CHIP SELECT (0 - 3): If D/SRAM- is low, these are the pseudo-Static RAM Memory Chip Selects (active low signals). SRCS(0-3)- are multiplexed with CASH3-0 using D/SRAM- as select. Each signal selects 2 banks of 128K x 8 type pseudo-SRAM for a total of 1MB of memory: **SIGNAL** **MEMORY SPACE** SRCS0- 00000 - 7FFFF(even word) SRCS1- 00000 - 7FFFF(odd word) SRCS2- 80000 - FFFFF(even word) SRCS3- 80000 - FFFFF(odd word)
/SRE-	27	O	SRAM READ ENABLE: If D/SRAM- is low, it is an active low read enable signal for SRAM memory. SRE- is multiplexed with CASL3- using D/SRAM- as select.
/MRAS-	28	O	STATIC RAM TIMING: IF D/SRAM- is low, it is an active low signal used for SRAM memory timing. MRAS- is multiplexed with CASL2- using D/SRAM- as select.
/SWEH- SWEL-	29-30	O	SRAM WRITE ENABLE (high and low): If D/SRAM- is low, they are active low write enable signals for SRAM: - SWEH- for odd byte. - SWEL- for even byte. SWEH- and SWEL- are multiplexed with CASL1- and CASL0- using D/SRAM- as select.
CROMCS-	35	O	CARTRIDGE ROM CHIP SELECT: is an active low signal used to enable the CARTRIDGE ROM to output data on to the data bus.
VDD	12,38,63,74		POWER: +5 V supply, 4 pins
VSS	6,17,26,44, 55,69,87,94		GROUND: 8 pins



3.0 OTI-053 FUNCTIONAL DESCRIPTION

OTI-053 functions can be categorized as follows:

1. Memory Control Unit
2. DMA Control
3. Arbiter and Refresh Control
4. Miscellaneous

3.1 Memory Control Unit

OTI-053 offers either a Dynamic or Pseudo-Static RAM memory control unit depending on the D/SRAM- input signal in OTI-055. If the D/SRAM- input is not available, then the system defaults to dynamic memory support.

- If D/SRAM- is strapped high (to VCC), OTI-053 will exercise on-board DRAM memory control. It supports 640KB of system memory plus another 384KB for shadow RAM implementation, EMS or remapped to above the 1M address space. OTI-053 supports full specification of EMS 4.0 which makes multitasking possible. The chip supports both 256K and 1M type memories. The memory size can vary from a minimum of 1 MB to a maximum of 8 MB.

- If D/SRAM- is strapped low (to GROUND), OTI-053 will exercise on-board pseudo-SRAM memory control. It supports 640KB of system memory and 384K of EMS memory using 128K x 8 type of pseudo-SRAM. It also supports pseudo-SRAM up to 4M minus 256KB of 128K x 8 type of memory for memory addresses above the 1M boundary. It provides 4 bit address select [SRA(18 - 21)] that can select 1 out of 16 banks of memory (256KB each). However, if EMS SRAM is not accessed, SRA(18 - 21) will be all 1's. Hence, only 15 possible ways are used. The decoding has to be done external to the chip on the mother board.

The function of Memory Control Units can be broken down to 5 sub-blocks:

1. System Memory Control
2. EMS Control
3. Memory Request Control
4. Memory Parity
5. Memory Address Generator

3.1.1 System Memory Control

3.1.1.1 System ROM Area

Two ROM address spaces are implemented:

0E0000 - 0FFFFF (128K)
FE0000 - FFFFFF (128K)

Physical ROM area is only 128KBytes, therefore both address spaces address the same physical ROM. Shadow RAM implementation is adopted for zero wait state operation. Shadow RAM address space covers:

0C0000 - 0CFFFF (video ROM area) (4 segments)
0D0000 - 0DFFFF (PC bus external device ROM area)
0E0000 - 0EFFFF (Model 30 - 286 BIOS area or EMS area)
0F0000 - 0FFFFF (Model 30 - 286 BIOS area)

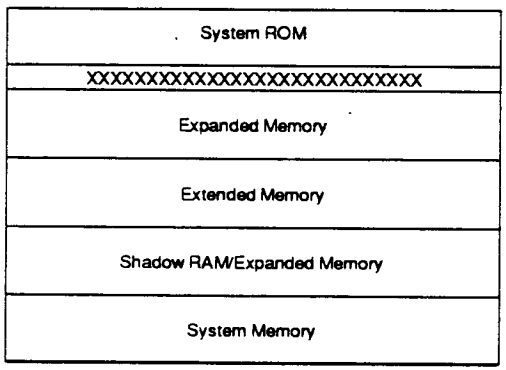
Indexed ports 18 & 19(Hex) can be programmed to indicate to the system whether the memory space is used for shadow RAM implementation. If the address space is not used, then it can be used as expanded memory or mapped to 1M through 1.384M address space. Protection circuitry on-chip can prevent writing to the shadow RAM area after the RAM content is loaded. The shadow RAM area is write enabled after power-up.

The sequence of loading after power-up is listed below:

1. ROM read cycles to download contents from ROM to shadow RAM area (wait states for slow ROM access time).
2. Disable access to physical ROM, enable shadow RAM write protection circuitry for ROM BIOS. Only RAM READ cycles are generated afterward.
3. Download video ROM content to shadow RAM.
4. Disable access to physical ROM, enable shadow RAM write-protection circuitry. Only RAM READ cycles are generated for the address space.

3.1.1.2 System Memory Map

Tabel 2. System Memory Map



RAS, CAS are generated for the 640K system memory space if they are enabled by the system board memory enable register. PC cycles are generated if the memory space is disabled through the SYSTEM BOARD MEMORY ENABLE register.

0F0000 - 0FFFFF	ROM READ and RAM WRITE cycle during initialization, RAM READ only after it is write-protected
0E0000 - 0EFFFF	ROM READ and RAM WRITE cycle during initialization, RAM READ only after it is write-protected. If it is not used as shadow ROM, PC cycles are generated to the PC bus. If it is used as shadow ROM, none of the EMS registers should be mapped to this area.
0D0000 - 0DFFFF 0C0000 - 0CFFFF	PC cycles generated during initialization, RAM READ only after it is write-protected. If it is used as shadow ROM, no EMS register should be mapped to this area. PC cycles are generated if it is not used as shadow ROM.

If neither Shadow RAM nor EMS is used, the physical memory between 0A0000(Hex) to 0FFFFF(Hex) can be mapped to the address space 1M to 1.384M through the POS register or indexed port 1A(Hex).

3.1.1.3 Shadow RAM Control Registers

Shadow RAM Control Register 0: I/O Port Index 0018(Hex) R/W:

Bit	Function
7	DIS/EN- WRITE TO SHADOW RAM, C0000-C3FFF
6	DIS/EN- WRITE TO SHADOW RAM, C4000-C7FFF
5	DIS/EN- WRITE TO SHADOW RAM, C8000-CBFFF
4	DIS/EN-WRITE TO SHADOW RAM, CC000-CFFFF
3	EN/DIS- SHADOW RAM, C0000-C3FFF
2	EN/DIS- SHADOW RAM, C4000-C7FFF
1	EN/DIS-SHADOW RAM, C8000-CBFFF
0	EN/DIS-SHADOW RAM, CC000-CFFFF

At Power On or Reset, the content of Shadow RAM Control Register 0 is 00.

Shadow RAM Control Register 1:I/O Port Index 0019(Hex) R/W:

Bit	Function
7	Not used
6	DIS/EN- WRITE TO SHADOW RAM, D0000-DFFFF
5	DIS/EN- WRITE TO SHADOW RAM, E0000-EFFFF
4	DIS/EN- WRITE TO SHADOW RAM, F0000-FFFFF
3	Not used
2	EN/DIS- SHADOW RAM, D0000-DFFFF
1	EN/DIS- SHADOW RAM, E0000-EFFFF
0	EN/DIS- SHADOW RAM, F0000-FFFFF

At Power On or Reset, the content of Shadow RAM Control Register 1 is 00.

3.1.1.4 System Memory Configurations

The 640K of system memory can be disabled individually in 128K blocks. At power-up, if certain memory is determined to be bad by POST, or if I/O memory is detected in any of the 5 blocks, POST will automatically disable that particular memory block by writing to System Board Memory Enable Register (port 104(Hex)).

System Board Memory Enable Register: I/O Port 0104 (Hex) R/W:

Bit	Function	
7-5	Not used	
4	Enable/Disable- 5th Bank	080000-09FFFF
3	Enable/Disable- 4th Bank	060000-07FFFF
2	Enable/Disable- 3rd Bank	040000-05FFFF
1	Enable/Disable- 2nd Bank	020000-03FFFF
0	Enable/Disable- 1st Bank	000000-01FFFF

At Power On or Reset, the content of port 104(Hex) is 1F(Hex).

OTI-053 supports both 256K type and 1M type DRAMs. In order to extract the highest performance out of the memory system, both page mode and interleave mode memory accessing techniques are implemented.

Maximum page size for 256K DRAM is 512 x 2bytes = 1 KBytes, and 1K x 2 Bytes = 2 KBytes for 1M type DRAM. Interleaving is done at page boundaries, which could increase the page size by 2.

Two-way Interleaved Memory: between BANK 0 and 1 or BANK 2 and 3

BANK 0	BANK 1
Page 0	Page 1
Page 2	Page 3
.	.
.	.
.	.

Four-way Interleaved Memory:

BANK 0	BANK 1	BANK 2	BANK 3
Page 0	Page 1	Page 2	Page 3
Page 4	Page 5	Page 6	Page 7
.	.	.	.
.	.	.	.

Since interleaving is done at the page boundary, it is unlikely that a program executing in the page could exceed the page boundary of 1KB or 2KB. With two-way interleaved memory, it is not likely that consecutive memory access will be from a different page on the same bank. Interleaving at the page boundary is better than interleaving at even and odd bytes, in which case there will be a problem if consecutive memory access is on even bytes alone (e.g. access an array with all even indices).

Table 3.1. Total Memory Size Versus Memory Type (DRAM Page Mode)

Memory Size	BANK 0	BANK 1	BANK 2	BANK 3	
1M	256K-RAS0,1	0	0	0	no interleave
1M	256K-RAS0	256K-RAS2	0	0	2-way interleave
2M	256K-RAS0,1	256K-RAS2,3	0	0	2-way interleave
2M	256K-RAS0	256K-RAS2	256K-RAS4	256K-RAS6	4-way interleave
2M	1M-RAS0	0	0	0	no interleave
3M	256K-RAS0,1	0	1M-RAS4	0	no interleave
3M	256K-RAS0	256K-RAS2	1M-RAS4	0	2-way interleave, banks 0, 1
3M	256K-RAS0,1	256K-RAS2,3	256K-RAS4,5	0	2-way interleave, banks 0, 1
3M	256K-RAS0,1	256K-RAS2,3	256K-RAS4	256K-RAS6	2 x 2-way interleave
4M	256K-RAS0,1	256K-RAS2,3	256K-RAS4,5	256K-RAS6,7	4-way interleave
4M	1M-RAS0	1M-RAS2	0	0	2-way interleave
5M	256K-RAS0,1	0	1M-RAS4	1M-RAS6	2-way interleave, banks 2, 3
5M	256K-RAS0	256K-RAS2	1M-RAS4	1M-RAS6	2 x 2-way interleave
5M	1M-RAS0	1M-RAS2	256K-RAS4	256K-RAS6	2 x 2-way interleave
5M	1M-RAS0	1M-RAS2	256K-RAS4,5		2-way interleave, banks 0, 1
6M	256K-RAS0,1	256K-RAS2,3	1M-RAS4	1M-RAS6	2 x 2-way interleave
6M	1M-RAS0	1M-RAS2	256K-RAS4,5	256K-RAS6,7	2 x 2-way interleave
8M	1M-RAS0	1M-RAS2	1M-RAS4	1M-RAS6	4-way interleave

In DRAM Page Mode, RAS0, RAS2, RAS4, RAS6 are to be used for both 256K type or 1M type DRAMs. RAS1, RAS3, RAS5, RAS7 are only to be used with 256K type of DRAMs. OTI-053 supports up to 8MB of memory including system memory, shadow RAM, extended memory and expanded memory.

Table 3.2. Total Memory Size Versus Memory Type (DRAM No Page Mode)

Memory Size	BANK 0	BANK 1	BANK 2	BANK 3	
1M	256K-RAS0	256K-RAS2	0	0	
2M	256K-RAS0,1	256K-RAS2,3	0	0	
4M	256K-RAS0,1	256K-RAS2,3	256K-RAS4,5	256K-RAS6,7	
2M	1M-RAS0	0	0	0	
4M	1M-RAS0	1M-RAS2	0	0	interleave
6M	1M-RAS0	1M-RAS2	1M-RAS4		
8M	1M-RAS0	1M-RAS2	1M-RAS4	1M-RAS6	interleave

In No Page Mode DRAM, memory of different types cannot be mixed as in normal Page Mode DRAM. When used with 256K DRAM, interleave has to be programmed. When used with 1M DRAM, both interleaving and non-interleaving are possible.

3.1.1.5 RAS Pulse Width Counter

There is a limitation to the number of consecutive DRAM cycles. The RAS pulse width cannot exceed a certain spec (10,000ns, 30,000ns or 100,000ns). A register is provided for the user to set the spec. A counter counts the number of consecutive memory accesses to the same page and would raise the RAS if the maximum count is exceeded. Wait states would be inserted to accommodate the RAS precharge time, and the next memory access can then continue with the counter being reset to zero.

3.1.1.5 Memory Timing Scheme

The default timing would be 0 wait state during page hit and 2 wait states during page miss and one wait state for the start of the first memory access from other cycles. This default timing would support 120ns DRAMs running at 8 MHz system speed. User programmability (indexed port 11(Hex)) is added so that the user can increase the number of wait states if he is using slower speed memories or running at a higher system speed.

Table 4. Wait States versus Memory Speed

DRAM SPEED	SYSTEM SPEED (MHZ)				
	8	10	12.5	16	20
120NS	1/0/2	1/0/2	1/0/2	2/0/3*	-
100NS	1/0/2	1/0/2	1/0/2	2/0/3*	2/0/3*
80NS	1/0/2	1/0/2	1/0/2	1/0/2	2/0/3
60NS	no page	no page	no page	no page	1/0/2

wait state at 1st access / wait state for page hit / wait state for page miss

* 2/1/3 may be required for slow DRAMs.

During no page mode, memory system is running at zero wait state for memory read and 1 wait state for memory write.

PSEUDO SRAM SPEED	SYSTEM SPEED (MHZ)				
	8	10	12.5	16	20
120NS	1/0	1/0	1/0	2/1	2/1
100NS	no wait	1/0	1/0	2/1	2/1

w.s. on CE- pulse width / w.s. on CE- precharge

3.1.1.6 Pseudo-SRAM Control

The system memory control generates 4 SRAM chip selects [SRCS(0 - 3)-] and read/write control signals (SRE-, SWEH-, SWEL-):

SIGNAL	MEMORY SPACE
SRCS0 -	00000 - 7FFFF(even word)
SRCS1 -	00000 - 7FFFF(odd word)
SRCS2 -	80000 - FFFFF(even word)
SRCS3 -	80000 - FFFFF(odd word)

Address lines SRA(14-17) are the most significant bits for the 128k x 8 pseudo-static RAM. Address lines SRA(18-21) are used to decode the additional 4M - 256KB of expanded/extended memory. External decoding logic is required. SRA(18-21) is qualified with MRAS- in the external decoder. The SRCS- lines should be connected to the OE- signal of the pseudo-static RAMs. The user can select either a one wait state operation or a two wait state operation by programming indexed port 1B(Hex) to the appropriate value. During power-down mode, MREF- will stay at low all the time to start the SELF-REFRESH mode of the pseudo-static RAM. MREF- should be tied to the /RFSH signal of the pseudo-SRAM.

The default memory type is DRAM. Pseudo-SRAM mode is selected by programming 0 to bit 4 on index port 1E.

3.1.2 EMS 4.0 and Cartridge ROM Control

EMS Control consists of EMS Current Map, EMS Alternate Map and EMS memory parity check and parity generator.

Current and Alternate Maps are 60 words by 10-bit register files each, containing enable bit and the physical address 22 to 14 of the EMS memory: MAP(0:9). The memory space is logically broken down into 64 pages of 16KB each. However, the ROM BIOS area (F0000 - FFFFF) is reserved and is not mappable to the EMS memory. Each block of 16KB size can be mapped to one of any of n blocks of EMS memory based on the content of the EMS Memory Map (if D/SRAM- is high, n = 128 for 256K memory type, n = 512 for 1M memory type; if D/SRAM- is low, n = 60). During the memory access, the LA(14-19) is used to select the content of the Current and Alternate Map. Cartridge ROM is supported through the EMS mapping scheme. When EMS is disabled and CROM is enabled, CROMCS- would be generated to select the cartridge ROM. The EMS mapper would also output the corresponding high order ROM address for the cartridge ROM.

3.1.3 Memory Request Control

Memory Request Control generates the internal RAS- timing control signal. Every memory cycle at system or EMS memory will follow this as a basic timing. There are 3 sources of timing to determine the RAS cycle:

During the CPU memory access, RAS- starts in the middle or at the end of TS and ends at the end of TC. CAS- signals are generated 1 to 1 1/2 clocks after RAS- if it is a memory read cycle, and 2 system clocks after RAS- if it is a memory write cycle.

During the DMA transfer, RAS- follows the memory read or memory write commands (MRD- or MWR-) that are synchronized to the system clock. CAS- signals are generated 2/3 clocks after RAS- if it is a memory read cycle, and 1 system clock after RAS- if it is a memory write cycle.

During memory refresh cycle, RAS- will follow the MRD- command. No CAS- signals are generated.

CAS signals are generated based on which byte is enabled and not during a memory refresh cycle.

3.1.4 Memory Parity Check and Generator

Parity is checked and generated by OTI-051 at an individual byte (odd byte or even byte) during memory read and write respectively.

3.1.5 Memory Address Generator

For DRAM control, the memory address generator takes the system memory address, EDR content of EMS MAP and LA address to generate the 20 bit address for memory. During the memory cycle, the lower order addresses A(0-9) are outputted through MA(1-10). At 1/2 to 1 clock after the RAS-, the higher order addresses A(9 or 19, 10- 18) start to drive the MA(1-10). During the memory refresh, the MA(1-10) is driven from LA(0-9). During the column address time, MA(1) carries address A9 if 256K type DRAMs are used, and carries address A19 if 1M type DRAMs are used. During Cartridge ROM access cycles, address A14 - A22 would be coming out through MA 1 - 9 to access the cartridge ROM.

3.2 DMA CONTROL

DMA Control consists of 3 blocks:
- 2 82C37 DMA Controllers
- DMA Page Registers
- DMA Ready Generator

3.2.1 8237 DMA Controller

The embedded 82C37 DMA Controllers together provide a 7 channel DMA operating at up to 10 MHz synchronized to the system speed. It is used to support 8 and 16-bit transfer operations between memory and peripherals capable of doing the DMA request and transferring data from such devices as a Floppy Controller. Their function is equivalent to the 8237 DMA chip. The DMA channels are assigned as follows:

Channel	Assignment	
Channel0 :	DRQ0	Reserved
Channel1 :	DRQ1	Reserved
Channel2 :	DRQ2	Diskette
Channel3 :	DRQ3	Fixed Disk
Channel4 :	DRQ4	Cascade for Ctrl 1
Channel5 :	DRQ5	Reserved
Channel6 :	DRQ6	Reserved
Channel7 :	DRQ7	Reserved

DMA controller 1 contains channels 0 to 3. It supports 8 bit DMA transfers. Each channel can transfer data throughout the 16MB system address space in 64KB per block at a time. The following figure shows address generation for the DMA channels.

Source	DMA Page Registers	Controller #1
Address	A23<——————>A16	15<———>A0

Note: The signal, 'byte high enable' (BHE-), is generated by inverting address line A0.

DMA controller 2 contains channels 4 to 7. Channel 4 is used to cascade with DMA controller 1. Channels 5, 6, and 7 support 16-bit data transfers throughout the 16M system address space in 128K blocks. However, data cannot be transferred on odd byte boundaries. The following figure shows address generation for the DMA channels.

Source	DMA Page Registers	Controller #2
Address	A23<——————>A17	16<———>A1

Note: The signal, 'byte high enable' (BHE-) and A0 are forced to a logical 0.

Seven DMA channels (0,1,2,3,5,6,7) are available on the I/O channel.

The 8237 DMA controller command code addresses follow:

Table 5. DMA Controller Command Code Addresses

I/O Address (in hex)	Register Function
0000	Channel 0 base and current address reg.
0001	Channel 0 base and current word count
0002	Channel 1 base and current address reg.
0003	Channel 1 base and current word count
0004	Channel 2 base and current address reg.
0005	Channel 2 base and current word count
0006	Channel 3 base and current address reg.
0007	Channel 3 base and current word count
0008	Read Status Reg./Write Command Reg.
0009	Write Request Reg.
000A	Write Single Mask Register Bit
000B	Write Mode Reg.
000C	Clear Byte Pointer Flip-Flop
000D	Read Temporary Reg./Write Master Clear
000E	Clear Mask Reg.
000F	Write All Mask Register Bits
00C0	Channel 4 base and current address reg.
00C2	Channel 4 base and current word count
00C4	Channel 5 base and current address reg.
00C6	Channel 5 base and current word count
00C8	Channel 6 base and current address reg.
00CA	Channel 6 base and current word count
00CC	Channel 7 base and current address reg.
00CE	Channel 7 base and current word count
00D0	Read Status Reg./Write Command Reg.
00D2	Write Request Reg.
00D4	Write Single Mask Register Bit
00D6	Write Mode Reg.
00D8	Clear Byte Pointer Flip-Flop
00DA	Read Temporary Reg./Write Master Clear
00DC	Clear Mask Reg.
00DE	Write All Mask Register Bits

3.2.2 DMA Page Register

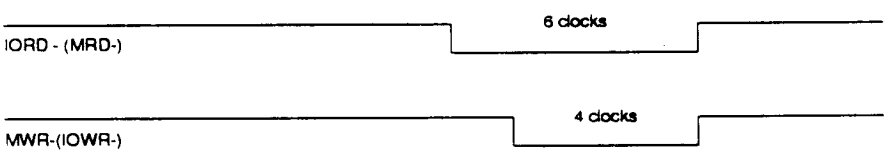
DMA Page Register can be accessed through the 8 bit I/O ports. These can be read or write ports. The following figure shows the address for the page register.

Page Register	I/O Address (in Hex)
DMA channel 0	0087
DMA channel 1	0083
DMA channel 2	0081
DMA channel 3	0082
DMA channel 5	008B
DMA channel 6	0089
DMA channel 7	008A
Refresh	008F

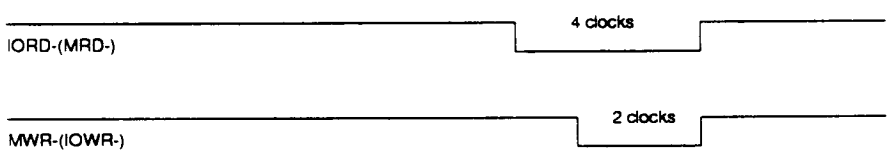
Addresses for all DMA channels do not increase or decrease through page boundaries (64KB for channels 0-3; 128KB for channels 5-7).

3.2.3 DMA Ready Generator

DMA Ready Generator controls the length of command time during the DMA cycle. At normal speed, the minimum DMA command cycle (IOCHRDY is not asserted) is 6/4 DMA clocks:



During FAST DMA cycle, the minimum DMA command cycle is 4/2 DMA clocks:



FAST DMA timing can be selected through indexed port 1E(Hex) bit 6.

The 8237 DMA controller command code addresses follow:

Table 5. DMA Controller Command Code Addresses

I/O Address (in hex)	Register Function
0000	Channel 0 base and current address reg.
0001	Channel 0 base and current word count
0002	Channel 1 base and current address reg.
0003	Channel 1 base and current word count
0004	Channel 2 base and current address reg.
0005	Channel 2 base and current word count
0006	Channel 3 base and current address reg.
0007	Channel 3 base and current word count
0008	Read Status Reg./Write Command Reg.
0009	Write Request Reg.
000A	Write Single Mask Register Bit
000B	Write Mode Reg.
000C	Clear Byte Pointer Flip-Flop
000D	Read Temporary Reg./Write Master Clear
000E	Clear Mask Reg.
000F	Write All Mask Register Bits
00C0	Channel 4 base and current address reg.
00C2	Channel 4 base and current word count
00C4	Channel 5 base and current address reg.
00C6	Channel 5 base and current word count
00C8	Channel 6 base and current address reg.
00CA	Channel 6 base and current word count
00CC	Channel 7 base and current address reg.
00CE	Channel 7 base and current word count
00D0	Read Status Reg./Write Command Reg.
00D2	Write Request Reg.
00D4	Write Single Mask Register Bit
00D6	Write Mode Reg.
00D8	Clear Byte Pointer Flip-Flop
00DA	Read Temporary Reg./Write Master Clear
00DC	Clear Mask Reg.
00DE	Write All Mask Register Bits

4.0 ELECTRICAL CHARACTERISTICS

4.1 A.C. Characteristics

Table 6. A.C. Characteristics of OTI-053

A.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	LOADING CAPACITANCE
t1	REFRQT SETUP Time	35		ns	
t2	CPUHRQ from CLK8		40	ns	CL= 20 pF
t3	CPUHLDA SETUP Time	35		ns	
t4	AEN from CLK8		50	ns	CL= 200 pF
t5	MREFN from CLK8		50	ns	CL= 200 pF
t6	Refresh MEMRDN from CLK8		40	ns	CL= 50 pF
t7	Refresh RASN from CLK8		55	ns	
t8	Refresh Address Valid		60	ns	
t9	DACKN from AEN		5 1/2 TDCY + 70	ns	Note 1
t10	MEMRDN, IORDN from AEN		6 TDCY + 70	ns	Note 1
t11	MEMRDN, IORDN Pulse Width	6 TDCY		ns	Note 1
t12	MEMWRN, IOWRN from IORDN, MEMRDN	2 TDCY		ns	Note 1
t13	MEMWRN, IOWRN Pulse Width	4 TDCY		ns	Note 1
t14	AEN from End of DMA Command		2 TDCY + 50	ns	Note 1
t15	DACKN from End of DMA Command		1/2 TDCY + 70	ns	Note 1
t16	WRITE Data SETUP Time	100		ns	
t17	WRITE Data HOLD Time	20		ns	
t18	READ Data from IORDN		100	ns	
t19	READ Data Float from IORDN	5		ns	
t20	CROMCSN from CPUCLK		40	ns	
t21	RASN from CPUCLK (page mode)		27	ns	CL = 72 pF
t22	CAS from CPUCLK (page mode)		31	ns	CL = 72 pF

Table 6. AC Characteristics of OTI-053 (Continued)

SYMBOL	PARAMETER	MIN	MAX	UNIT	LOADING CAPACITANCE
t25	MDIR from CPUCLK		40	ns	CL = 100 pF
t26	SRDYN Low from CPUCLK (page mode)		25	ns	CL = 50 pF
t27	SRDYN High from CPUCLK		30	ns	CL = 50 pF
t28	ROW Address from CPUCLK		50	ns	CL = 120 pF
t29	COLUMN Address from CPUCLK		40	ns	CL = 120 pF
t30	CAS to MA Hold Time	TCLK-10		ns	Note 2
t31	RASN from CPUCLK (no page mode)		25	ns	CL = 72 pF
t32	CAS from CPUCLK (no page mode)		31	ns	CL = 72 pF
t33	SRDYN Low from CPUCLK (no page mode)		27	ns	CL = 50 pF
t34	SRCSN from CPUCLK		35	ns	
t35	SREN from CPUCLK		35	ns	
t36	MRASN from CPUCLK		35	ns	
t37	SWEHN, SWELN from CPUCLK		35	ns	
t38	Static RAM Address from SA		50	ns	

4.2 D.C. Characteristics of OTI-053

Table 7. D.C. Characteristics of OTI-053

D.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
VOH	Output HIGH Voltage	2.4		V	IOH=400 µA
VOL1	Output LOW Voltage		0.45	V	IOL=20 mA, Note 3
VOL2	Output LOW Voltage		0.45	V	IOL=16 mA, Note 3
VOL3	Output LOW Voltage		0.45	V	IOL=12 mA, Note 3
VOL4	Output LOW Voltage		0.45	V	IOL= 8 mA, Note 3
VOL5	Output LOW Voltage		0.45	V	IOL= 4 mA, Note 3
VOL6	Output LOW Voltage		0.45	V	IOL= 2 mA, Note 3
VIH	Input HIGH Voltage	2.0	VDD+0.5	V	TTL
VIL	Input LOW Voltage	- 0.5	0.8	V	TTL
VIS	Schmit Input HIGH	2.4	VDD+0.5	V	Schmitt, Note 4
VIC	CMOS Input HIGH Voltage	3.8	VDD+0.5	V	CMOS, Note 4
ILI	Input Leakage Current	- 10	10	µA	
OLI	Output Leakage Current	- 10	10	µA	
ICC	Operating Supply Current		100	mA	Input=VDD or VSS No Output Load
CI	Input Capacitance		8	pF	
CO	Output Capacitance		8	pF	
CIO	I/O Capacitance		16	pF	

Notes:
1. TDCY is the internal DMA clock. Minimum period is 100ns.

2. TCLK is CPUCLK period.

3. Output Current (IOL) Capabilities:

20 mA :	MREFN, TC, AEN, DACK7-0
12 mA :	MA1-10
8 mA :	RASN0-7, CASHN0-3, CASLN0-3, SRDYN, MDIR
4 mA :	CROMCSN, A0, SA1-19, A20, SA21-23, MEMRDN, MEMWRN, IORDN, IOWRN
2 mA :	COMRQN, CPUHRQ

4. Input Structures:

Schmitt triggered:	–
CMOS :	CPUCLK, A20, A0
TTL :	all others
Input with pullup:	–

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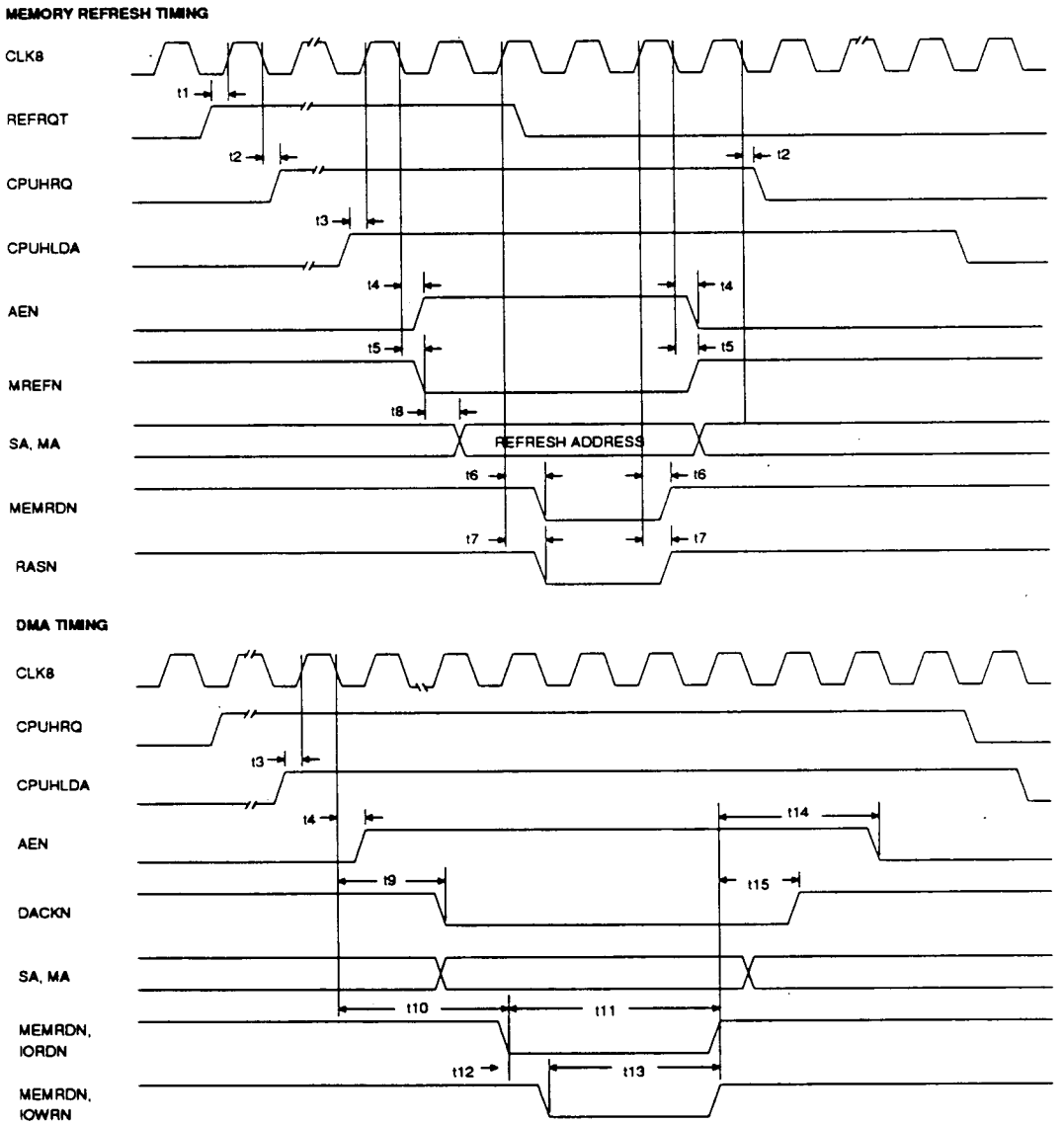
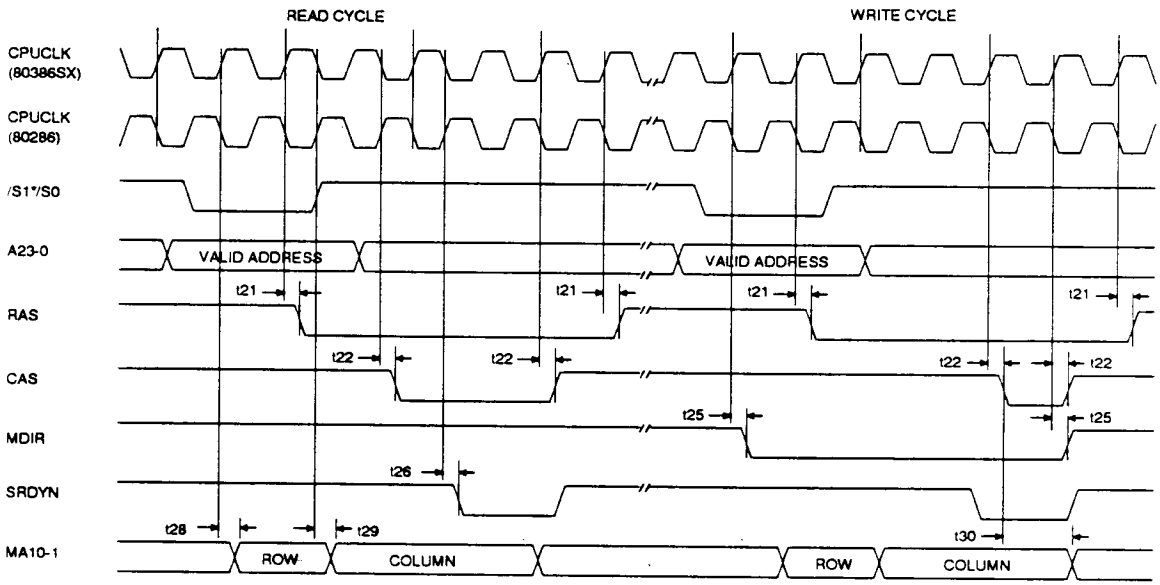
5.0 OTI-053 TIMING DIAGRAMS

FIGURES 3-1 & 3-2



FIGURES 3-3 & 3-4

SYSTEM MEMORY TIMING: DRAM PAGE MODE



SYSTEM MEMORY TIMING: DRAM NO PAGE MODE

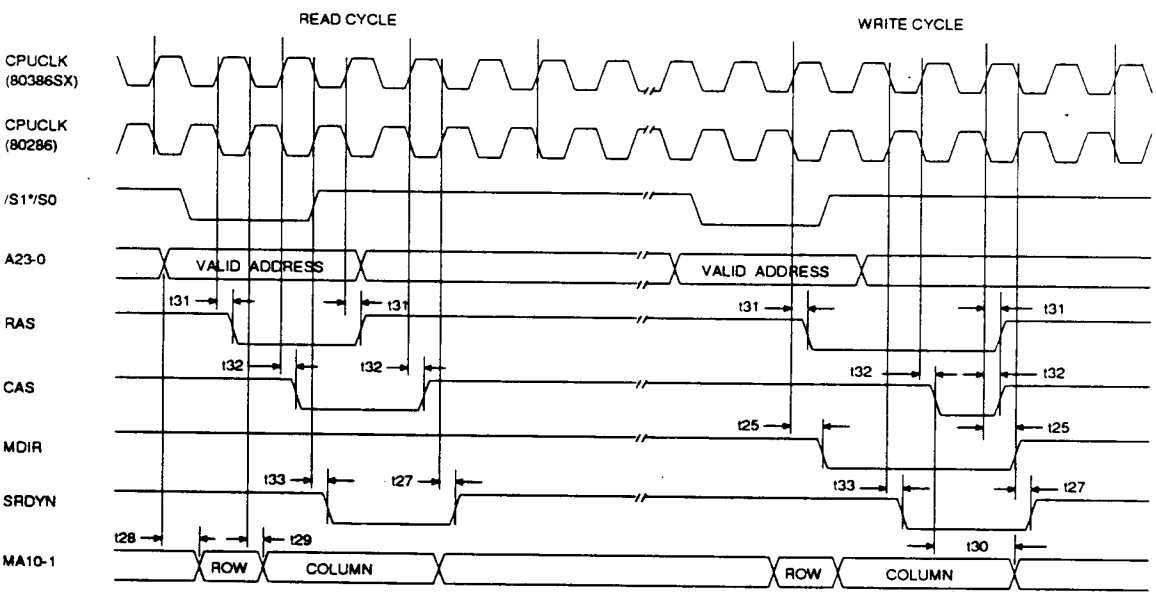


FIGURE 3-5.

SYSTEM MEMORY TIMING: P-SRAM