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Revision 1.1

LXT918

Multi-Segment Hub Repeater

General Description

The LXT918 provides four complete 10 Megabit Ethernet repeaters in one mixed-signal IC. An internal switch matrix allows any of the external ports - including a 7-pin MAC interface - to be switched to any repeater segment at will. Each segment has its own independent Inter-Repeater Backplane which allows multiple segments to be cascaded in stackable and modular hub applications.

The LXT918 provides per-segment and per-port support for the Repeater MIB and for RMON. All variables are implemented as 32-bit counters for maximum roll-over time. A high-speed serial management interface provides software access to the internal switch, RMON and Repeater MIB counters, and to port status and control features.

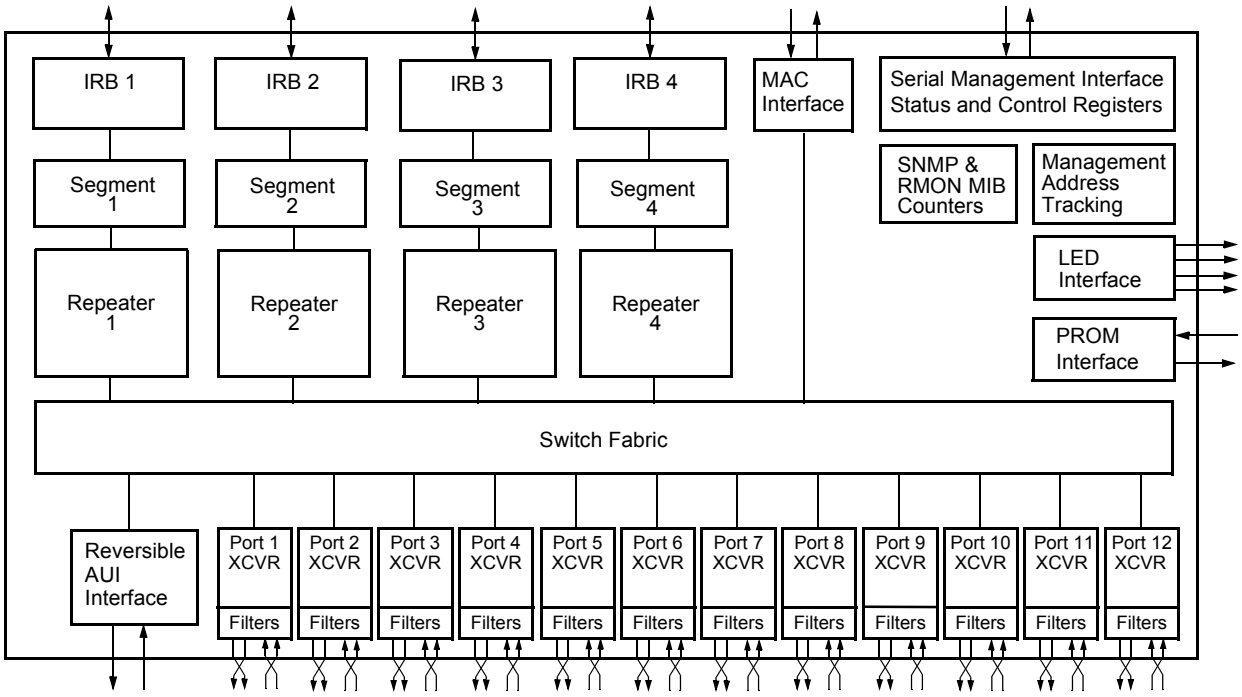
A unique feature of the LXT918 architecture is that when a port is switched to a new segment, its counters follow it. In addition the LXT918 has a SoftReconnect feature, which switches ports without corrupting network traffic.

Features

Advanced features enable new dimensions in Next Generation Repeater applications:

- Four independent 10 Mbit Ethernet Repeaters
- Twelve 10BASE-T ports with Integrated Filters
- Hardware assist for RMON and the Repeater MIB
- Reversible AUI port
- Four mixed-signal backplanes for cascading
- 7-pin "roaming" MAC interface for probe access
- High-speed serial management interface
- Two address-tracking registers per port
- Source Address matching function
- 0-70°C Temperature Range
- 208-pin PQFP

LXT918 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT918QC Pin Assignments

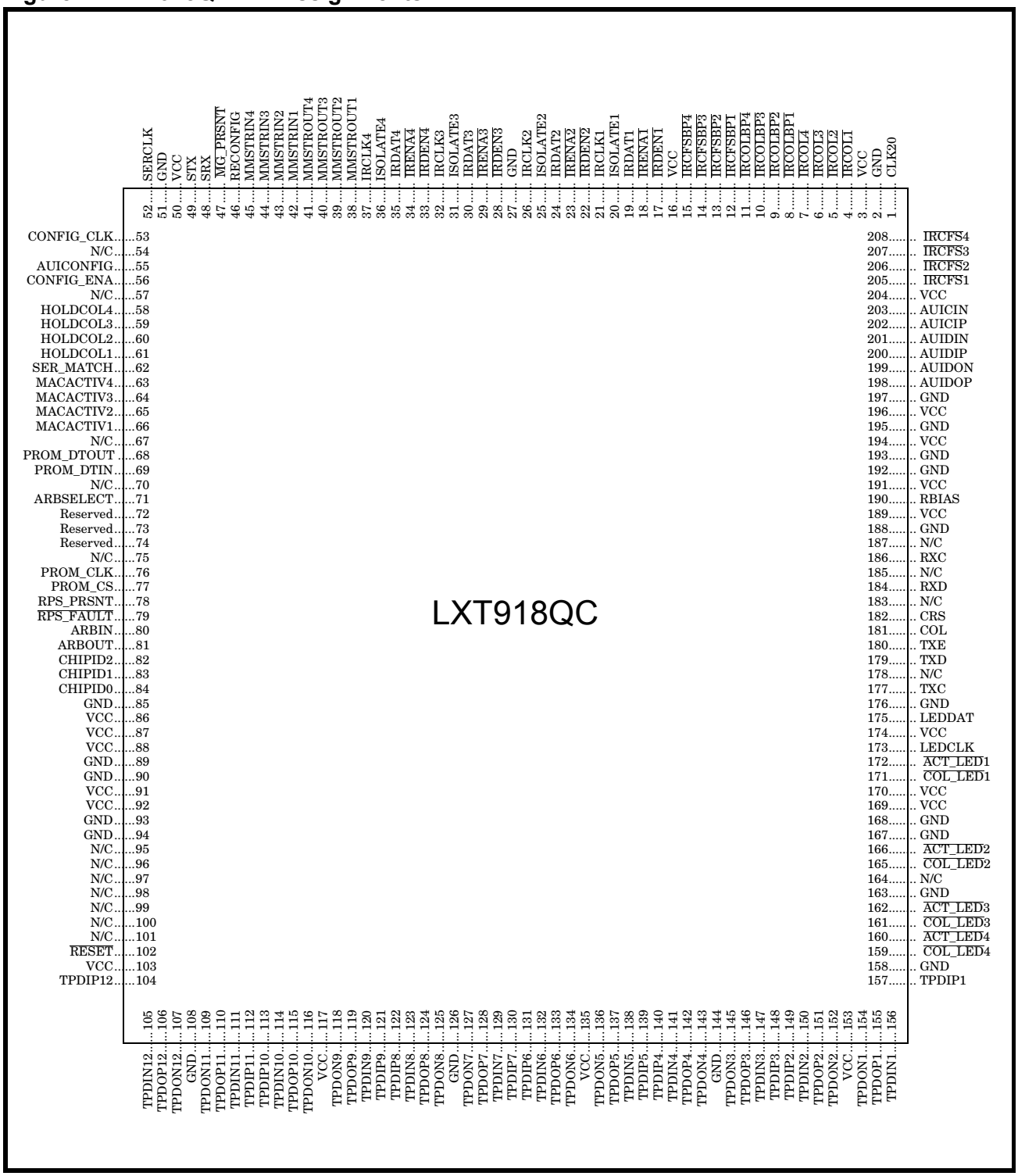


Table 1: Twisted-Pair Port Signal Descriptions

Pin	Symbol	Type	Description
155 154	TPDOP1 TPDON1	Analog Output Port 1	**Twisted-Pair Data Outputs - Ports 1 through 12.** These pins are the positive (TPDOP*x*) and negative (TPDON*x*) differential output pairs from the respective LXT918 twisted-pair port line drivers.
151 152	TPDOP2 TPDON2	Analog Output Port 2	
146 145	TPDOP3 TPDON3	Analog Output Port 3	
142 143	TPDOP4 TPDON4	Analog Output Port 4	
137 136	TPDOP5 TPDON5	Analog Output Port 5	
133 134	TPDOP6 TPDON6	Analog Output Port 6	
128 127	TPDOP7 TPDON7	Analog Output Port 7	
124 125	TPDOP8 TPDON8	Analog Output Port 8	
119 118	TPDOP9 TPDON9	Analog Output Port 9	
115 116	TPDOP10 TPDON10	Analog Output Port 10	
110 109	TPDOP11 TPDON11	Analog Output Port 11	
106 107	TPDOP12 TPDON12	Analog Output Port 12	
157 156	TPDIP1 TPDIN1	Analog Input Port 1	**Twisted-Pair Data Inputs - Ports 1 through 12.** These pins are the positive (TPDIP*x*) and negative (TPDIN*x*) differential input pairs to the respective LXT918 twisted-pair ports.
149 150	TPDIP2 TPDIN2	Analog Input Port 2	
148 147	TPDIP3 TPDIN3	Analog Input Port 3	
140 141	TPDIP4 TPDIN4	Analog Input Port 4	
139 138	TPDIP5 TPDIN5	Analog Input Port 5	
131 132	TPDIP6 TPDIN6	Analog Input Port 6	
130 129	TPDIP7 TPDIN7	Analog Input Port 7	
122 123	TPDIP8 TPDIN8	Analog Input Port 8	
121 120	TPDIP9 TPDIN9	Analog Input Port 9	
113 114	TPDIP10 TPDIN10	Analog Input Port 10	
112 111	TPDIP11 TPDIN11	Analog Input Port 11	
104 105	TPDIP12 TPDIN12	Analog Input Port 12	

Table 2: AUI Port Signal Descriptions

Pin	Symbol	Type	Description
55	AUICONFIG	TTL Input PD	**AUI Configuration Data In.** Up to 16 bits of AUI Configuration Register data is shifted in via this pin (LSB to MSB). Bits 15:1 are user defined. Bit 0 sets the AUI port operating mode as follows: 0 = Normal (DTE) mode; 1 = Reversed (MAU) mode.
56	CONFIG_ENA	TTL Output	**AUI Configuration Register Read Enable.** An active Low pulse is output on this pin at the beginning of each AUI Configuration Register read cycle. This signal is provided to control an external shift register.
53	CONFIG_CLK	TTL Output	**AUI Configuration Register Clock.** The LXT918 drives sixteen 100ns clock pulses on this pin each time the AUI Configuration Register is read. This signal is used to clock in configuration data (up to 16 bits) from an external shift register.
198 199	AUIDOP AUIDON	Analog Output	**AUI Data Outputs**. Positive and negative data outputs from the AUI port. In normal (DTE) mode, connect to pins 3 and 10 of the AUI D-connector. In reverse (MAU) mode, connect to pins 5 and 12 of the AUI D-connector.
200 201	AUIDIP AUIDIN	Analog Input	**AUI Data Inputs.** Positive and negative data inputs to the AUI port. In normal (DTE) mode, connect to pins 5 and 12 of the AUI D-connector. In reverse (MAU) mode, connect to pins 3 and 10 of the AUI D-connector.
202 203	AUICIP AUICIN	Tri-State, Analog, I/O	**AUI Collision Inputs.** In normal (DTE) mode these pins are the positive and negative collision inputs for the AUI port. In reverse (MAU) mode these pins are outputs.

1. PD = Input contains pull-down.

Table 3: Inter-Repeater Backplane Signal Descriptions

Pin	Symbol	Type	Description
17 22 28 33	$\overline{\text{IRDEN1}}$ $\overline{\text{IRDEN2}}$ $\overline{\text{IRDEN3}}$ $\overline{\text{IRDEN4}}$	Open-Drain Output	**IRB Driver Enables - Segments 1 through 4.** These outputs allow multiple devices to share a common set of external bi-directional transceivers (‘245s) for driving the IRB’s off-board. Each IRB must have its own transceiver. When a device assumes control of an IRB, it drives the corresponding $\overline{\text{IRDENx}}$ output Low. When an IRB is idle, a 330 Ω pull-up resistor (required) pulls the corresponding $\overline{\text{IRDEN}x}$ output High. Attach each output to the direction control of the corresponding transceiver.
18 23 29 34	$\overline{\text{IRENA1}}$ $\overline{\text{IRENA2}}$ $\overline{\text{IRENA3}}$ $\overline{\text{IRENA4}}$	CMOS I/O Open Drain	**Inter-Repeater Backplane Enables - Segments 1 through 4.** These active Low outputs indicate carrier presence on the corresponding IRB’s. When an IRB is idle, a 330 Ω pull-up resistor pulls the corresponding $\overline{\text{IRENA}x}$ output High. These signals may be buffered between modules.
19 24 30 35	IRDAT1 IRDAT2 IRDAT3 IRDAT4	CMOS I/O Open Drain	**IRB Data - Segments 1 through 4.** These bidirectional signals carry data on the corresponding IRB’s. Data is driven and sampled on the rising edge of the corresponding IRCLK. Each of these signals must be pulled up by a 330 Ω resistor. Between modules, these signals can be buffered.

1. PU = Input contains pull-up.
2. PD = Input contains pull-down.
3. NC = No Clamp. Pad will not clamp input in the absence of power.
4. Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 3: Inter-Repeater Backplane Signal Descriptions – continued

Pin	Symbol	Type	Description
20 25 31 36	ISOLATE1 ISOLATE2 ISOLATE3 ISOLATE4	Output	**Isolate Enables - Segments 1 through 4.** These outputs allow one device per module the ability to isolate the IRB's from the outside world. Attach each output to the Enable input of the corresponding transceiver. The output is driven High (disable) when the corresponding IRB should be isolated, and Low (enable), when it should not be isolated.
21 26 32 37	IRCLK1 IRCLK2 IRCLK3 IRCLK4	CMOS I/O TriState, PU Schmitt Trigger #2	**IRB Clocks - Segments 1 through 4.** These bi-directional, non-continuous, 10 MHz clocks are recovered from received network traffic. During idle periods, these outputs are high-impedanced. Schmitt triggering is used to increase noise immunity, therefore full rail-to-rail signals are required. Between modules, buffering may be used on these signals.
4 5 6 7	$\overline{\text{IRCOL1}}$ $\overline{\text{IRCOL2}}$ $\overline{\text{IRCOL3}}$ $\overline{\text{IRCOL4}}$	CMOS I/O Open Drain	**IRB Collision - Segments 1 through 4.** Each of these outputs is driven Low to indicate that a collision has occurred on the corresponding segment. When there is no collision, a 330 Ω pull-up resistor (required) on each output pulls it High. These signals are intended only to be used between devices on the same module; they may not be buffered.
8 9 10 11	$\overline{\text{IRCOLBP1}}$ $\overline{\text{IRCOLBP2}}$ $\overline{\text{IRCOLBP3}}$ $\overline{\text{IRCOLBP4}}$	CMOS I/O Open Drain NC	**IRB Collision-BackPlane - Segments 1 through 4.** These active Low outputs have the same function as $\overline{\text{IRCOL}}$, but are used between modules. Attach these signals only from the device with ChipID = 0 to the backplane or connector, **without buffering**. Each output must be pulled up by one 330Ω resistor per system.
205 206 207 208	$\overline{\text{IRCFS1}}$ $\overline{\text{IRCFS2}}$ $\overline{\text{IRCFS3}}$ $\overline{\text{IRCFS4}}$	Analog, I/O	**IRB Collision Force Sense - Segments 1 through 4.** Each of these three-state analog outputs indicates that a transmit collision has occurred on its corresponding segment when it is driven Low. Each must be pulled up with a 680 Ω 1% resistor. These signals are intended only to be used between devices on the same module; they may not be buffered.
12 13 14 15	$\overline{\text{IRCFSBP1}}$ $\overline{\text{IRCFSBP2}}$ $\overline{\text{IRCFSBP3}}$ $\overline{\text{IRCFSBP4}}$	Analog I/O, N/C	**IRB Collision Force Sense-BackPlane - Segments 1 through 4.** These outputs have exactly the same function as $\overline{\text{IRCFS}}$, but are used between modules. Attach these signals only from the device with ChipID = 0 to the backplane or connector, **without buffering**. Each output must be pulled up by one 330 Ω, 1% resistor per system.
61 60 59 58	HOLDCOL1 HOLDCOL2 HOLDCOL3 HOLDCOL4	TTL Tri-state I/O, PD	**Hold Collision - Segments 1 through 4.** Each of these active High signals is driven by the device with ChipID = 0 to extend a non-local transmit collision to other devices on the same module. The HOLDCOLx signals from different modules should NOT be attached together.

1. PU = Input contains pull-up.
2. PD = Input contains pull-down.
3. NC = No Clamp. Pad will not clamp input in the absence of power.
4. Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 3: Inter-Repeater Backplane Signal Descriptions – continued

Pin	Symbol	Type	Description
42 43 44 45	MMSTRIN1 MMSTRIN2 MMSTRIN3 MMSTRIN4	TTL Input, NC	**Management Master In - Segments 1 through 4**. The MMSTR daisy chain ensures that collisions will be counted correctly in multi-module applications. Attach the MMSTRIN input of each device to the MMSTROUT output of the previous device. Ground MMSTRIN of the first or only device.
38 39 40 41	MMSTROUT1 MMSTROUT2 MMSTROUT3 MMSTROUT4	Output, NC	**Management Master Out - Segments 1 through 4**. MMSTR daisy chain output. In hot-swap applications, a 1 kΩ - 3 kΩ resistor can be used as a bypass between MMSTRIN and MMSTROUT.
66 65 64 63	MACACTIV1 MACACTIV2 MACACTIV3 MACACTIV4	TTL Input, PD	**MAC Active - Segments 1 through 4.** These active High inputs allow external Ethernet controllers to directly drive the Inter Repeater Backplanes. When the controller asserts MACACTIV*x*, the LXT918 drives the $\overline{\text{IRCOL}x}$, $\overline{\text{IRCOLBP}x}$, $\overline{\text{IRCFS}x}$ and $\overline{\text{IRCFSBP}x}$ signals on behalf of the controller. If any of these inputs are unused, tie them to ground.

1. PU = Input contains pull-up.
2. PD = Input contains pull-down.
3. NC = No Clamp. Pad will not clamp input in the absence of power.
4. Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 4: MAC Interface Signal Descriptions

Pin	Symbol	Type	Description
177	TXC	Output	**Transmit Clock.** This 10 MHz continuous output is derived from the 20 MHz input clock.
179	TXD	TTL Input, PD	**Transmit Data.** External controllers use this input to transmit data to the LXT918. The device samples TXD on the rising edge of TXC, when TXE is High.
180	TXE	TTL Input, PD	**Transmit Enable** External controllers drive this input High to indicate that data is being transmitted on the TXD pin. Tie this input Low if it is unused.
181	COL	Output	**Collision**. The LXT918 drives this signal High to indicate that a collision has occurred.
182	CRS	Output	**Carrier Sense.** The LXT918 drives this signal High to indicate that valid data is present on RXD.
184	RXD	Output	**Receive Data.** The LXT918 transmits received data to the controller on this output. Data is driven on the falling edge of RXC.
186	RXC	Output	**Receive Clock.** This is a non-continuous 10 MHz clock that the LXT918 recovers from the network when traffic is actively being received.

1. PD = Input contains pull-down.

Table 5: Serial Management Interface Signal Descriptions

Pin	Symbol	Type	Description
46	RECONFIG	TTL Input, NC	**Reconfigure**. This input controls the driving of the clock signal on the high-speed serial management interface (SERCLK). When this input is High, the LXT918 drives SERCLK with a 625 kHz output. When this input is Low, SERCLK is an input to the LXT918. In addition, a Low-to-High transition on RECONFIG causes the LXT918 to drive 13 continuous 0's on the serial management bus, causing a re-arbitration to occur.
47	$\overline{\text{MG\_PRSNT}}$	TTL Input, NC	**Manager Present**. This signal is sensed at power up. If it is High, it indicates that no local manager is present, and the 918 enables all ports and sets all LEDs to operate in "hardware mode". If it is Low, indicating that a manager is present, the 918 disables all ports, pending control of network manager.
48	SRX	TTL Input	**Serial Receive.** Receive data input for high-speed serial management interface. Must be tied to STX externally. SRX is sampled on the rising edge of SERCLK.
49	STX	Open Drain Output	**Serial Transmit.** Transmit data output for high-speed serial management interface. Must be tied to SRX externally. Data transmitted on STX is compared with data received on SRX. In the event of a mismatch, STX is put in the high impedance state. STX is driven on the falling edge of SERCLK.
52	SERCLK	Tri-State TTL Output	**Serial Clock.** Clock for serial management interface. Depending on RECONFIG, this pin is either a 625 kHz output or a 0 to 1 MHz input.

1. NC = No Clamp. Pad will not clamp input in the absence of power.

Table 6: LED Signal Descriptions

Pin	Symbol	Type	Description
171 165 161 159	$\overline{\text{COL\_LED1}}$ $\overline{\text{COL\_LED2}}$ $\overline{\text{COL\_LED3}}$ $\overline{\text{COL\_LED4}}$	Open-Drain Output, PU	**Collision LED Driver - Segments 1 through 4.** These outputs provide up to 10 mA of sink current.
172 166 162 160	$\overline{\text{ACT\_LED1}}$ $\overline{\text{ACT\_LED2}}$ $\overline{\text{ACT\_LED3}}$ $\overline{\text{ACT\_LED4}}$	Open-Drain Output, PU	**Activity LED Driver - Segments 1 through 4.** These outputs provide up to 5 mA of sink current.
173	LED_CLK	Output	**LED Clock.** Clock for LED serial data output.
175	LED_DAT	Output	**LED Data.** Serial data output for LED data.

1. PU = Pad contains pull-up.

Table 7: PROM Interface Signal Descriptions

Pin	Symbol	Type	Description
76	PROM_CLK	TTL Input, Tri-State Output	**PROM Clock.** 1 MHz clock for reading PROM data.
77	PROM_CS	Tri-State Output, PD	**PROM Chip Select.**
68	PROM_OUT	Tri-State Output, PD	**PROM Data Output.**
69	PROM_IN	TTL Input	**PROM Data Input.** If a PROM is not used, this input can be tied Low or High.

1. PD = Input contains pull-down.

Table 8: Power Supply and Indication Signal Descriptions

Pin	Symbol	Type	Description
3, 16, 50, 86, 87, 88, 91, 92, 103, 117, 135, 153, 169, 170, 174, 189, 191, 194, 196, 204	VCC	Power	**Power Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to digital ground should be supplied for every one of these pins.
2, 27, 51, 85, 89, 90 93, 94, 108 126, 144, 158, 163, 167, 168, 176, 188, 192, 193, 195, 197	GND	Power	**Ground.** Connect each of these pins to digital ground. Note: the LXT918 does NOT require separate digital and analog grounds.
190	RBIAS	Analog	**RBias**. Connect this pin to ground through a 22 kΩ, 1% resistor. Note: Do NOT route any other signals near or around this resistor.
78	RPS_PRSNT	TTL Input	**Redundant Power Supply**. Active High input indicates presence of redundant power supply. The state of this input and the $\overline{\text{RPS\_FAULT}}$ input is reflected in the RPS LED bit in the serial LED output (refer to Tables 10 and 11). Tie Low if not used.
79	$\overline{\text{RPS\_FAULT}}$	TTL Input	**Redundant Power Supply Fault**. Active Low input indicates redundant power supply fault. Tie High if not used.

Table 9: Miscellaneous Signal Descriptions

Pin	Symbol	Type	Description
1	CLK20	CMOS Input, Schmitt Trigger #1	**20 MHz System Clock**. Drive with CMOS levels.
62	SER_MATCH	Output	**Hub ID Match.** Active High. The device with ChipID = 0 asserts this signal whenever it detects a message on the serial bus which matches the local Hub ID.
71	ARBSELECT	TTL Input, PU	**Arbitration Select**. If this pin is pulled Low, Arbitration Mechanism #1 is disabled, only Arbitration Mechanism #2 will be available. If this pin is pulled High, both mechanisms will be enabled. If Arbitration Mechanism #1 is enabled, the device with ChipID = 0 will transmit an "Arbitration Request" message every 2-3 ms on the serial management interface until a Hub ID is assigned.
80	ARBIN	Tri-State Input, PD, NC	**Arbitration In/Out**. Daisy chain hub ID arbitration mechanism #2. If used, tie ARBIN to ARBOUT of the previous device, and to ground of the first/only device. If unused, tie ARBIN High.
81	ARBOUT	Output, NC	
82 83 84	CHIPID2 CHIPID1 CHIPID0	TTL Input	**Chip ID.** These pins assign unique ChipIDs to as many as eight devices on a single module. One device on each module must be assigned ChipID=0.
102	$\overline{\text{RESET}}$	CMOS Input, Schmitt Trigger #1, PU, NC	**Reset**. This active Low input causes internal circuits and state machines to reset, but does not affect counters or address tracking registers. On power-up, devices should not be brought out of reset until the power supply has stabilized and reached 4.5 volts. When there are multiple devices, it is recommended that all be supplied by a common reset that is driven by an 'LS14 or similar device.
72, 73, 74	RESERVED	-	**Reserved**. Reserved for future application development. *Leave these pins unconnected.*
53, 54, 56, 57, 67, 70, 75, 95, 96, 97, 98, 99, 100, 101, 164, 178, 183, 185, 187	NO CONNECT	-	***No Connects***. *Leave these pins unconnected.*

1. PU = Input contains pull-up.
2. PD = Input contains pull-down.
3. NC = No Clamp. Pad will not clamp input in the absence of power.

FUNCTIONAL DESCRIPTION

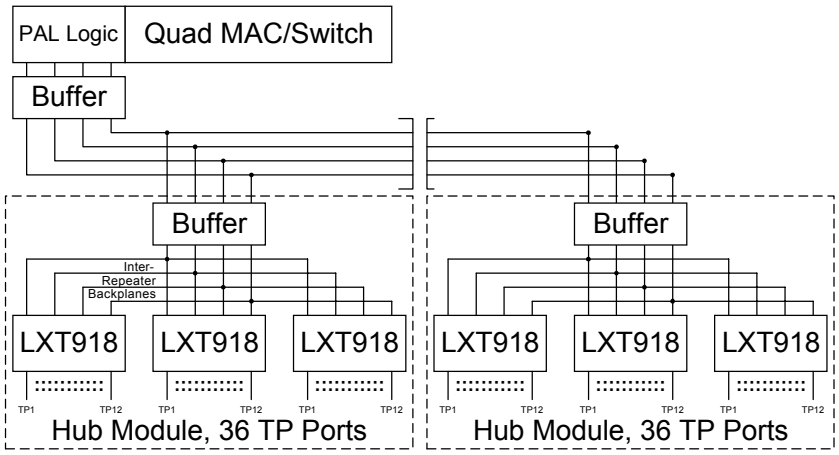
Introduction

With its unique port-switching architecture, the LXT918 revolutionizes the design of networking products by facilitating hybrid repeater/switch architectures. A mixture of the traditional repeater and the state-of-the-art switch, the hybrid repeater/switch architecture provides a cost optimized solution that allows network bandwidth to be allocated as needed under the control of the end-user. The key to this approach is to tie switched 10 Megabit outputs to the 14 LXT918 ports (12 TP + AUI + 7-Pin MAC Interface). This can be done in several different architectures depending on application needs as shown in Figure 2.

Figure 2: LXT918 Hybrid Architecture

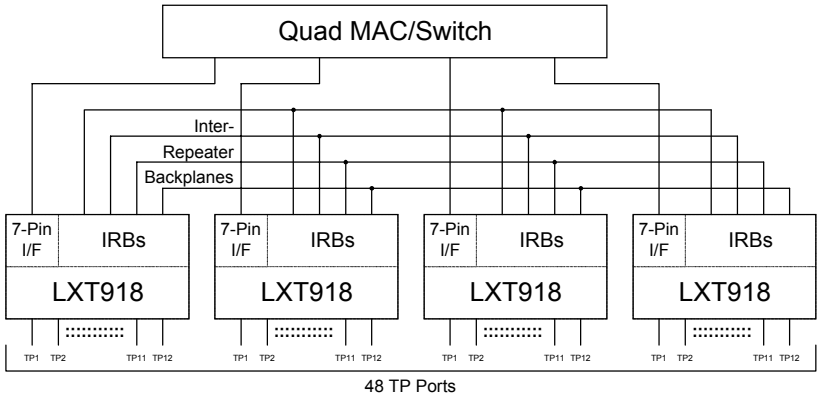
Architecture Type 1:

IRB Connected Switch



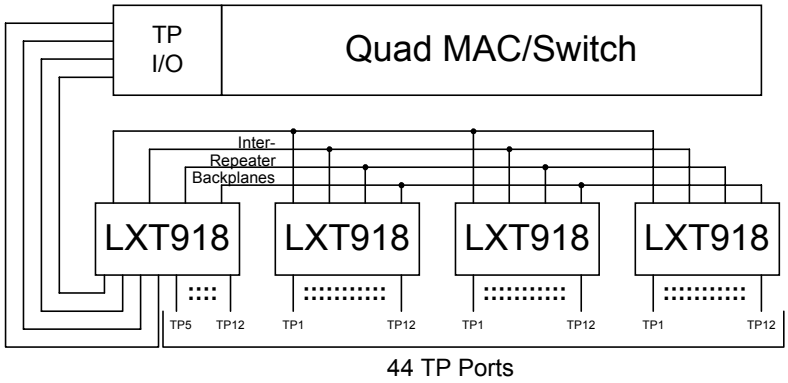
Architecture Type 2:

Direct MAC Connected Switch



Architecture Type 3:

Twisted Pair Connected Switch



The switching matrix of the LXT918 allows the dedicated bandwidth of the switch outputs to be shared among a set of users, which can be changed at will. The additional cascading capability provided by the Inter Repeater Backplanes allows the set of users sharing the bandwidth to grow arbitrarily larger. A more detailed LXT918 application block diagram is shown in Figure 3.

The switching capabilities of the LXT918 also create support for static VLANs (Virtual LANs), where users can easily be re-configured to support moves, adds and changes to the network topology. The switchable MAC interface provides the opportunity for a built-in "roaming" network monitoring or bridging function.

10BASE-T Ports

The LXT918 provides 10BASE-T ports with integrated filters. Level One's patented filter technology helps facilitate low-cost systems which meet EMI requirements. Refer to Table 1 for 10BASE-T port pin assignments and signal descriptions.

AUI Port

The LXT918 provides a reversible AUI interface that can function either as a DTE or as a MAU. When this interface functions as a MAU, it supports remote-office and embedded-hub applications (such as file servers) by allowing integration of the LXT918 to existing PHY interfaces. The mode of operation is determined by bit 0 of the AUI Configuration Register. Refer to Table 2 for AUI port pin assignments and signal descriptions.

Inter-Repeater Backplane

The LXT918 easily accommodates stackable and modular hub architectures through the Inter-Repeater Backplane, which allows multiple devices to function as one logical repeater. For example, typical LXT918 stack designs accommodate as many as 192 10BASE-T ports. Refer to Table 3 for IRB pin assignments and signal descriptions.

7-pin MAC Interface

The LXT918 provides a 7-pin MAC Interface, which can be interfaced to an Ethernet controller or a switch ASIC. Refer to Table 4 for MAC Interface pin assignments and signal descriptions.

Serial Management Interface

Multiple devices can easily be managed through the high-speed serial management interface. This synchronous interface operates at rates up to 1 Mbps, and uses an HDLC-like zero-bit insertion protocol. This interface provides access to the Port Switching functions, RMON and Repeater MIB variables as well as complete control over all device functions and visibility of all status registers. Refer to Table 5 for Serial Management Interface pin assignments and signal descriptions.

Management Support

The LXT918 supports RMON and the Repeater MIB using on-chip 32-bit counters. Counters are provided for each port, including the MAC Interface port, and for each segment. Interface counters include all of the RMON Statistics group and Repeater MIB Total Octets and Transmit Collisions. Per-port counters include:

Readable Frames	Readable Octets	FCS Errors
Alignment Errors	FramesTooLong	ShortEvents
Runts	Collisions	LateEvents
VeryLongEvents	DataRateMismatch	AutoPartitions
Broadcast	Multicast	SA Changes

Source Address Management Functions

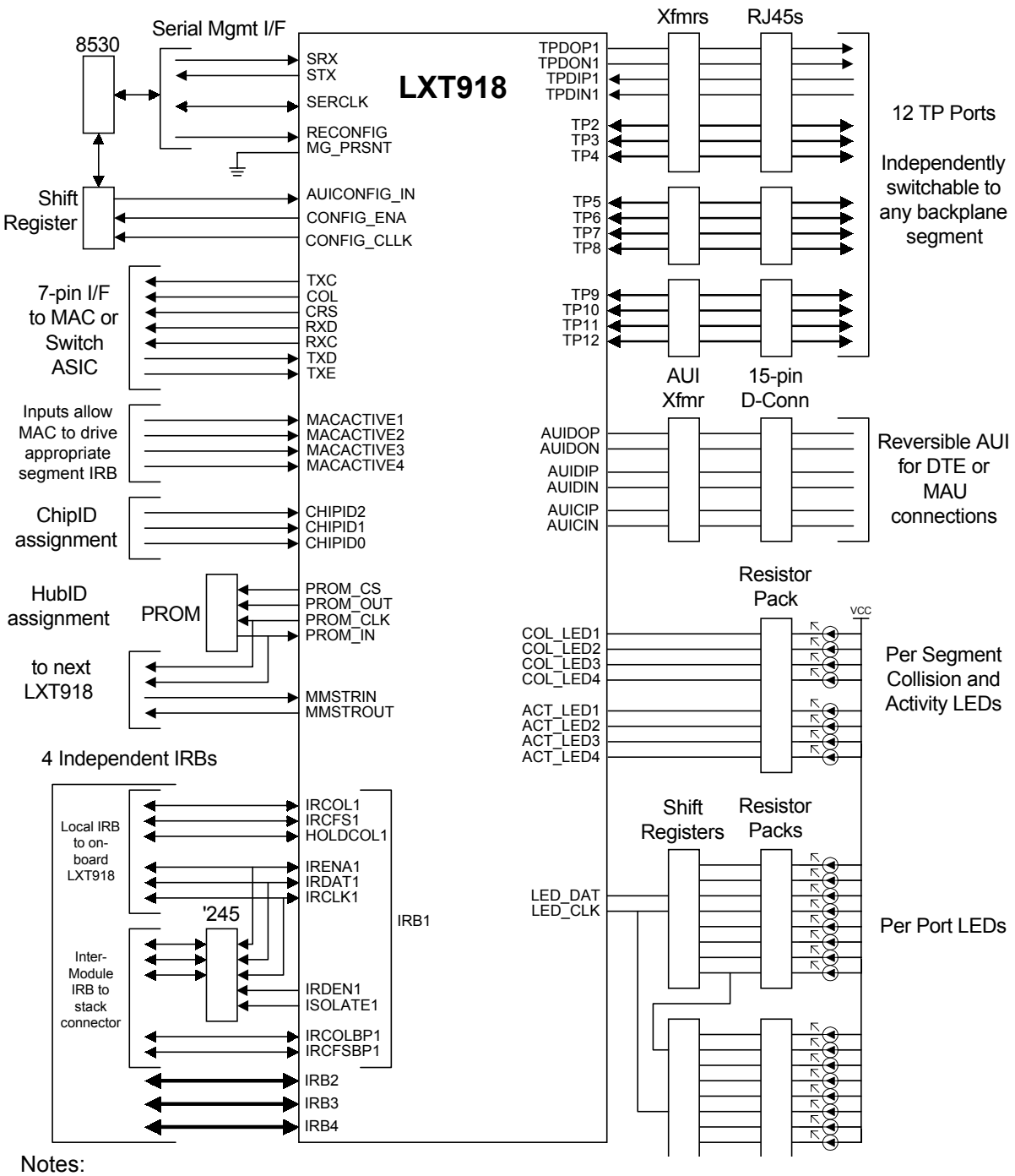
The LXT918 provides Source Address Management functions for all ports. Each port has two source address tracking registers. The rptrAddrTrackNewLastSrcAddress register is always free-running and contains the source address of the last valid packet received from the port. The Authorized Address Register operates in three states: free-run, lock-on-next or lock. This register can track source addresses or lock on an address that has been assigned by the network manager or that it has previously tracked. Once this register is locked, subsequent Source Address changes on a port cause the device to set the corresponding bits in the SA Change Detection Register and the Interrupt Status Register.

The LXT918 also provides a Source Address Tracking Function for each segment. Supplied with a 48-bit Ethernet Source Address, this function identifies all ports on a particular segment that sourced that Source Address.

LED Interface

The serial LED interface (data and clock) supplies link and partition status for each of the TP ports, status for the AUI port, and miscellaneous functions. The device directly provides activity and collision LEDs for each segment. Refer to Table 6 for LED Interface pin assignments and signal descriptions.

Figure 3: Typical Application Block Diagram



Notes:

1. Refer to Figure 11 for typical TP port interface circuitry.
2. Refer to Figures 12 and 13 for typical AUI port interface circuitry.
3. Refer to Figure 14 for typical IRB circuitry.
4. Refer to Figure 15 for typical Serial Management Interface circuitry.
5. Refer to Figure 17 for typical PROM circuitry.

Requirements

Power

The LXT918 requires a single +5V power supply, and a single ground reference. Separate analog and digital grounds are NOT required. Refer to Table 8 for power and ground pin assignments.

Clock

The LXT918 requires a continuous 20 MHz clock input, driven with CMOS levels.

RBIAS Input

The LXT918 requires a 1%, 22 kΩ resistor connecting its RBIAS input to ground.

Reset Signal

At power up, the $\overline{\text{RESET}}$ input must be held Low until VCC reaches at least 4.5V. An 'LS14 or equivalent should be used to drive $\overline{\text{RESET}}$ if there are multiple 918 devices.

External PROM

The LXT918 requires an external, auto-incrementing PROM, which is used to supply a 48-bit ID at power-up. If the PROM is not available, the PROM data input signal must be tied either High or Low. Multiple devices on the same module can share a single common PROM. Refer to Table 7 for PROM interface pin assignments and signal descriptions.

Chip Identification

Each LXT918 on a module requires a unique 3-bit Chip ID value asserted on these pins in order for the serial management bus to function correctly. One LXT918 on each module must be assigned ChipID = 0.

Management Master I/O Link

In multiple device applications, the Management Master daisy chain (MMSTRIN/MMSTROUT) ensures that collisions are counted correctly. Connect the MMSTRIN input to the MMSTROUT output of the previous device, even across module boundaries. Ground the MMSTRIN input of the first or only device in the system. In hot-swap applications, resistive bypassing can be used, with a value between 1k and 3 kΩ.

Repeater Operation

LXT918 repeater operation is controlled by the state machine shown in Figure 4. When the LXT918 detects activity at any input, it begins generating preamble to all other outputs on the same segment. Once 62 bits of preamble have been transmitted, and a start-of-frame delimiter (SFD) has been received, the device begins repeating the received packet to all outputs on that segment. An internal FIFO provides buffering. Operation continues until the receiver goes idle, or until the jabber timer is exceeded.

If activity is detected simultaneously at two or more inputs on the same segment, that segment enters the transmit collision state. The device sends a jam signal to all ports on that segment for 96 bit times. A jam signal continues to be sent to all ports as long as two or more inputs on that segment are active. If activity simultaneously ceases at all inputs, the segment returns to the idle state. If activity continues at only one input, the segment enters the one-port-left state. In that state, the device continues to transmit a jam signal to all ports on that segment *except* to the one that has the active input. Once this activity ceases, the segment returns to the idle state.

If the AUI port is functioning as the DTE, and an external MAU activates the CI inputs while the port is active, the segment to which the AUI port is attached enters the receive collision state. The device sends a jam signal to all ports on the segment except for the AUI port for at least 96 bit times and until all activity ceases.

In multiple-device configurations, all devices participate in data exchange and the various collision states via the Inter Repeater Backplane.

Exception Conditions

Fragment Extension

Any received activity shorter than 96 bits (also known as a fragment) will be extended so that it is at least 96 bits long. On the Inter Repeater Backplane, a fragment extension will look like a receive collision, however it will not be counted as a collision.

Packets with No SFD

Packets with no start-of-frame delimiter will be repeated to all ports as long preamble patterns with no SFD. These packets will be counted as "fragments" by the management counters, no matter how long they are.

Packets with Too Early SFD

Any packet with less than 40 bits of preamble will cause the internal FIFO to overflow, causing invalid packets to be transmitted to all ports.

If the EFIFOERR bit in the Master Configuration register is set when this occurs, a transmit collision will be generated.

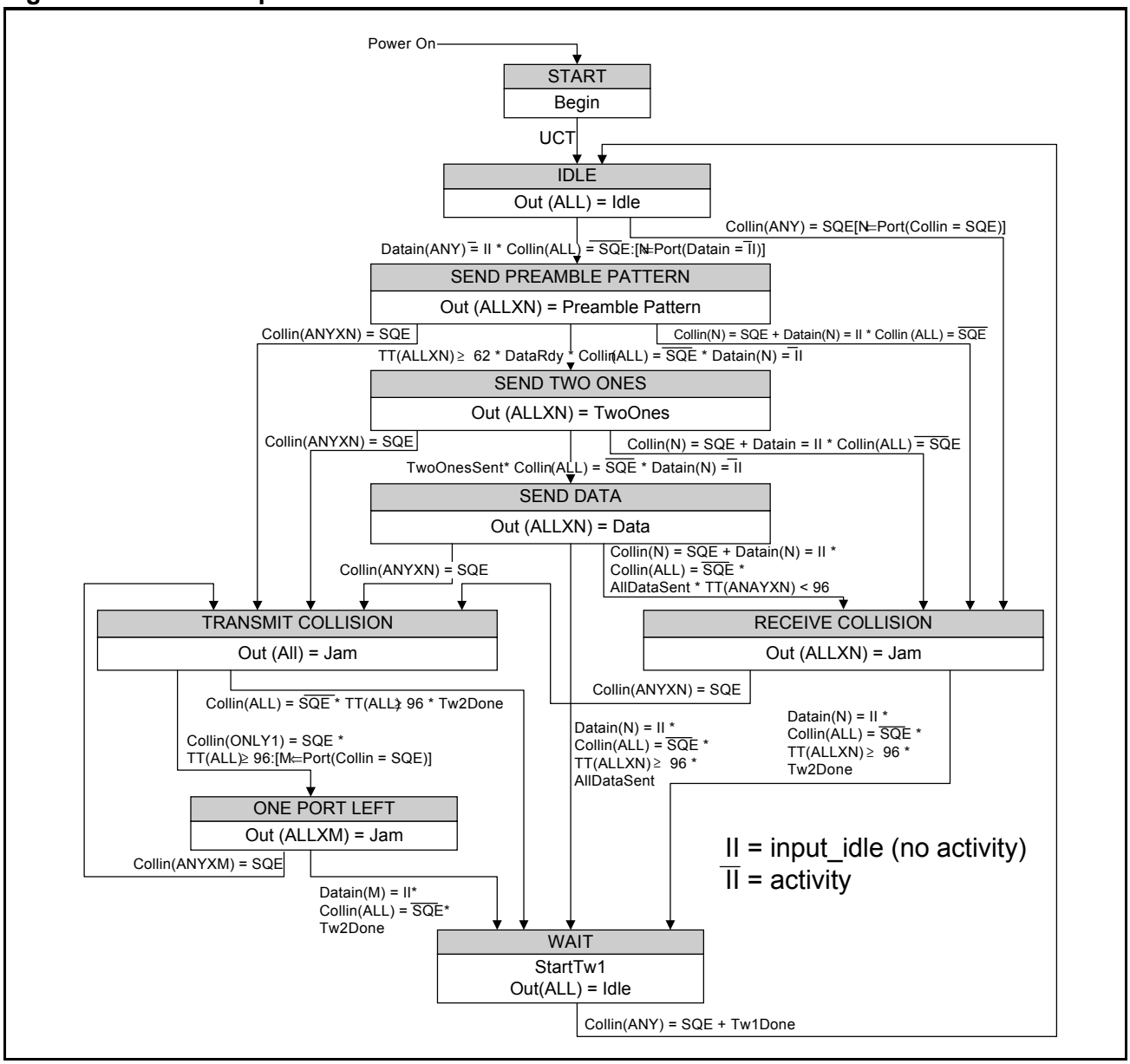
Manchester Code Violations

If the EMCV bit in the Master Configuration register is set, an input packet with Manchester Code Violations will be treated as a transmit collision. If this bit is clear (default), incoming packets with this type of error will simply be repeated to all ports. **Note that a packet that does not have a proper end-of-frame marker (2 bit times High with no transitions) will also be flagged as having a Manchester Code Violation.**

Data Rate Mismatches

Severe data rate mismatches will cause the internal FIFO to underflow or overflow. Depending on the state of the EFIFOERR bit, these conditions can be treated either as transmit collisions, or simply passed along as bad data.

Figure 4: LXT918 Repeater State Machine



Port Functions

Jabber (all ports)

If any input port is active for more than 5 ms, the device will automatically terminate all transmit activity for at least 96 bit times. This will give waiting ports an opportunity to access the network. A port that is continuously babbling will constantly collide with other ports, and will eventually be isolated by the auto-partitioning function.

Auto-partitioning (all ports)

Any port that causes 32 consecutive collisions will be *partitioned* as shown in Figure 5. A port will also be partitioned if it continues to be active for more than 100 µs after a collision has occurred. Once a port is partitioned, data received from that port is not repeated, until the port is *reconnected*. There are two re-connection algorithms. The normal algorithm allows a port to be reconnected if a packet can be successfully transmitted or received from the port. The alternative algorithm allows re-connection only if a packet can be successfully transmitted to the port. For re-connection to occur, at least 512 bit times of non-idle, non-collision activity must occur. Once this happens, the port is re-connected after the activity stops. The activity that causes the re-connection is *not* repeated.

Link Integrity Function (10BASE-T ports only)

The device supports the Link Integrity function, which is used to determine if a 10BASE-T connection is working. The function can be enabled on a port-by-port basis. When enabled, the device looks for Link Integrity Pulses from each of the 10BASE-T ports. When these pulses are received from a port, it is put into the "Link Up" state, enabling transmissions to the port, and vice versa. If the Link Integrity function is disabled, the port is forced into the Link Up state. The device generates Link Pulses to all ports, regardless of the Link State of any port or whether the Link Function is enabled or disabled.

Polarity Detection and Correction (10BASE-T ports only)

The device can detect reversed polarity on any 10BASE-T port and internally correct for it. This function can also be disabled on a port-by-port basis.

SQE Mask (AUI Port only)

Ethernet MAU devices (also known as transceivers) typically generate an SQE signal (also called heartbeat) on the CI inputs after each data transmission to the MAU. This function is normally supposed to be disabled when a MAU is attached to a repeater, but often times this is overlooked. The result can be a collision at the end of each packet transmitted. An SQE Mask function is provided to overcome this problem. When the Mask is set, SQE heartbeat signals from external MAU's will not be passed on as collisions.

Reverse AUI Mode

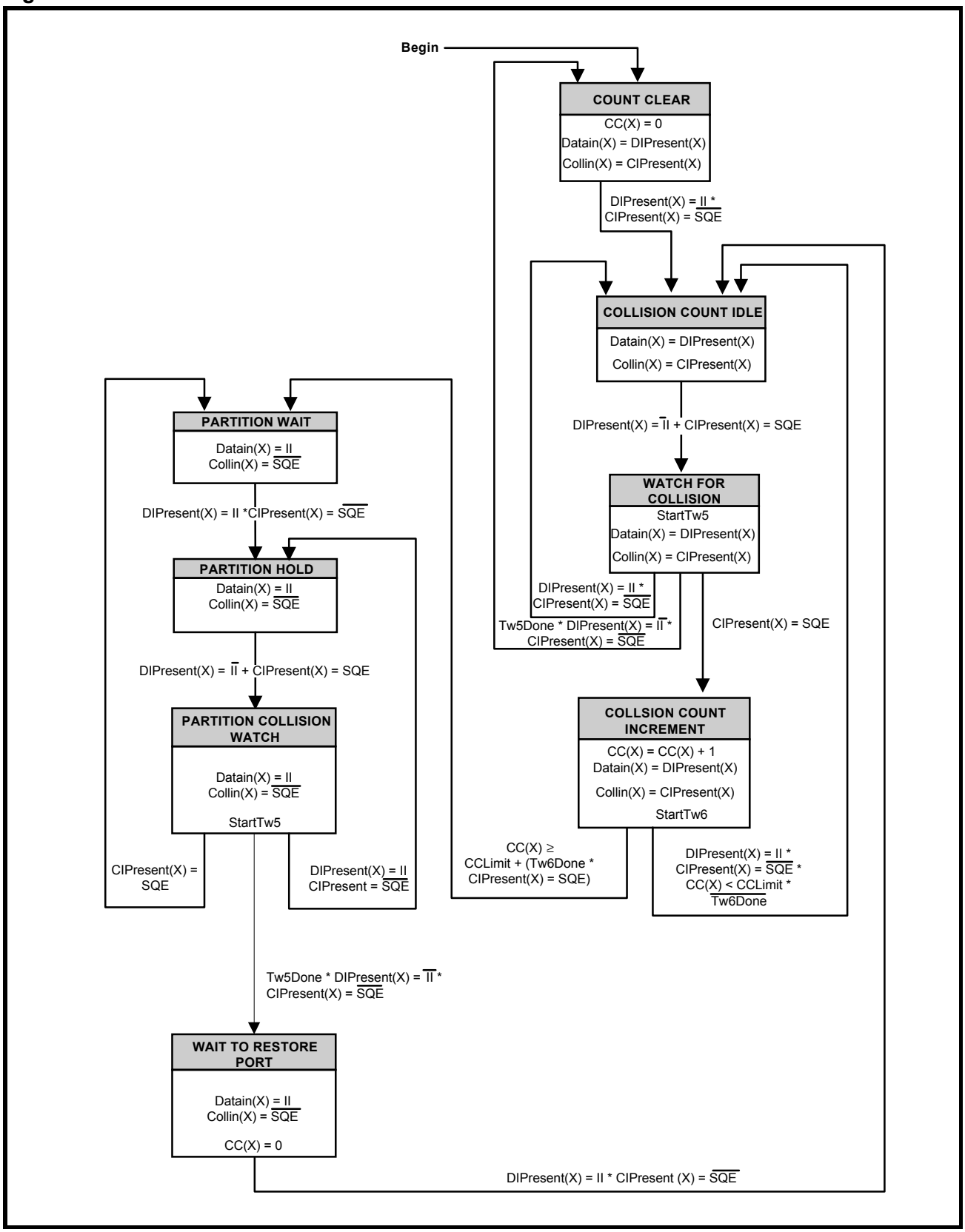
In the reverse mode, the AUI interface operates as a MAU rather than as a DTE. This allows it to directly interface to an LXT901/904/907. In this mode, the following apply:

- The CI pins function as outputs.
- The MaskSQE function determines whether or not the device generates SQE/heartbeat after each successful transmission to the device.
- The AUIDI pins continue to function as inputs, and the AUIDO pins continue to function as outputs. If these signals are being brought out to an external connector, they must be physically swapped from their normal positions (Refer to Figures 12 and 13.)
- The device will loopback data presented at the AUIDI inputs to the AUIDO outputs.

Reduced Squelch (10BASE-T ports only)

The squelch threshold on the 10BASE-T receivers can be lowered. This allows the device to detect weaker than normal signals, and can be used to support cables longer than 100m. It also makes the device more sensitive to cross-talk and other noise, and must be used with great care.

Figure 5: LXT918 Partition State Machine



LED Functions

The LXT918 provides a serial LED output and two global LEDs. Two programmable blink rates are provided. Refer to Table 49 for details.

Serial LEDs

The LXT918 provides a serial LED interface which should be attached to an external shift register. This interface provides status LEDs for the 10BASE-T and AUI ports. It also provides a global fault LED, a redundant power supply (RPS) LED and a user definable LED. Refer to Figure 18 in the Application section, and to Tables 10 and 11 below for details on the serial LED interface.

Activity and Collision LEDs (global)

These outputs can directly drive LEDs to indicate activity and collision status.

Table 10: LED-DAT Serial Port Bit Assignments

15[1]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RPS	GF	UD	AUI	TP12	TP11	TP10	TP9	TP8	TP7	TP6	TP5	TP4	TP3	TP2	TP1

1. Bit 15 is shifted out first.

Table 11: Serial LED Operational Modes

Bit	Name	Software Control	Hardware Control		
			On	Slow	Off
15	RPS	N/A	Present, No Fault	Present & Fault	Any other state
14	Global Fault	On, Off or Slow Blink via Global LED Control Register, Address 181	N/A	Any Port Partitioned or RPS Fault	Any other state
13	User Definable		N/A		
12	AUI Port LEDs	On, Off or Fast Blink, via LED Control Register, Address 176	Enabled, Link Up, Not Partitioned	Partitioned	Any other state
11:0	TP Port LEDs				

IRB Operation

The Inter Repeater Backplane (IRB) allows multiple devices to operate as a single logical repeater, exchanging data collision status information. Each segment on the LXT918 has its own complete, independent IRB. Each backplane uses a combination of digital and analog signals as shown in Figure 6. In the following discussion '*x*' is used to indicate the segment number

Data Handling

Three signals - $\overline{\text{IRENA}}x$, IRDAT*x* and IRCLK*x* - are used to transmit data. All of them can be buffered between modules. A fourth signal - $\overline{\text{IRDEN}}x$ - provides directional control of this buffer. IRDAT*x*, $\overline{\text{IRENA}}x$ and $\overline{\text{IRDEN}}x$ need to be pulled High by 330 Ω resistors. During a collision, the LXT918 releases all four signals to prevent bus contention.

Collision Handling

Four signals - $\overline{\text{IRCOL}}x$, $\overline{\text{IRCOLBP}}x$, $\overline{\text{IRCFS}}x$ and $\overline{\text{IRCFSBP}}x$ - handle collisions. $\overline{\text{IRCFS}}x$ and $\overline{\text{IRCOL}}x$ should be connected between all the devices on any module. $\overline{\text{IRCFSBP}}x$ and $\overline{\text{IRCOLBP}}x$ should be connected between modules, to the devices that have ChipID = 0.

Collision States

There are three repeater collision states:

- Receive Collision - This occurs when an external transceiver detects a collision. On the LXT918, this can only happen on the AUI port.
- Transmit Collision - This occurs when two or more inputs become active at the same time.
- One Port Left - This is a special state that can occur after a Transmit Collision, when only one port remains active. This state prevents dead-locks in multiple-repeater configurations.

Collision Indications

$\overline{\text{IRCOL}}x$ and $\overline{\text{IRCOLBP}}x$ go Low to indicate any collision (receive, transmit or one-port-left). $\overline{\text{IRCFS}}x$ and $\overline{\text{IRCFSBP}}x$ are three-state signals which are used to detect when a transmit collision occurs. The three states are:

- Idle: High (+5V) Indicates that no ports are active.
- Single drive: Mid (+2.8V) Indicates that exactly one port is active (normal data transmission, receive collision, or one-port-left).
- Multiple-drive: Low (0V). Indicates that two or more ports are active (transmit collision).

$\overline{\text{IRCFSBP}}x$ indicates the number of active drivers across all the ports in a repeater stack. $\overline{\text{IRCFS}}x$ indicates the number of active drivers on the local board, and the first 96-bits of a non-local transmit collision (defined as a collision between a local port and a non-local port, or between two non-local ports). The state of $\overline{\text{IRCFS}}x$ is fed forward to $\overline{\text{IRCFSBP}}x$ by the device with ChipID = 0. To prevent dead-locks, $\overline{\text{IRCFSBP}}x$ is NOT fed back to $\overline{\text{IRCFS}}x$. During non-local transmit collisions, the signal HOLDCOL*x* is used to hold the local devices in the transmit collision state. Table 12 summarizes the use of these signals.

Collision Hold (HOLDCOL)

Each segment can produce a HOLDCOL signal to prevent dead-locks between $\overline{\text{IRCFS}}$ and $\overline{\text{IRCFSBP}}$. The device with ChipID = 0 drives HOLDCOL High to indicate that a transmit collision is in progress, and that local devices should remain in the transmit collision state.

MAC IRB Access

The MACACTIV1:4 pins allow external MACs or other digital ASICs to interface directly to the IRB via any of the LXT918 segments. When a segment's MACACTIV pin is asserted, the LXT918 will drive the associated $\overline{\text{IRCFS}}$ and $\overline{\text{IRCFSBP}}$ signals on behalf of the external device, allowing it to participate in the transmit collision detection function of $\overline{\text{IRCFS}}$ and $\overline{\text{IRCFSBP}}$.

IRB Isolation

The ISOLATE1:4 outputs are provided to control the enable pins of external bidirectional transceivers. In multi-module applications, they can be used to isolate one module from the rest of the system. Only one device can control these signals. The output states of these pins are controlled by the Isolate bits in the Master Configuration Register.

MMSTRIN / MMSTROUT

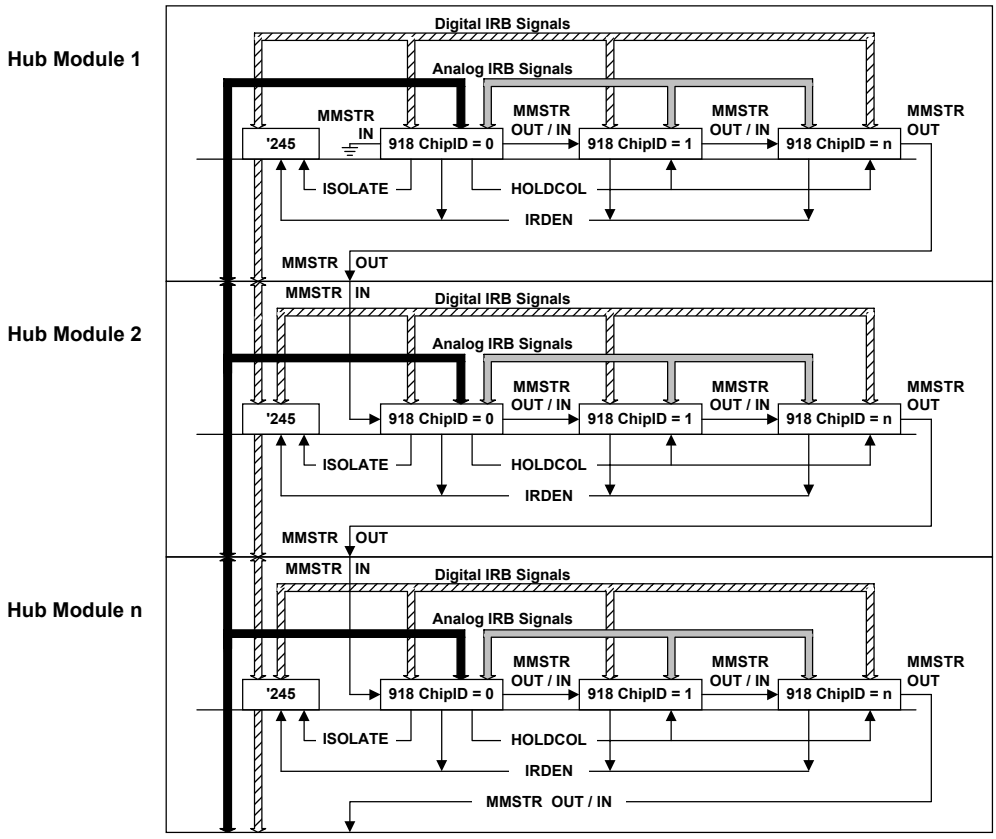
This daisy chain is provided for correct gathering of statistics in multiple-device configurations. In multiple-module applications, this daisy chain must be maintained across modules. In stand-alone applications, or for the first device in a chain, the MMSTRIN input must be pulled Low in order for the management counters to work correctly.

Table 12: $\overline{\text{IRCOL}}$ and $\overline{\text{IRCFS}}$ Condition Indications

Condition	$\overline{\text{IRCOLBP}}$	$\overline{\text{IRCOL}}$	$\overline{\text{IRCFSBP}}$[3]	$\overline{\text{IRCFS}}$[3]
Idle	High	High	High	High
Local Data	High	High	Mid	Mid
Non-Local Data	High	High	Mid	High
Local RxCol or OPL [1]	Low	Low	Mid	Mid
Non-local RxCol/OPL [1]	Low	Low	Mid	High
Local TxCol or first 96 bits of non-local TxCol [2]	Low	Low	Low	Low
Non-local TxCol after 96 bits [2]	Low	Low	Low	Mid or High

1. Receive Collision (RxCol) and One Port Left (OPL) conditions have identical bus characteristics and can be differentiated only by timing. Fragment extensions are generally treated as receive collisions.
2. Manchester code violations and FIFO overruns are generally treated as transmit collisions.
3. Signal employs 3-state logic: High = 5V; Mid = 2.8V; Low = 0V.

Figure 6: IRB Block Diagram



This diagram shows a single IRB. The LXT918 actually has four independent IRBs, one per segment.

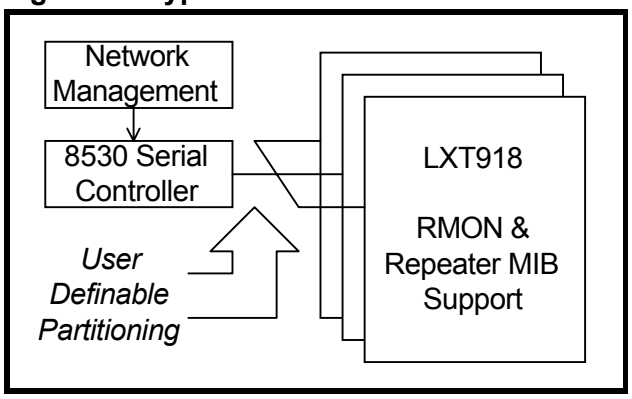
- Digital IRB signals include IRDAT, IRENA and IRCLK.
- Local Analog IRB signals include IRCOL and IRCFS.
- Inter-Module Analog IRB signals include IRCOLBP and IRCFSBP.

Serial Management Interface

The serial management interface provides access to Repeater MIB variables, RMON Statistics attributes and status and control information. A network manager can access the interface through a simple serial communications controller. The interface is designed to be used in a multi-drop configuration, allowing multiple LXT918 devices to be managed from one common line.

The interface consists of a data input line (SRX), data output line (STX) and a clock (SERCLK), and can operate up to 1 Mbps. The interface operates on a simple command response model, with the network manager as the master and the LXT918 devices as slaves. Figure 7 is a simplified view of typical serial management interface architecture.

Figure 7: Typical Serial I/F Architecture



Serial Clock

SERCLK is a bidirectional pin; direction control is provided by the RECONFIG input. If RECONFIG is High, the LXT918 will drive SERCLK at 625 kHz. If RECONFIG is Low, SERCLK is an input, between 0 and 1 MHz. There is no lower bound to how slow the interface can operate. The clock can be stopped after each operation, as long as an idle (ten 1's in a row) is transmitted first.

Serial Data I/O

The serial data pins, SRX and STX, should be tied together. The SRX input is compared with the STX output. If a mismatch occurs, STX goes to a high impedance. STX is driven on the falling edge of SERCLK; SRX is sampled on the rising edge.

Management Format

Normally the network manager directs read and write operations to a specific LXT918 device using a two-part address consisting of HubID and ChipID. The interface allows up to 127 32-bit registers to be read at one time. Up to two registers can be written at a time.

The interface uses a simple frame format, which is shown in Figure 8. All frames begin and end with a flag of consisting of "01111110". All fields are transmitted LSB first. Zero-bit stuffing is required if more than five 1's in a row appear in the header, data or CRC fields. In addition, all operations directed to the device must be followed by an idle (ten 1's in a row), and the first operation must be preceded with an idle.

Figure 8: Serial Management Frame Format

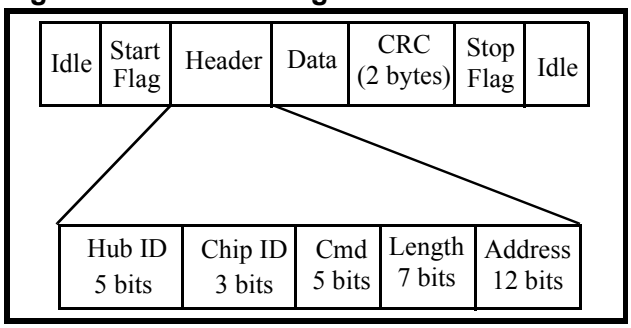


Table 13: Serial Management Frame Message Fields

Message	Description
Start or Stop Flag	"01111110". Protocol requires zero insertion after any five consecutive "1's" in the data stream.
Hub ID	Identifies module or sub-system. Assigned by one of two arbitration mechanisms at power-up.
Chip ID	Identifies one of eight modules on a system. Assigned by 3 external pins on each device.
Command	Identifies the particular operation being performed (see Table 14)
Length	Specifies number of registers to be transferred (1 to 127). Maximum is 2 per write, 127 per read.
Address	Specifies address of register or register block to be transferred.

1. All fields are transmitted LSB first.

Table 14: Serial Management Instruction Set

Command Value	Name	Usage	Normally Sent By	Description
18 (Hex)	Write	Normal Ops	Network Mgr	Used to write up to 2 registers (8 bytes) at a time.
04 (Hex)	Read	Normal Ops	Network Mgr	Used to read up to 127 registers at a time.
08 (Hex)	RequestID	Arbitration	LXT918	Requests Hub ID. Repeated periodically.
00 (Hex)	ConfigChg	Arbitration	LXT918	Notifies system of configuration change (hot swap). Requests new arbitration phase.
10 (Hex)	Re-arbitrate	Arbitration	Network Mgr	Re-starts arbitration
14 (Hex)	Assign HubID	Arbitration Mech. 2	Network Mgr	Assigns Hub ID to device with ARBIN=0 and ARBOUT = 1 (top of chain)
0C (Hex)	Set ARBOUT to 1	Arbitration Mech. 2	Network Mgr	Commands specific device to set ARBOUT to 1.
1C (Hex)	Set ARBOUT to 0	Arbitration Mech. 2	Network Mgr	Commands specific device to set ARBOUT to 0
02 (Hex)	DevID	Config	Network Mgr	Generic command for reading device type (no register address needed).

Table 15: Typical Serial Management Packets

Message	Contents of Fields in Serial Management Packet					
	Hub ID	Chip ID	Command	Length	Address	Data
Write	User Defined	User Defined	18 (Hex)	01 or 02	User Defined	User Defined
Read Request	User Defined	User Defined	04 (Hex)	01 to 7F Hex	User Defined	Null
Read Response	00000	000	04 (Hex)	Echo	Echo	Data Values
Assign Hub ID (Arb Method 1)	11111	111	18 (Hex)	02	188 Hex	Formatted per Table 51
Assign Hub ID (Arb Method 2)	11111	111	14 (Hex)	01	0	Hub ID (LSB) and 27 0's
Set ARBOUT To 1	User Defined	User Defined	0C (Hex)	00	0	Null
Arb Request	00000	000	08 (Hex)	02	190	PROM ID
Re-Arbitrate	11111	111	10 (Hex)	00	0	Null
Request Device ID	User Defined	User Defined	02 (Hex)	01	0	Null
Device ID Response	00000	000	02 (Hex)	01	185	Formatted per Table 50
Config Change	thirteen 0's					

AUI Configuration Register

The AUI Configuration Register (Address 184) operates differently from the rest of the Serial Management Interface. This 16-bit register is loaded from an external shift register which can be implemented using a pair of LS'165 devices. Three dedicated pins: AUICONFIG_IN, CONFIG_CLK and CONFIG_ENA are used to load the register (refer to Table 2 for pin

assignments and signal descriptions). Bits 15:1 may be used to hold up to 15 bits of user-defined board or system configuration data.

Bit 0 (LSB) sets the AUI port operating mode as follows:

- 0 = Normal (DTE) mode
- 1 = Reversed (MAU) mode

Two events cause shift register data to be loaded into the AUI Configuration Register: reset/power-up and a management read of Register 184. To load new data into the register, two reads are required. The first read reflects the initial content and causes the register to shift in data from AUICONFIG_IN. The new data will be reflected in the second read.

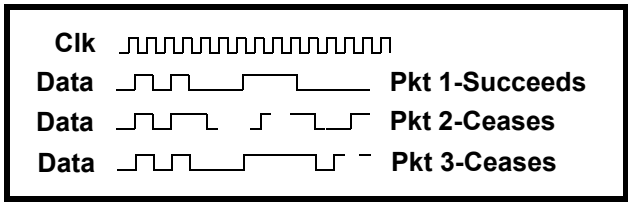
Address Arbitration

Each device has a two part address, consisting of a HubID and a ChipID. The ChipID is assigned the input pins CHIPID<2:0>. The HubID is assigned through one of two arbitration mechanisms.

Arbitration Mechanism #1: EPROM Method

This method requires that a PROM be located on each module, and that the ARBSELECT pin (71) not be pulled Low. At power-up, the device with ChipID = 0 reads a 48-bit ID from the PROM. All other devices on the module listen in and also record this ID. The device with ChipID = 0 then transmits "Arbitration Request Messages" on the Serial Management Interface every 2-3 milliseconds. The request messages from two modules may collide; if this happens a resolution scheme ensures that only one message will win (see Figure 9). The network manager responds to each request with a message that includes the 48-bit ID and the HubID. All devices hear this message, but only those that match the 48-bit ID receive the HubID as their own. Once the HubID is assigned, the device with ChipID=0 stops sending request messages. It is possible for response messages to be lost due to collisions with request messages.

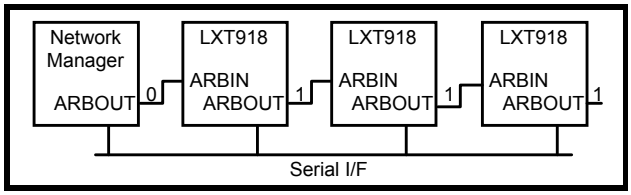
Figure 9: Arbitration Mechanism #1 : Collision Resolution



Arbitration Mechanism #2: Chain Method

In this method, all of the devices are daisy-chained using the ARBIN and ARBOUT pins as shown in Figure 10. The ARBIN input of the first device is directly connected to an output of the network manager. At power-up all the devices drive their ARBOUT outputs High while the network manager drives the ARBIN input to the first device Low. The manager transmits a special "Assign Hub ID" message which is recognized only by the device with ARBIN = Low and ARBOUT = High. The network manager then sends a command addressed to this device which commands it to set its ARBOUT pin Low. This cycle repeats until all devices have been assigned a HubID.

Figure 10: Arbitration Mechanism #2: ARBIN/OUT Chain Links



Address Re-arbitration

There are two mechanisms for address re-arbitration following a configuration change, such as a module hot-swap:

- Device power up - At power-up, the LXT918 normally sends out a "Configuration Change" message (all 0's) on the bus, which causes re-arbitration.
- The network manager can direct or re-start arbitration at any time by sending the "Re-arbitrate" command.

Source Address Utilities

Source Address Tracking Function

Each port has two source address tracking registers. The rptrAddrTrackNewLastSrcAddress register for each port continuously tracks the source addresses of packets emanating from that port. The Authorized Address Register operates in three modes: it can free run, lock, or lock on the next packet. In any mode, it can always be updated by network management.

Source Address Matching Function

Each segment has a Source Address Matching Function to discover which port or ports sourced packets with a particular Source Address. The input to the function is an Ethernet Address; the output is a register which identifies any ports that sourced packets with that Source Address.

APPLICATION INFORMATION

Magnetics Information

The LXT918 requires a 1:1 ratio for the TP receive transformers and a 1:1.41 ratio for the TP transmit transformers. Table 16 lists suitable transformers by manufacturer and part number. This information was valid as of the printing date of this document. Before committing to a specific component, designers should contact the manufacturer for current product specifications, and should test and validate the magnetics for the specific application to verify that system requirements are met.

Layout Requirements

The Twisted Pair Interface

The layout of the twisted-pair port is critical in complex designs. Run the traces directly from the LXT918 to the discrete termination components (located close to the transformers).

The transformer isolation voltage should be rated at 2 kV to protect the circuitry from static voltages across the connectors and cables. The traces running from the transformers to the connector should run in close pairs directly to the connector. Be careful not to cross the transmit and receive pairs. One way to avoid this problem is to run the receive pairs on the component side and the transmit pairs on the solder side. Careful planning during the schematic and layout stages can avoid these problems.

The PCB layout should have no ground or power planes between the transformers and the connectors. The data signals should be the only traces in this area. Place the chassis ground for the connectors near the edge of the PCB, away from the signals, connecting the connector shield with the chassis.

The RBIAS Pin

The RBIAS signal sets the levels for the output drivers. Any emissions or common mode noise entering the device here could be measured on the twisted pair output signals.

The LXT918 requires a 22 kΩ, 1% resistor directly connected between the RBIAS pin and ground. These traces should be as short as possible. The ground traces from adjacent GND pins should come directly off of the device to enclose the resistor and pin forming a shielded area between the RBIAS connection and other signals on the PCB.

Typical Application Circuitry

Figures 11 through 19 show typical LXT918 application circuitry. Table 17 summarizes signal operation of the three AUI signal pairs in the two modes (normal and reversed).

Table 16: Suggested Magnetics List[1]

Manufacturer	Quad Transmit	Quad Receive	Quad Tx/Rx (Octal)
BEL	S553-5999-02	S553-5999-03	
HALO	TD54-1006L1 TG54-1006N2	TD01-1006L1 TG01-1006N2	TG44-S010NX TG45-S010NX TG46-S010NX
Nanopulse	5976	5977	
Kappa	TP4003P	TP497P101	
PCA	EPE6009	EPE6010	
TDK	TLA-3T107	TLA-3T106	
VALOR	PT4116	PT4117	

1. Before committing to a specific component, designers should contact the manufacturer for current product specifications, and should test and validate the magnetics for the specific application to verify that system requirements are met.

Figure 11: Typical 10BASE-T Port Interface

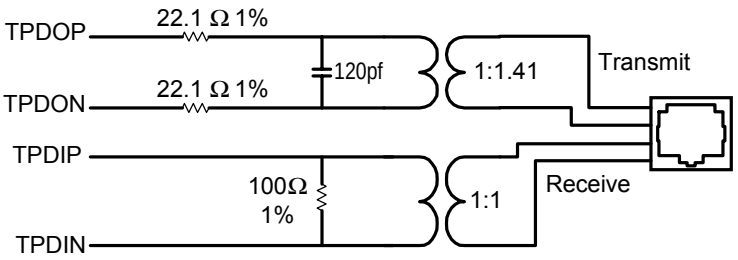


Figure 12: Normal AUI Circuit

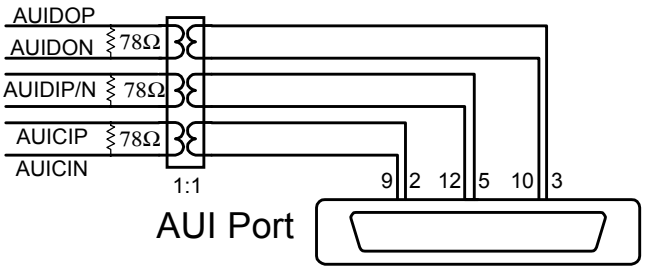


Figure 13: Reversed AUI Circuit

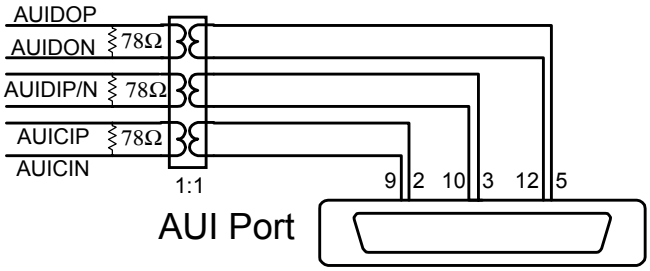


Table 17: AUI Signals - Direction and Pin-Out

LXT918		AUI Connector Pin #	
Signal	**Pin #**	**Normal**	**Reversed**
DOP	198	3	5
DON	199	10	12
DIP	200	5	3
DIN	201	12	10
CIP	202	2	2
CIN	203	9	9

Figure 14: Typical IRB Implementation

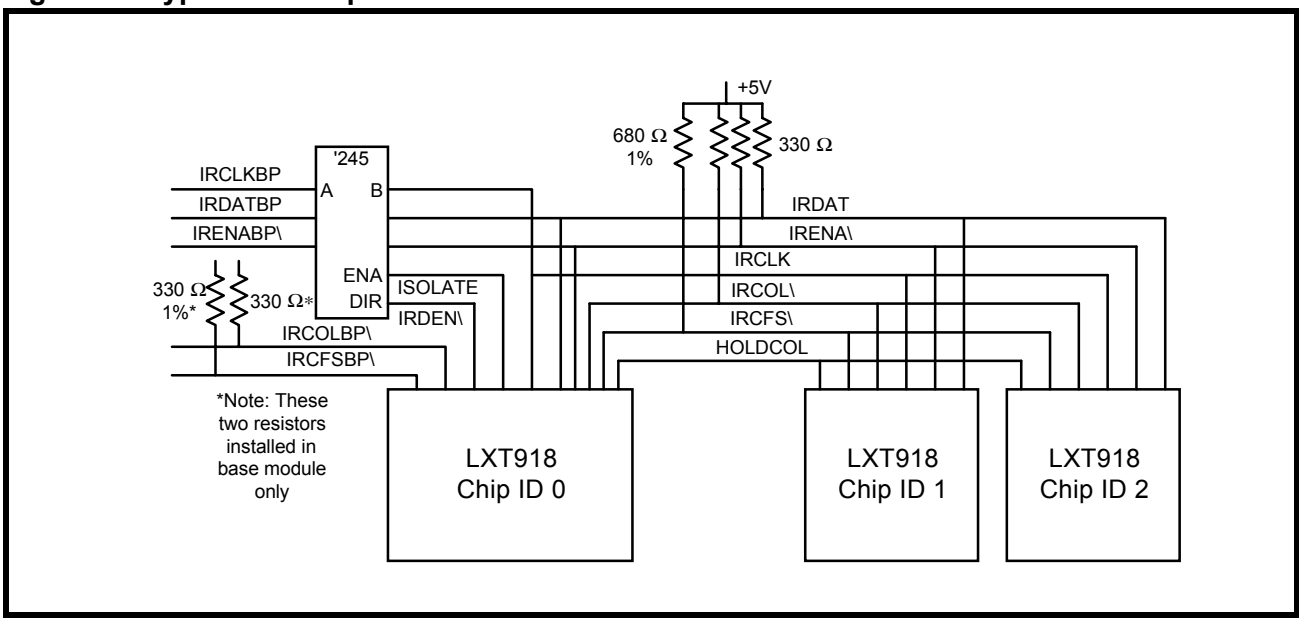


Figure 15: Typical Serial Management Interface Connections

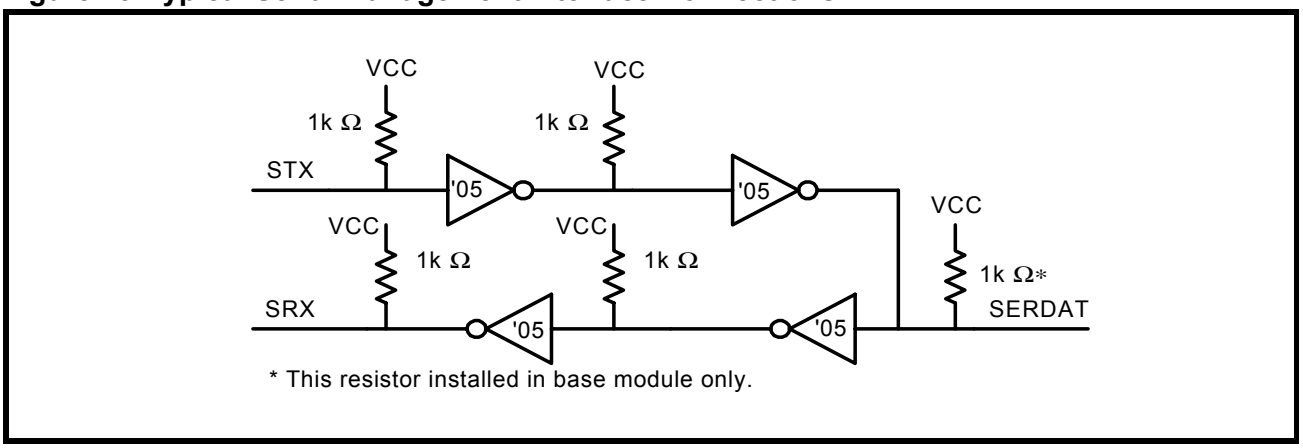


Figure 16: Typical Chip ID Architecture

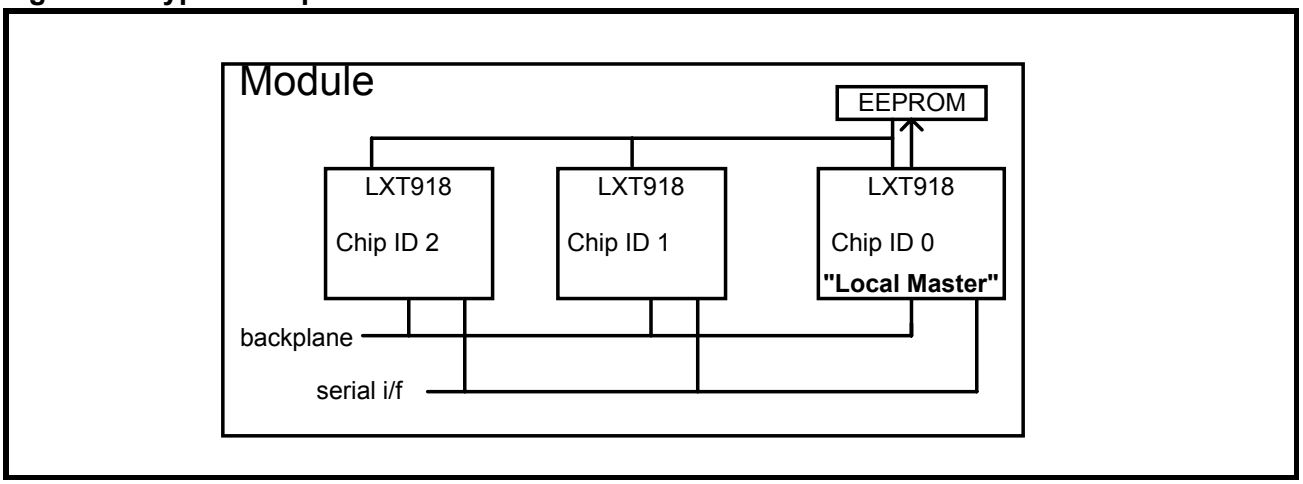


Figure 17: Typical EPROM Circuit

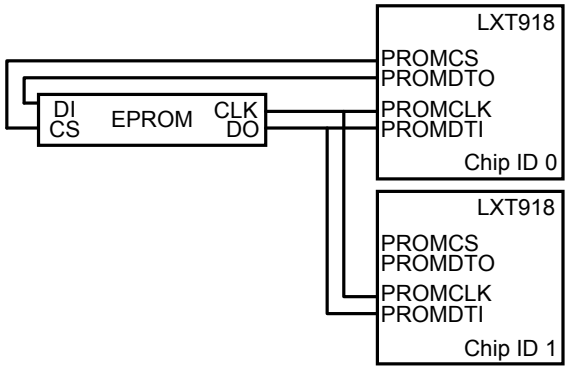


Figure 18: Typical Serial LED Interface Circuit

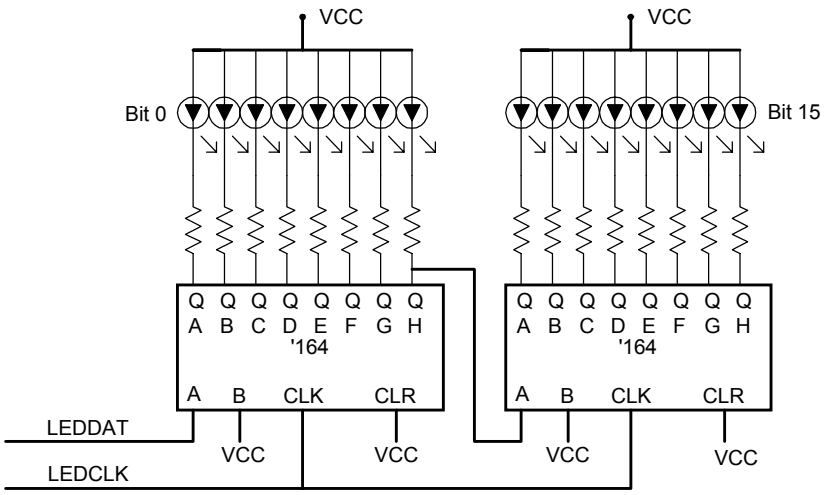
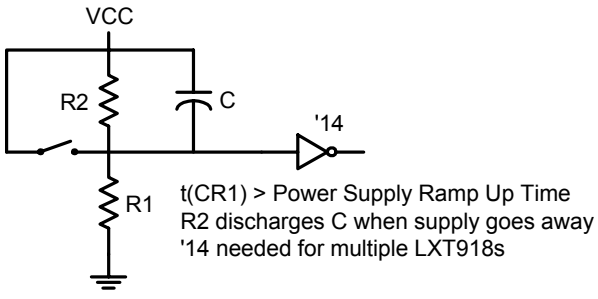


Figure 19: Typical $\overline{\text{RESET}}$ Circuit



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 18 through 28 and Figures 20 through 24 represent the performance specifications of the LXT918 and are guaranteed by test, except where noted by design

Table 18: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply voltage	VCC	-0.3	6	V
Operating temperature	TOP	0	70	ºC
Storage temperature	TST	-65	+150	ºC

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19: Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Recommended supply voltage[1]	VCC	4.75	5.0	5.25	V	
Recommended operating temperature	TOP	0	–	70	ºC	
VCC current	ICC	–	400	–	mA	

1. Voltages with respect to ground unless otherwise specified.

Table 20: I/O Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	VIL	–	–	0.8	V	TTL inputs
		–	–	2.0	V	CMOS inputs [2]
		–	–	1.0	V	Schmitt Trigger #1
		–	–	1.0	V	Schmitt Trigger #2
Input High voltage	VIH	2.0	–	–	V	TTL inputs
		VCC-2.0	–	–	V	CMOS inputs [2]
		VCC-1.0	–	–	V	Schmitt Trigger #1
		VCC-2.0	–	–	V	Schmitt Trigger #2
Hysteresis voltage	–	1.0	–	–	V	Schmitt Trigger #1
		0.5	–	–	V	Schmitt Trigger #2

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Does not apply to IRB pins. Refer to Table 23 for IRB I/O characteristics.

Table 20: I/O Electrical Characteristics (Over Recommended Range) – continued

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage	VOL	–	–	0.4	V	IOL = 1.6 mA
Output Low voltage (LED)	VOLL	–	–	1.0	V	IOLL = 10 mA
Output High voltage	VOH	2.4	–	–	V	IOH = 40 µA
Input Low current	IIL	-100	–	–	µA	
Input High current	IIH	–	–	100	µA	
Output rise / fall time	–	–	3	10	ns	CLOAD = 15 pF

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Does not apply to IRB pins. Refer to Table 23 for IRB I/O characteristics.

Table 21: 10BASE-T Electrical Characteristics (Over Recommended Range)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmitter	Transmit output impedance	ZOUT	–	2	–	Ω	
	Peak differential output voltage	VOD	2.2	2.5	2.8	V	Load = 100Ω at TPOP/ TPON
	Transmit timing jitter addition	–	–	±2	±10	ns	0 line length for internal MAU
	Transmit timing jitter added by the MAU and PLS sections	–	–	±1	±5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU
Receiver	Receive input impedance	ZIN	20	36	–	kΩ	Between TPIP/TPIN
	Differential squelch threshold - Normal	VDSN	300	420	585	mV	5 MHz square wave input
	Differential squelch threshold - Reduced	VDSR	150	250	350	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 22: AUI Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Differential output voltage	VOD	±550	–	±1200	mV	
Receive input impedance	ZIN	20	36	–	kΩ	Between CIP/CIN & DIP/DIN
Differential squelch threshold	VDS	150	250	350	mV	

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 23: IRB Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage	VOL	–	.3	.7	V	RL = 330 Ω
Output rise or fall time	TF	–	4	10	ns	CL = 15 pF
Input High voltage	VIH	VCC - 2.0	–	–	V	CMOS inputs
Input Low voltage	VIL	–	–	2.0	V	CMOS inputs
$\overline{\text{IRCFS}}$ current	–	2.6	3.3	4.0	mA	RL = 680 Ω
$\overline{\text{IRCFSBP}}$ current	–	5.4	6.7	8.3	mA	RL = 330 Ω

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 24: Repeater Timing Characteristics[1] (Over Recommended Range)

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
AUI DIN active to $\overline{\text{IRENA}}$ Low	trep1	–	2	3	BT[4]	
TP DIN to $\overline{\text{IRENA}}$ Low	trep2	–	5	7	BT	
$\overline{\text{IRENA}}$ Low to AUI DOP active	trep3	–	3	4	BT	
$\overline{\text{IRENA}}$ Low to TP DOP active	trep4	–	4	5	BT	
IRCLK rising edge to IRDAT rising edge.	trep5	25	–	55	ns	330 Ω pullup, 150 pF load on IRDAT. 1k Ω pullup, 150 pF load on IRCLK. All measurements at 2.5V.
IRCLK rising edge to IRDAT falling edge.	trep6	5	–	25	ns	
AUI DIN idle to $\overline{\text{IRENA}}$ High	trep7	–	–	8	BT	
TP DIN idle to $\overline{\text{IRENA}}$ High	trep8	–	–	11	BT	
$\overline{\text{IRENA}}$ High to AUI DOP idle	trep9	–	–	5	BT	
$\overline{\text{IRENA}}$ High to TP DOP idle	trep10	–	–	5	BT	

1. This table contains propagation delays from the TP and AUI ports to the IRB, and from the IRB to the AUI and TP ports, for normal repeater operation (start of packet, end of packet). All values in this table are output timings.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
3. There is a delay of approximately 13 to 16 bit times between the assertion of $\overline{\text{IRENA}}$ and the assertion of IRCLK and IRDAT. This delay does not affect repeater operation because downstream devices begin generating preamble as soon as $\overline{\text{IRENA}}$ is asserted.
4. BT = Bit Times (100 ns).

Figure 20: Repeater Timing

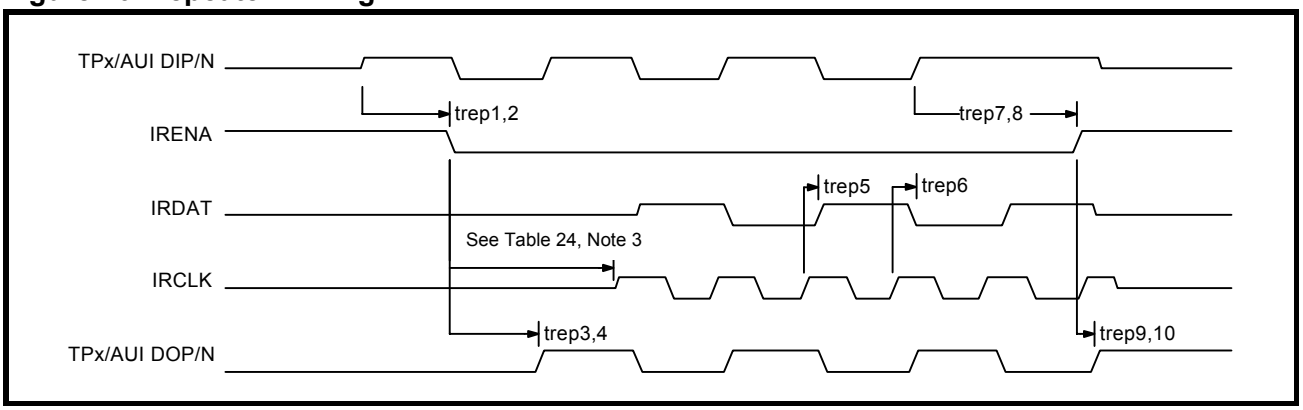


Table 25: MAC Interface Transmit Timing Characteristics [1] (Over Recommended Range)

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
TXD to TXC setup time	tmactx1	20	–	–	ns	TXD valid to TXC rising edge [3]
TXC to TXD hold time	tmactx2	5	–	–	ns	TXC rising edge to TXD change [3]
TXE to TP DOP prop delay	tmactx3	–	6	7	BT	TXE High to TPDOP active [4]

1. This table contains propagation delay times for the 7-pin MAC interface.
2. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
3. Input.
4. Output.

Figure 21: MAC Interface Transmit Timing

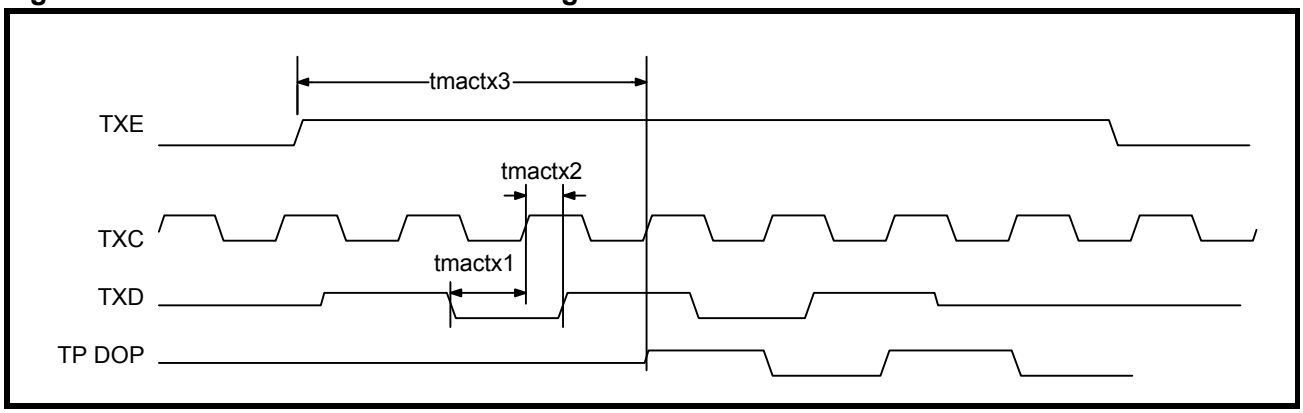


Table 26: MAC Interface Receive Timing Characteristics [1] (Over Recommended Range)

Parameter	Symbol	Min	Typ[2]	Max	Units	Test Conditions
RXC to RXD prop delay	tmacrx1	–	–	10	ns	Falling edge of RXC to RXD valid
TP/AUI to CRS delay	tmacrx2	–	9	10	BT	TP/AUI DIP active to CRS High
Number of extra receive clocks	tmacrx3	–	5	–	ea	RXC rising edges after CRS Low

1. This table contains propagation delay times for the 7-pin MAC interface outputs.
2. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Figure 22: MAC Interface Receive Timing

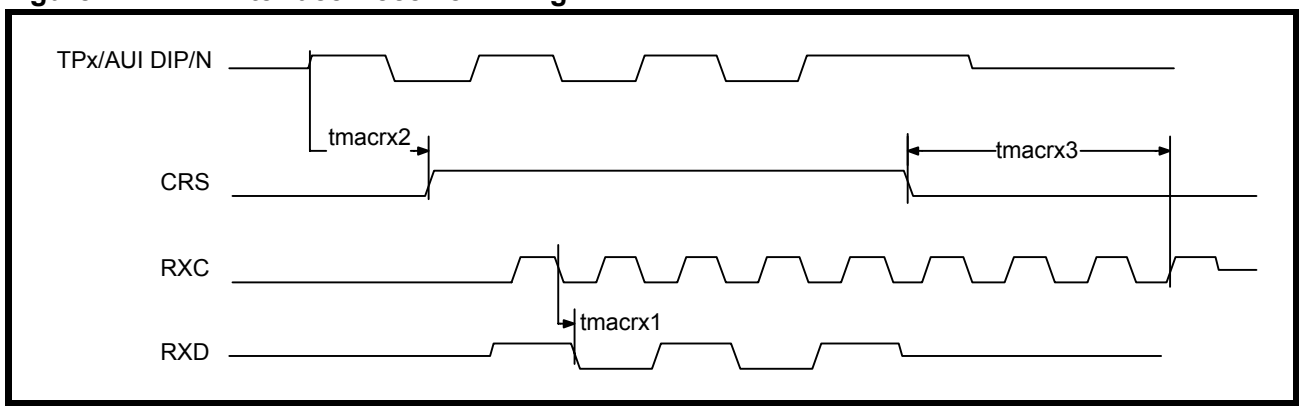


Table 27: MACACTIVE Delays - MAC/IRB Interface Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
MACACTIV to $\overline{\text{IRENA}}$ assertion delay [3]	tmacbp1	–	100	–	ns	MACACTIV High to $\overline{\text{IRENA}}$ Low [2]
IRDAT to IRCLK setup time	tmacbp2	21	–	–	ns	IRDAT valid to IRCLK rising edge [2]
IRDAT to IRCLK hold time	tmacbp3	0	–	–	ns	IRCLK rising edge to IRDAT change [2]

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Input.
3. External devices should allow at least one 10 MHz clock cycle (10 ns) between assertion of MACACTIV and $\overline{\text{IRENA}}$.

Figure 23: MACACTIVE Timing (MAC to IRB Interface)

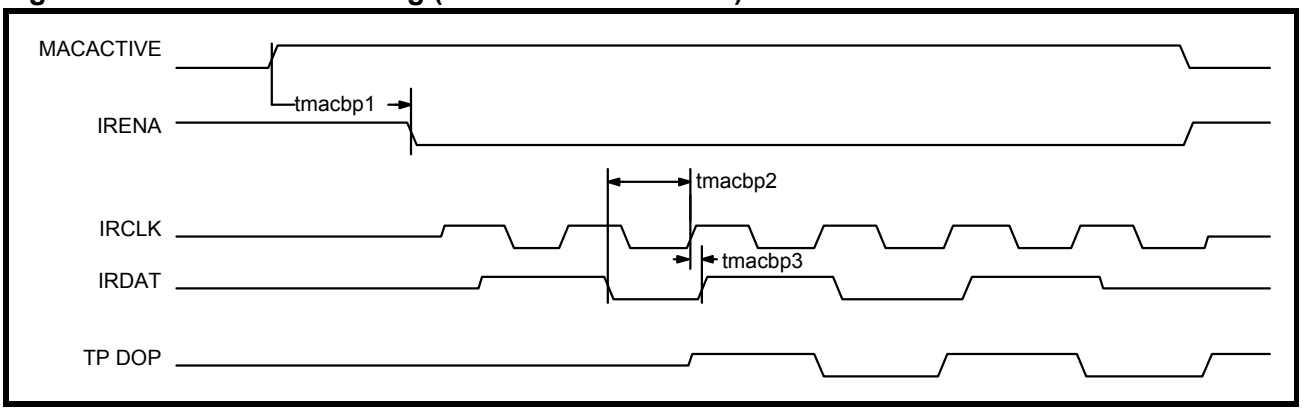
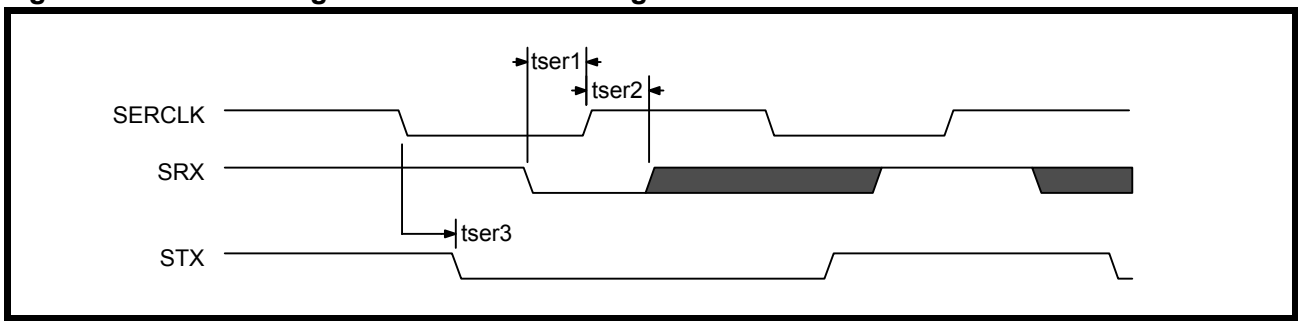


Table 28: Serial Management Interface Timing Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Data to Clock setup	tser1	100	–	–	ns	SRX valid to SERCLK rising edge [2]
Clock to Data Hold Time	tser2	100	–	–	ns	SERCLK rising edge to SRX change [2]
Data Propagation Delay	tser3	–	–	100	ns	SERCLK falling edge to STX valid [3]

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Input.
3. Output.

Figure 24: Serial Management Interface Timing



REGISTER DEFINITIONS

Introduction

The LXT918 register set is composed of multiple 32-bit registers (and a single 16-bit register) of the following types:

- Configuration Registers
- Control and Status Registers
- Ethernet Address Registers
- Counters

Table 29 lists the register base memory locations. Refer to Tables 30 through 54 for specific addresses and bit assignments. *Note that all register addresses are specified in hexadecimal*

Table 29: Memory Map

Base Address	Register Type	Notes
184	AUI Configuration	1 Register. This is the only 16-bit register in the LXT918. The AUI Configuration Register is loaded from an external shift register and may be read via the Serial Management Port.
181	Configuration	11 Registers
170	Control and Status	9 Control Registers, 7 Status Registers
156	Ethernet Address	12 Search Registers
13C		Authorized Port Address, 2 per port (TP and AUI)
120		Port Address Tracking, 2 per port (TP, AUI and MAC)
118	Counters	MAC Interface Counters, 8 Registers
100		Segment 4 Interface Counters, 18 Registers
0F0		Segment 3 Interface Counters, 18 Registers
0E0		Segment 2 Interface Counters, 18 Registers
0D0		Segment 1 Interface Counters, 18 Registers
0C0		AUI Port Counters, 15 Registers
0B0		TP Port 12 Counters, 15 Registers.
0A0		TP Port 11 Counters, 15 Registers.
090		TP Port 10 Counters, 15 Registers.
080		TP Port 9 Counters, 15 Registers.
070		TP Port 8 Counters, 15 Registers.
060		TP Port 7 Counters, 15 Registers.
050		TP Port 6 Counters, 15 Registers.
040		TP Port 5 Counters, 15 Registers.
030		TP Port 4 Counters, 15 Registers.
020		TP Port 3 Counters, 15 Registers.
010		TP Port 2 Counters, 15 Registers.
000		TP Port 1 Counters, 15 Registers.

Counter Registers

As shown in Table 30, all counters are 32-bit, read-only, “little-Endian” registers, with undetermined values at power-up. The “Zero Counters” bit in the Master Configuration Register allows all counters to be “zeroed”.

Table 30: Counter Registers Bit Assignments

31	30	29	28	27	26	25 : 7	6	5	4	3	2	1	0
D31	D30	D29	D28	D27	D26	D25:D7	D6	D5	D4	D3	D2	D1	D0

Port Counter Registers

Table 31 contains descriptions of the per-port counters for the TP ports and the AUI port. These descriptions are intended to be illustrative. For the exact definitions of these counters, refer to the Repeater MIB, RFC 1516. To obtain the address of a particular register for a particular port, add the offset value for the register (from Table 31) to the base address for that port (from Table 29).

Table 31: Port Counter Registers

Name	Offset	Description[1]
rptrMonitorPortReadableFrames	0	Counts valid-length (64 to 1518 bytes), valid-CRC, collision-free packets. Depending on the state of the CountMode bit in the Master Configuration Register, this counter will count either all packets (CountMode=0) or only Unicast Packets (CountMode=1) Minimum roll-over time = 80 hours
rptrMonitorPortReadableOctets	1	Counts the number of octets in the packets counted by the rptrMonitor-PortReadableFrames counter, not including preamble and framing bits. Minimum roll-over time = 58 minutes.
rptrMonitorPortFrameCheckSe-quence	2	Counts valid length, collision-free packets that had FCS errors, but were correctly framed (had an integral number of octets). Minimum roll-over time = 80 hours.
rptrMonitorPortAlignmentErrors	3	Counts valid length, collision-free packets that had FCS errors and were incorrectly framed (had a non-integral number of octets) . Minimum roll-over time = 80 hours.
rptrMonitorPortFramesTooLong	4	Counts packets that had a length greater than 1518 octets. Minimum roll-over time = 61 days.
rptrMonitorPortShortEvents	5	Counts events that lasted for 82 bit times or less. Minimum roll-over time = 16 hours.
rptrMonitorPortRunts	6	Counts events longer than 82 bit times, but shorter than 512 bit times. Minimum roll-over time = 16 hours.
rptrMonitorPortCollisions	7	Counts the number of collisions that occurred, not including late colli-sions. Minimum roll-over time = 16 hours.
rptrMonitorPortLateEvents	8	Counts the number of times collision was detected more than 512 bit times after the start of carrier. Minimum roll-over time = 81 hours.

1. All Port Counters are Read Only.

Table 31: Port Counter Registers – continued

Name	Offset	Description[1]
rptrMonitorPortVeryLongEvents	9	Counts the number of times any activity continued for more than 4 to 7.5 ms. Minimum roll-over time = 198 days.
rptrMonitorPortDataRateMismatches	A	Counts the number of times the incoming data rate mismatched the local clock source enough to cause a FIFO underflow or overflow.
rptrMonitorPortAutoPartitions	B	Counts the number of times this port has been partitioned by the Auto-partition algorithm.
rptrTrackSourceAddrChanges	C	Counts the number of times the source address has changed. Minimum roll-over time of 81 hours.
rptrMonitorPortBroadcastPkts	D	Counts the number of good broadcast packets received by this port.
rptrMonitorPortMulticastPkts	E	Counts the number of good multicast packets received by this port.

1. All Port Counters are Read Only.

Interface Counter Registers

Table 32 contains descriptions of the segment counters, which are intended to be illustrative. For the exact definition of these counters, refer to the RMON MIB, RFC 1757. To arrive at the address of a particular register for a particular segment, add the offset for that register (shown below) to the base address for the segment (refer to Table 29), except for repeaterMonitorTotalOctets and repeaterMonitorTotalCollisions.

Table 32: Interface Counter Registers

Name	Offset[1]	Description[2]
etherStatsOctets	0	The number of data octets including those in bad packets and octets in FCS fields, but does not include preamble or other framing bits.
etherStatsPkts	1	The number of packets received from the network, including errored packets.
etherStatsBroadcastPkts	2	The number of good broadcast packets received.
etherStatsMulticastPkts	3	The number of good multicast packets received.
etherStatsCRCAlignErrors	4	The number of valid-length packets (64 to 1518 bytes inclusive) that had a bad Frame Check Sequence (FCS).
etherStatsUndersizePkts	5	The number of well-formed packets that were smaller than 64 octets.
etherStatsOversizePkts	6	The number of well-formed packets that were longer than 1518 octets.
etherStatsFragments	7	The number of ill-formed packets less than 64 octets. Note: Any event without a start-of-frame delimiter (0-octet packet) will be counted as a fragment, no matter how long it is.
etherStatsJabbers	8	The number of ill-formed packets longer than 1518 octets. An ill-formed packet is one with an FCS error.
etherStatsCollisions	9	The best estimate of the total number of collisions on this interface.
etherStatsPkts64Octets	A	The number of packets (good and bad) that were 64 octets long.
etherStatsPkts65to127Octets	B	The number of packets (good and bad) between 65 and 127 octets long.

1. Absolute addresses are given for repeaterMonitorTotalOctets and repeaterMonitorTotalCollisions
2. All Interface Counters are Read Only

Table 32: Interface Counter Registers – continued

Name	Offset[1]	Description[2]
etherStatsPkts128to255Octets	C	The number of packets (good and bad) between 128 and 255 octets long.
etherStatsPkts256to511Octets	D	The number of packets (good and bad) between 256 and 511 octets long.
etherStatsPkts512to1023Octets	E	The number of packets (good and bad) between 512 and 1023 octets long.
etherStatsPkts1024to1518Octets	F	The number of packets (good and bad) between 1024 and 1518 octets long.
rptrMonitorTotalOctets	110 (Seg 1) 111 (Seg 2) 112 (Seg 3) 113 (Seg 4)	These per-segment counters record the total number of octets received on each interface.
rptrMonitorTransmitCollisions	114 (Seg 1) 115 (Seg 2) 116 (Seg 3) 117 (Seg 4)	These per-segment counters record the total number of transmit collisions that occurred each interface.

1. Absolute addresses are given for repeaterMonitorTotalOctets and repeaterMonitorTotalCollisions
2. All Interface Counters are Read Only

Port Counters for the 7-pin MAC Interface

Port Counters for the 7-pin MAC Interface are described in Table 33. These counters are a subset of the port counters for the other ports. Refer to Table 30 for bit assignments.

Table 33: MAC Interface Registers

Name	Type[1]	Addr	Description
MAC Interface-Readable-Frames	R	118	Valid-length (64 to 1518 bytes), valid-CRC, non-collision frames. Depending on the state of the CountMode bit in the Master Configuration Register, this counter counts either all valid packets (CountMode=0) or Unicast packets only (CountMode=1). Minimum roll-over time = 80 hours.
MAC Interface-Readable-Octets	R	119	Octets contained in MAC Interface-ReadableFrames. Minimum roll-over time = 58 minutes.
MAC Interface-Runts	R	11A	Number of packets and events shorter than 512 bit times. Minimum roll-over time = 16 hours.
MAC Interface-Collisions	R	11B	Number of collisions that were detected on this interface. Minimum roll-over time = 16 hours.
MAC Interface-FCS/FAE	R	11C	Valid length (64-1518 bytes), non-collision packets with FCS errors. Minimum roll-over time = 80 hours.
MAC Interface-Broadcast	R	11D	Number of good broadcast packets received from this port.
MAC Interface-Multicast	R	11E	Number of good multicast packets received from this port.
MAC Interface-SAchanges	R	11F	Number of times the source address has changed. Minimum roll-over time = 81 hours.

1. R = Read Only.

Ethernet Address Registers

All Ethernet Address Registers consist of two 32-bit registers that together contain a 48-bit Ethernet address. Refer to Table 34 for register bit assignments.

Table 34: Ethernet Address Register Bit Assignments

Upper Address	Bits 15:0 contain bits 47:32 of the Ethernet Address.
Lower Address	Bits 31:0 contain bits 31:0 of the Ethernet Address.

Port Address Tracking Registers

The Port Address Tracking Register set is described in Table 35. These registers continuously monitor the Source Addresses of packets emanating from the corresponding ports. Refer to Table 34 for bit assignments.

Table 35: Port Address Tracking Registers

Name	Type[1]	Addr	Description
rptrAddrTrackNewLastSrcAddress-TP Port 1	R/W	120, 121	
rptrAddrTrackNewLastSrcAddress-TP Port 2	R/W	122, 123	
rptrAddrTrackNewLastSrcAddress-TP Port 3	R/W	124, 125	
rptrAddrTrackNewLastSrcAddress-TP Port 4	R/W	126, 127	
rptrAddrTrackNewLastSrcAddress-TP Port 5	R/W	128, 129	
rptrAddrTrackNewLastSrcAddress-TP Port 6	R/W	12A, 12B	
rptrAddrTrackNewLastSrcAddress-TP Port 7	R/W	12C, 12D	
rptrAddrTrackNewLastSrcAddress-TP Port 8	R/W	12E, 12F	
rptrAddrTrackNewLastSrcAddress-TP Port 9	R/W	130, 131	
rptrAddrTrackNewLastSrcAddress-TP Port 10	R/W	132, 133	
rptrAddrTrackNewLastSrcAddress-TP Port 11	R/W	134, 135	
rptrAddrTrackNewLastSrcAddress-TP Port 12	R/W	136, 137	
rptrAddrTrackNewLastSrcAddress-AUI Port	R/W	138, 139	
rptrAddrTrackNewLastSrcAddress-MAC Port	R/W	13A, 13B	

1. R/W = Read / Write

Authorized Port Address Registers

The Authorized Port Address Register set is described in Table 36. The operation of these registers is determined by the Authorization Control Register. Refer to Table 34 for bit assignments.

Table 36: Authorized Port Address Registers

Name	Type[1]	Addr	Description
Authorized Address Register - TP Port 1	R/W	13C, 13D	
Authorized Address Register - TP Port 2	R/W	13E, 13F	
Authorized Address Register - TP Port 3	R/W	140, 141	
Authorized Address Register - TP Port 4	R/W	142, 143	
Authorized Address Register - TP Port 5	R/W	144, 145	
Authorized Address Register - TP Port 6	R/W	146, 147	
Authorized Address Register - TP Port 7	R/W	148, 149	
Authorized Address Register - TP Port 8	R/W	14A, 14B	
Authorized Address Register - TP Port 9	R/W	14C, 14D	
Authorized Address Register - TP Port 10	R/W	14E, 14F	
Authorized Address Register - TP Port 11	R/W	150, 151	
Authorized Address Register - TP Port 12	R/W	152, 153	
Authorized Address Register - AUI Port	R/W	154, 155	

1. R/W = Read / Write

Search Registers

The Search Register set is described in Table 37.

Table 37: Search Registers

Name	Type[1]	Addr	Description
Search Address Register - Segment 1	R/W	156,157	Each register-pair specifies an Ethernet Source Address to match on the corresponding segment. Refer to Table 34 for bit assignments
Search Address Register - Segment 2	R/W	158,159	
Search Address Register - Segment 3	R/W	15A,15B	
Search Address Register - Segment 4	R/W	15C,15D	
Search Result Register - Segment 1	R	160	Each register indicates which ports on a particular segment sent packets with source addresses that matched the register pair described in the row above. Refer to Table 38 for bit assignments (bit 13 not used). These registers clear when read.
Search Result Register - Segment 2	R	161	
Search Result Register - Segment 3	R	162	
Search Result Register - Segment 4	R	163	

1. R/W = Read / Write.
R = Read Only.

Control and Status Registers

The Control and Status Register set includes general port control and status registers which conform to the bit assignments shown in Table 38, and additional control and status registers with alternate bit assignments shown in Tables 40 through 45.

Table 38: Port Control and Status Register Bit Assignments

31:14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	MAC	AUI	TP12	TP11	TP10	TP9	TP8	TP7	TP6	TP5	TP4	TP3	TP2	TP1

1. Bits 13:12 not used in all registers. Refer to individual register descriptions.

General Port Control Registers

The General Port Control Register set is described in Table 39. Refer to Table 38 for Port Control Register bit assignments. Bits 12 and 13 are not used in all cases (refer to specific register descriptions).

Table 39: Port Control Registers

Name	Type[1]	Addr	Description
Enable Register	R/W	171	Writing a 1 to any bit enables the transmitter and receiver on the corresponding port, writing a 0 disables them. Changing a port's status while the network is active may cause packet fragments to be generated. If the $\overline{\text{MG\_PRSNT}}$ pin is Low, this register will initialize to all 0's (all ports disabled). If the $\overline{\text{MG\_PRSNT}}$ pin is High, this register will initialize to all 1's (all ports enabled).
Reserved	-	172	
Reserved	-	173	
Alternate Partition Register	R/W	174	Writing a 1 to any bit enables the alternate partition algorithm (re-connect on transmit only) for the corresponding port, a 0 the normal algorithm (re-connect on transmit or receive). (Bits 31:13 not used)
Link Control Register	R/W	178	Writing a 1 to any bit enables the Link Partition Algorithm for the corresponding Twisted Pair port, writing a 0 disables it. When this function is disabled, the port automatically goes to Link Pass state and continues to transmit link pulses. (Bits 31:12 not used; Power-up state is all 1's)
Polarity Control Register	R/W	179	Writing a 1 to any bit disables polarity correction for the corresponding Twisted Pair port. (Bits 31:12 not used)
Squelch Control Register	R/W	17A	Writing a 1 to any bit enables the receiver for the corresponding port to use reduced squelch levels for longer-distance cables; writing a 0 enables normal squelch levels to be used. (Bits 31:12 not used)

1. R/W = Read/Write.

Interrupt Status Register

The Interrupt Status Register is described in Table 41. Refer to Table 40 for bit assignments.

Table 40: Interrupt Status Register Bit Assignments

Bits 31:3	Bit 2	Bit 1	Bit 0
Reserved	Jabber	Source Address Change - TP Port	Source Address Change - AUI Port

Table 41: Interrupt Status Register

Name	Type[1]	Addr	Notes
Interrupt Status Register	R	17B	Indicates one of three interrupt conditions. Clears when read. Power-up state is all 0s.

1. R = Read Only

Port Status Registers

The Port Status Register set is described in Table 42. Refer to Table 38 for bit assignments.

Table 42: Port Status Registers

Name	Type[1]	Addr	Notes
AUI Status Register	R	17C	Reports SQE (heartbeat) and Loopback status of AUI port. Refer to Table 44 for details.
Link Status Register	R	17D	A “1” in any bit position indicates the corresponding port is in the “Link Up” state. (Bits 31:12 not used)
Partition Status Register	R	17E	A “1” in any bit position indicates the corresponding port has been partitioned. (Bits 31:13 not used.)
Polarity Status Register	R	17F	A “1” in any bit position indicates that the polarity for the corresponding port has been reversed (Bits 31:12 not used.)
SA Change Detection Register	R	180	A “1” in any bit position indicates that the Source Address has changed on the corresponding port. (Bits 31:13 not used.)

1. R = Read Only.

AUI Control and Status Registers

The AUI Control and Status Register set is described in Table 44. Refer to Table 43 for bit assignments.

Table 43: AUI Control and Status Register Bit Assignments

Register	Bits 31:2	Bit 1	Bit 0
AUI Control	Reserved	Reserved	SQE Mask
AUI Status	Reserved	Loopback	SQE (Heartbeat) Status

Table 44: AUI Control and Status Registers

Name	Type[1]	Addr	Description
AUI Control Register	R/W	177	This bit controls masking or generation of the AUI "heartbeat", defined as brief activity on the AUI CI pair generated by the MAU shortly after successful completion of a transmission. The power-up state of this register is "0". **When the AUI is functioning as a DTE** - If this bit is 1 the device will not react to heartbeat, other than to update the AUI status register. If this bit is 0, the device will react to heartbeat by going into a full receive collision. **When the AUI is functioning as a MAU** - If this bit is 1, the device will not generate heartbeat; if it is 0, the device will generate heartbeat.
AUI Status Register	R	17C	This register reports SQE and Loopback status of AUI port when the LXT918 is operating as the DTE, and has no function when the operating as the MAU). **SQE Heartbeat Status** - This bit indicates the presence or absence of a heartbeat signal from an external MAU (1 = present, 0 = absent). This function operates regardless of the state of the SQE Mask bit in the AUI Control Register. **Loopback** - This bit indicates whether or not data loopback was detected from an external MAU (1 = present, 0 = absent.)

1. R/W = Read/Write.
R = Read Only.

Port Switch, Authorization and LED Control Registers

The Port Switch, Authorization and LED Control Registers are described in Table 46. Refer to Table 45 for bit assignments.

Table 45: Port Switch, Authorization and LED Control Register Bit Assignments[1]

31:28	27:26	25:24	23:22	21:20	19:18	17:16	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
Rs'vd	MAC	AUI	TP12	TP11	TP10	TP9	TP8	TP7	TP6	TP5	TP4	TP3	TP2	TP1

1. Bits 27:26 used by Port Switch Control Register only.

Table 46: Port Switch, Authorization and LED Control Registers

Name	Addr	Description[1]
Port Switch Control Register	170	This register controls the mapping of ports to segments. Each port is assigned two bits in this register, as shown in Table 45. For each set of bits, the mapping is as follows: 00 = Segment 1 01 = Segment 2 10 = Segment 3 11 = Segment 4
Authorization Control Register	175	Determines the operational mode of the Authorized Address Register for each port. 00 = Free-Run. The Authorized Address Register continuously re-learns its contents from the source addresses of incoming packets (Power-up default). 01 = Next Lock. The Authorized Address Register learns the source address of the next valid packet and locks. Once it locks, the corresponding bits in this register automatically change to '10'. 10 = Lock. The Authorized Address Register does not change with traffic flow. In this mode, it can only be updated under network management control. 11 = Reserved.
LED Control Register	176	Controls operation of the serial LED bits associated with each port. The power-up state of this register is all 1's if an external manager is detected, and defaults to "hardware control" otherwise. 00 = LED off 01 = LED fast blink 10 = hardware control 11 = LED on

1. The Port Switch Control Register, Authorization Control Register and the LED Control Register are all Read/Write.

Configuration Registers

Configuration Registers are listed in Table 47. Bit assignments for the Configuration Registers are shown in Table 48 through 53. The Master Configuration Register is defined in Table 54.

Table 47: Configuration Registers

Name	Type[1]	Addr	Notes
Global LED Control Register	R/W	181	Refer to Table 48 for bit assignments. This register controls the operating modes of the Global Fault LED and User Defined LED. Bit Encodingas follows: **Global Fault LED** 00 = Off 01 = Hardware Control 10 = Slow Blink 11 = 0n Steady **User Defined LED** 00 = Off 01 = Fast Blink 10 = Reserved 11 = On Steady
LED Timer Register	R/W	182	Refer to Table 49 for bit assignments. Bits 8-15 of this register set the fast blink frequency of the LEDs. Bits 0-7 set the slow blink frequency. The same formula is used in each case, with a maximum of 128 Hz and a minimum of 0.5 Hz (for example, fast blink = 32 (0.4 s); slow blink = CC (1.6 s)).
Master Configuration Register	R/W	183	Refer to Tables 53 and 54 for bit assignments and definitions. At power-up, all bits in this register default to 0.
AUI Configuration Register	R/W [2]	184	Bit 0 sets the AUI port mode (0 = Normal, 1 = Reversed). Bits 15:1 may contain user-defined configuration data.
Device ID Register	R	185	This register follows the IEEE 1149.1 specification; refer to Table 50 for bit assignments. The upper 4 bits identify the device revision level. The next 16 bits store the Part ID Number in hexadecimal, which is '0396'. The lower 12 bits contain a JEDEC Manufacturer ID, which for Level One is hexadecimal 'FE'.
Repeater Reset Register	W	186	Writing any data value to this register causes all functional logic to reset, but does not affect the state of counters, configuration registers or status registers.
Software Reset Register	W	187	Writing any data value to this register is identical to a hardware reset. Everything is reset except counters and addresses.
HUB ID Register (1 and 2)	W	188, 189	Refer to Table 51 for bit assignments. Writing a valid 48-bit ID (one that matches the EPROM ID) to this register causes the device to change its Hub ID to the contents of the EPROM ID register listed below. This register cannot be read.
EPROM ID Register (1 and 2)	R	190, 191	These two registers contain the 48-bit ID read in from EPROM at power-up. Refer to Table 52 for bit assignments.

1. R = Read Only.
   W = Write Only.
   R/W = Read/Write.
2. Writes to Register 184 are accomplished via the AUICONFIG_IN pin, not via the STX pin. Reads to Register 184 are standard, except that 2 reads are required to ensure new data is shifted into the register after a change.

Table 48: Global LED Control Register Bit Assignments

31:4	3	2	1	0
Reserved	Global Fault LED		User Defined LED	

Table 49: LED Timing Control Register Bit Assignments

31:16	15:8	7:0
Reserved	Fast Blink Frequency	Slow Blink Frequency

1. Period = 7.8125 ms x (Register Value + 1)

2. Frequency = $\frac{1}{7.8125\ ms\ x\ (Register\ Value + 1)}$

Table 50: Device ID Register Bit Assignments

31:28	27:12	11:8	7:1	0
Version	Part ID	Jedec Continuation Characters	JEDEC ID	Chip ID
XXXX	0000 0011 1001 0110	0000	111 1110	0

Table 51: Hub ID Register Bit Assignments

Upper Address	31:21 - All 0s	20:16 - Hub ID	15:0 - Must match bits 15:0 of upper EPROM ID Register
Lower Address	31:0 - Must match bits 31:0 of lower EPROM ID Register		

Table 52: EPROM ID Register Bit Assignments

Upper Address	31:16 - All 0s	15:0 - Bits 15:0 of Address read from EPROM
Lower Address	31:0 - Bits 47:16 of Address read from EPROM	

Table 53: Master Configuration Register Bit Assignments

31:11	10	9	8:5	4	3	2	1	0
Reserved	Arbin	Zero Counters	Isolate 4:1	CountMode	Soft Reconnect	EFIFOERR	EMCV	Reserved

Table 54: Master Configuration Register Bit Definitions

Bit	Name	Type[1]	Description	Default
31:11	Reserved	-	Write as 0, ignore on read.	N/A
10	Arbin	R	This bit shows the value present at the ARBIN input pin.	0
9	Zero Counters	R/W	Setting this bit to "1" will cause all counters to be zeroed. Upon completion of this operation, the device will reset this bit to "0".	0
8:5	Isolate4:1	R/W	Each of these bits controls the corresponding Isolate output. Setting any bit to "1" causes the corresponding Isolate output pin to be asserted High.	0
4	CountMode	R/W	This bit affects the operation of the portReadableFrames and MACReadableFrames counters. Setting this bit to 0 will cause these counters to count all readable frames; setting this bit to 1 will cause these counters to count only readable unicast frames.	0
3	Soft Reconnect	R/W	Setting this bit to 1 enables the Soft Reconnect feature of the device. When this feature is enabled, when a port switch is initiated (by writing to the Port Switch Register), the device waits until traffic is idle before removing the port from the old segment, or adding it to the new segment.	0
2	EFIFOERR	R/W	This bit determines whether the device will enter the Transmit Collision State if its internal FIFO overflows or underflows (data-rate mismatch). 0 = no, 1 = yes.	0
1	EMCV	R/W	This bit determines whether the device will enter the Transmit Collision State upon reception of a Manchester Code Violation; 0 = no, 1 = yes.	0
0	Reserved	-	Write as 0, ignore on read.	N/A

1. R/W = Read/Write.
   R = Read Only.