4 CHANNEL PUSH-PULL INVERTING OUTPUT DRIVER

LAS-8091P

FEATURES

- 200mA per channel continuous output rating
- 50 KHz operation
- Latching current limit for each output (source mode) with reset and status check
- Internal clamp diodes
- Non-latching overtemperature protection

DESCRIPTION

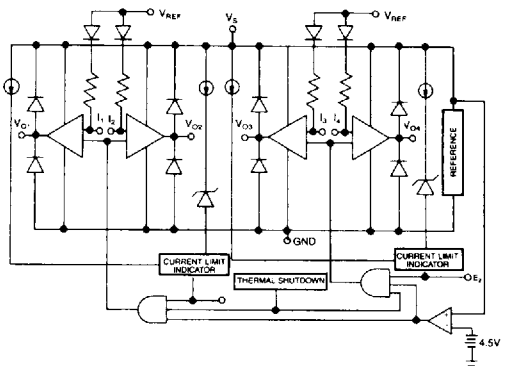
The LAS 8091P is a monolithic integrated circuit designed for application as a four channel inverting output driver for inductive loads such as relays and solenoids, in addition to capacitive loads up to 0.03μF. The LAS 8091P offers latching current limit in the source mode to protect the device against fault conditions at the load. A latched output state can be detected by measuring voltage levels at the enable pins. Reset of the current latch can be cleared by grounding the appropriate pin for that output channel or toggling its input. Input ports to the LAS 8091P are controlled by voltage or resistance loads for each channel, allowing direct drive from voltage sources or open collector devices such as opto-couplers.

The LAS 8091P is packaged in a 16 lead DIP configuration which has the 4 center pins connected together for heatsinking. Thermal protection is provided to force all outputs to off state.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MAXIMUM	UNITS
Supply Voltage	V_S	36	Volts
Input Voltage	V_I	30	Volts
Enable Voltage	V_E	30	Volts
Peak Output Current Source Mode Sink Mode	I_O	 Internally Limited 440	 mA
Total Power Dissipation at $T_{GROUND\ PINS}$ = 25°C	P_D	2.2	Watts
Thermal Resistance Junction to Ground Pins	θ_{JC}	10	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	80	°C/W
Operating Junction and Storage Temperature Range	T_J T_{STG}	−25 to 125	°C
Lead Temperature (Soldering, 12 Seconds)	T_{LEAD}	260	°C

BLOCK DIAGRAM



14

LAS-8091P

4 CHANNEL PUSH-PULL INVERTING OUTPUT DRIVER

ELECTRICAL CHARACTERISTICS

Test conditions for each channel are as follows: I_O = 0A, V_S = 4.75–36 V[1], T_J = 25°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
INPUT CHARACTERISTICS						
Input Logic Level						
"Low"	V_{IL}		−0.3		0.8	Volts
"High"	V_{IH}		2.9		30	Volts
Input Current		T_J = −25°C to +125°C				
"Low"	I_{IL}	V_I = 0.8V	−60	−300	−600	µA
"High"	I_{IH}	V_I = 30V	0		10	µA
Enable Logic Level						
"Low"	V_{EL}		−0.3		0.8	Volts
"High"	V_{EH}		2.5		V_S + 0.3	Volts
Enable Current						
"Low"	I_{EL}	V_E = 0.8V	−50	−300	−1500	µA
"High"	I_{EH}	V_E = 30V	0		10	µA
Current Limit	I_{ECL}			1.7	5.0	mA
CURRENT LIMIT CHARACTERISTICS[2,3]						
Output Current Limit Latch Threshold	I_{CL}	T_J = −25°C to +125°C	240	340	440	mA
Output Current Limit Latch Delay Time	T_{DELAY}	Min load to trigger latch		50		µS
		Shorted load		10		µS
Output Current Limit Latch Reset (Clear) Time	T_{RESET}	V_E = −0.3V to 0.8V			10	µS
OUTPUT CHARACTERISTICS						
Output Voltage Saturation						
"Sink"	V_{SATL}	I_O = −200mA		0.95	1.05	Volts
		I_O = −100mA		0.90	1.00	Volts
"Source"	V_{SATH}	I_O = 200mA		0.95	1.05	Volts
		I_O = 100mA		0.90	1.00	Volts
Output Leakage Current (Per Channel)	I_L	V_E = 0.8V			200	µA
Clamp Diode Forward Voltage Drop	V_F	I = 200mA			1.45	Volts
Total Quiescent Current	I_S	All outputs low, high or off		32	42	mA
Undervoltage Lockout				4.5		Volts
Thermal Shutdown				160		°C
SWITCHING CHARACTERISTICS						
Output Rise Time	T_R	0.1V_O to 0.9V_O		85	200	nS
Output Fall Time	T_F	0.9V_O to 0.1V_O		85	200	nS
Turn-on Delay Time	T_{DH}	0V to 0.1V_O		0.8	2.0	uS
Turn-off Delay Time	T_{DL}	V_O to 0.9V_O		0.8	2.0	uS

(1) When V_S is greater than 24V, external clamp diodes may be required for some inductive load applications.
(2) A current limited output state can be determined by measuring the voltage levels at the Enable pins.
(3) The latched output state is reset when a "LOW" is applied to the Enable pins or the input for that output is toggled. Upon completion of the reset cycle, voltage levels at the Enable pins will reflect the new output current latch status.

4 CHANNEL PUSH-PULL INVERTING OUTPUT DRIVER

LAS-8091P

OPERATIONAL DATA

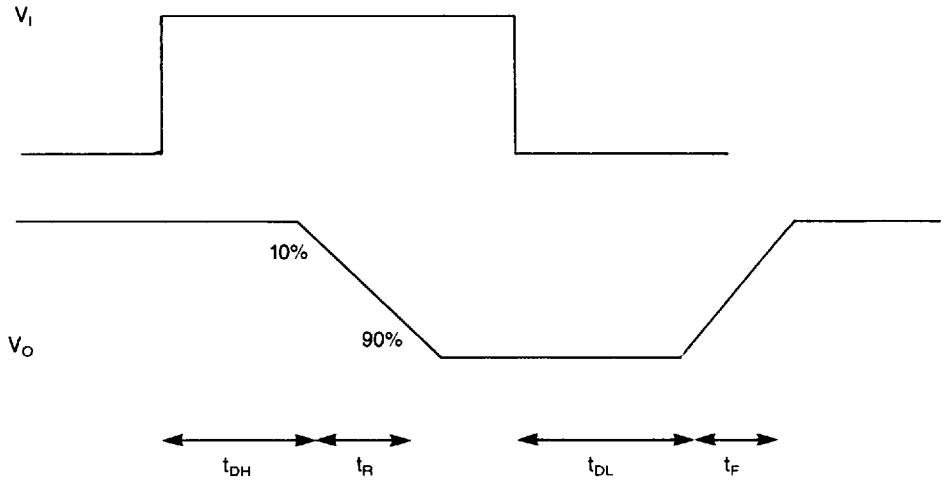
OUTPUT CURRENT LATCH STATUS

OUTPUT CHANNELS IN A CURRENT FOLDBACK STATE	ENABLE 1 OUTPUT VOLTAGE (PIN 1)[4]		ENABLE 2 OUTPUT VOLTAGE (PIN 9)[4]	
	MIN.	MAX.	MIN.	MAX.
NONE	0.8	2.5	0.8	2.5
#1	$V_S - 0.6$	V_S	0.8	2.5
#2	$V_S - 8.0$	$V_S - 6.0$	0.8	2.5
#3	0.8	2.5	$V_S - 0.6$	V_S
#4	0.8	2.5	$V_S - 8.0$	$V_S - 6.0$
#1 & #2	$V_S - 0.6$	V_S	0.8	2.5
#3 & #4	0.8	2.5	$V_S - 0.6$	V_S

[4] In order to make a proper voltage reading at either Enable 1 or Enable 2, it is recommended to load each pin with 100KΩ to 1 MΩ resistance. Overloading either of the Enable pins may result in a condition similar to grounding the pins.

14

SWITCHING TIMES



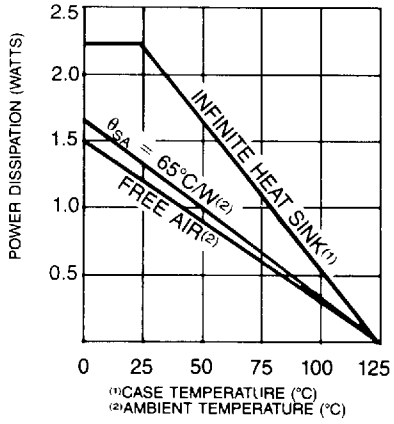
TRUTH TABLE PER CHANNEL

INPUT	ENABLE	OUTPUT
L	H	H
H	H	L
H	L	OFF
L	L	OFF

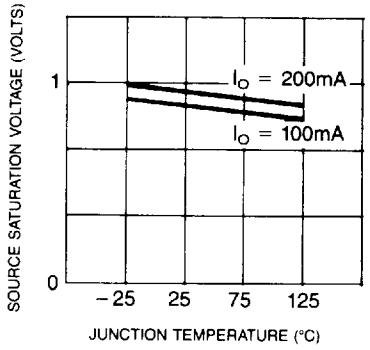
LAS-8091P

4 CHANNEL PUSH-PULL INVERTING OUTPUT DRIVER

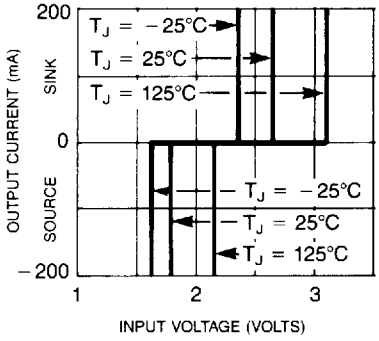
POWER DERATING (POWER DISSIPATION FOR 2 FULL BRIDGES AT 100% D.C.)



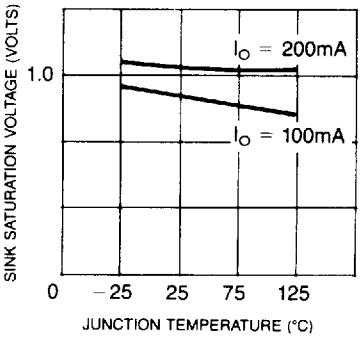
SOURCE SATURATION VOLTAGE VS TEMPERATURE



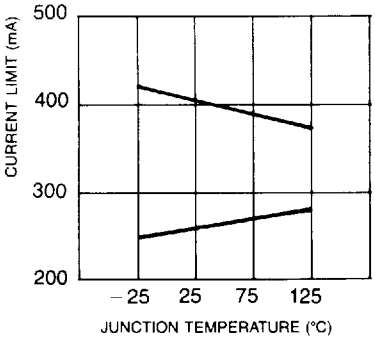
OUTPUT CURRENT VS INPUT VOLTAGE



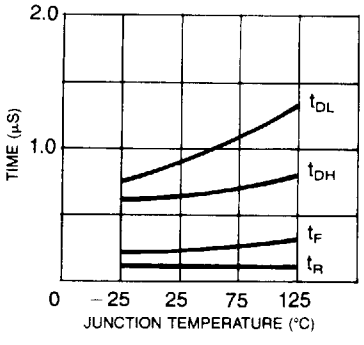
SINK SATURATION VOLTAGE VS TEMPERATURE



CURRENT LIMIT VS TEMPERATURE



SWITCHING TIMES VS TEMPERATURE

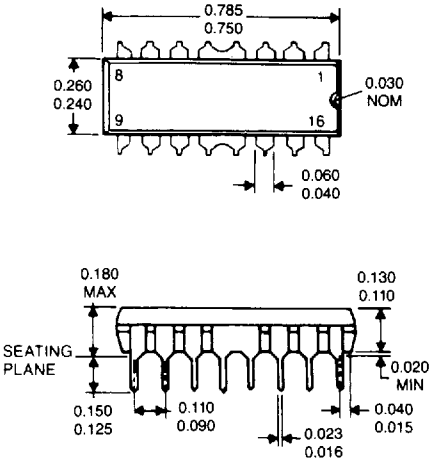


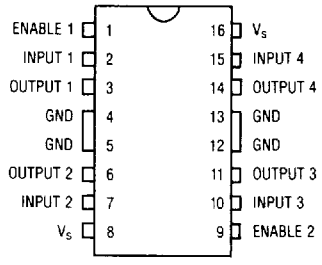
4 CHANNEL PUSH-PULL INVERTING OUTPUT DRIVER

LAS-8091P

DEVICE OUTLINE

16-PIN MOLDED DUAL IN-LINE





NOTE: The V_S pins (pins 8 & 16) are connected together inside the IC. In order to reduce the voltage drop (saturation voltage) at any of the output ports (pins 3, 6, 11 & 14), both DC power pins (pins 8 & 16) should be connected together external to the IC. This is strongly recommended for any application. All dimensions are in inches.