HYUNDAI

HY514410B Series

1M x 4-bit CMOS DRAM with Write-Per-Bit

PRELIMINARY

DESCRIPTION

The HY514410B is the new generation and fast dynamic RAM organized 1,048,576 x 4-bit with function of Write-Per-Bit. The HY514410B utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY514410B to be packaged in a standard 20/26 pin plastic SOJ, TSOP-II and Reverse TSOP-II.
The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5V± 10% tolerence and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- **Low power dissipation**
  Max. battery back-up 1.1mW (L-part)
  Max. CMOS standby 0.825mW (L-part)
  5.5mW
  Max. TTL standby 11.0mW
  Max. Self refresh 1.1mW (SL-part)
  Max. operating

Speed	Power
50	550.0mW
60	495.0mW
70	440.0mW

- **Single power supply of 5V± 10%**
- **TTL compatible inputs and outputs**
- **Fast access Time**

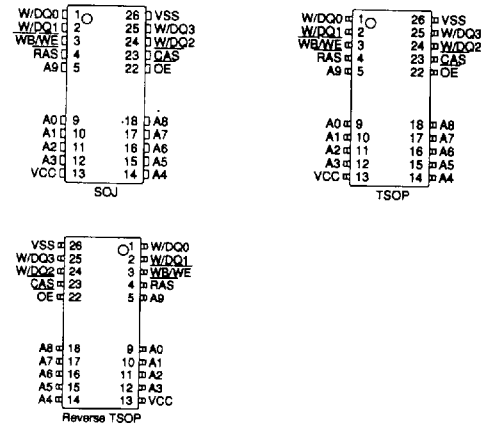
Speed	tRAC	tCAC	tPC
50	50ns	15ns	35ns
60	60ns	15ns	40ns
70	70ns	20ns	45ns

- **Fast page mode operation**
- **Write-Per-Bit and Multi-bit test capability**
- **Read-Modify-Write capability**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh and Self refresh**
- **1024 refresh cycles / 128ms (L-part)**
  1024 refresh cycles / 16ms

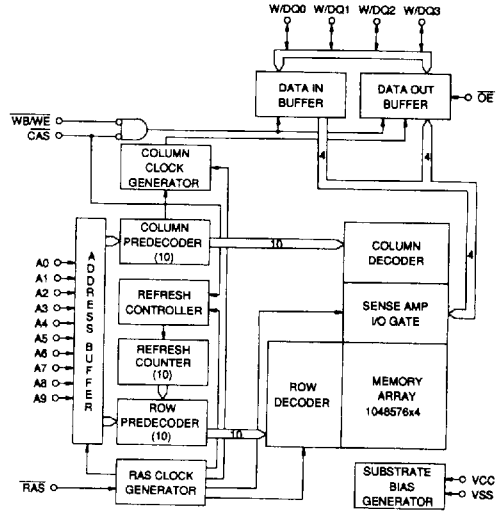
PIN DESCRIPTION

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB/WE}$	Write-Per-Bit/Write Enable
$\overline{OE}$	Output Enable
A0-A9	Address Input
W/DQ0-W/DQ3	Write Mask/Data IO
Vcc	Power (+ 5V)
Vss	Ground

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	–1.0 to 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	–1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	0.90	W
T_{SOLDER}	Soldering Temperature• Time	260• 10	°C• sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC}+ 1.0	V
V_{IL}	Input Low Voltage	–1.0	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A= 0°C to 70°C, V_{CC}= 5V± 10%, V_{SS}= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pins)	$V_{SS} \le V_{IN} \le 6.5V$, All other pins not under test= V_{SS}		-10	10	µA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le 5.5V$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	V_{CC} Supply Current, Operating	t_{RC}= t_{RC} (min.)	50 60 70	- - -	100 90 80	mA	1,2,3
I_{CC2}	V_{CC} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, other inputs≥ V_{SS}		-	1	mA	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-only refresh	t_{RC}= t_{RC} (min.)	50 60 70	- - -	100 90 80	mA	1,3
I_{CC4}	V_{CC} Supply Current, Fast Page mode	t_{PC}= t_{PC} (min.)	50 60 70	- - -	70 60 50	mA	1,2,3
I_{CC5}	V_{CC} Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≥ V_{CC}–0.2V	 L-part	- -	1 0.15	mA	 5
I_{CC6}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_{RC}= t_{RC} (min.)	50 60 70	- - -	100 90 80	mA	1,3
I_{CC7}	V_{CC} Supply Current, Battery Back Up (L-part only)	t_{RC}= 125µs, t_{RAS}≤ 1µs $\overline{CAS}$= CBR cycling or 0.2V $\overline{OE}$ & $\overline{WE}$= V_{CC}–0.2V, A0-A9= V_{CC}–0.2V or 0.2V W/DQ0-W/DQ3= 0.2V, V_{CC}–0.2V or open		-	200	µA	1,4,5
I_{CC8}	V_{CC} Supply Current, Self Refresh (SL-part only)	$\overline{RAS}$ & $\overline{CAS}$ ≤ 0.2V other pins same as I_{CC7}		-	200	µA	6
V_{OL}	Output Low Voltage	I_{OL}= 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH}= –5mA		2.4	-	V	

NOTE :

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading. Specified values are obtained with the output open.
3. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$= V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$= V_{IH}.
4. Only t_{RAS}(max.)= 1µs is applied to refresh of battery backup but t_{RAS}(max.)= 10µs is applied to normal functional operation .
5. I_{CC5}(max.)= 0.15mA and I_{CC7} are applied to L-parts (HY514410BLJ, HY514410BLT, HY514410BLR, HY514100BSLJ, HY514100BSLT, and HY514100BSLR).
6. I_{CC8} is applied to SL-parts only (HY514410BSLJ, HY514410BSLT and HY514410BSLR)

AC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 5V± 10%, Vss= 0V, unless otherwise noted.) NOTE : 1, 2, 3,13

#	SYMBOL	PARAMETER	HY514410BJ/BT/BR/BLJ/BLT/BLR/BSLJ/BSLT/BSLR						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	130	-	150	-	180	-	ns	
3	tPC	Fast Page Mode Cycle Time	35	-	40	-	45	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	75	-	80	-	95	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	50	-	60	-	70	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	15	-	15	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	30	-	35	-	40	ns	4,15
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	$\overline{RAS}$ Precharge Time	30	-	40	-	50	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	50	10K	60	10K	70	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	50	200K	60	200K	70	200K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	15	-	15	-	20	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	50	-	60	-	70	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	15	10K	15	10K	20	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	15	35	15	45	20	50	ns	9
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	10	25	15	30	15	35	ns	10
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	15
21	tCP	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	17
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	8	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	14
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	14
26	tAR	Column Address Hold Time from $\overline{RAS}$	40	-	50	-	55	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	25	-	30	-	35	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	14
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	6,14
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	14
32	tWCR	Write Command Hold Time from $\overline{RAS}$	40	-	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	10	-	15	-	15	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	15	-	15	-	20	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	15	-	15	-	20	-	ns	16
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	40	-	50	-	55	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	12
		L-part	-	128	-	128	-	128		11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8,14

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY514410BJ/BT/BR/BLJ/BLT/BLR/BSLJ/BSLT/BSLR						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	35	-	35	-	40	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	70	-	80	-	95	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	45	-	50	-	60	-	ns	8
44	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	14
45	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	15
46	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	14
47	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	25	-	30	-	35	-	ns	17
48	tROH	$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	10	-	10	-	10	-	ns	
49	tOEA	$\overline{OE}$ Access Time	-	15	-	15	-	20	ns	
50	tOED	$\overline{OE}$ to Data Delay	15	-	15	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	15	0	15	0	20	ns	5
52	tOEH	$\overline{OE}$ Command Hold Time	15	-	15	-	20	-	ns	
53	tCPWD	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	50	-	55	-	65	-	ns	8
54	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	30	-	35	-	40	-	ns	
55	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
57	tWTS	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
58	tWTH	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
59	tWBS	Write-Per-Bit Set-up Time	0	-	0	-	0	-	ns	
60	tWBH	Write-Per-Bit Hold Time	10	-	10	-	10	-	ns	
61	tWDS	Write-Per-Bit Selection Set-up Time	0	-	0	-	0	-	ns	
62	tWDH	Write-Per-Bit Selection Hold Time	10	-	10	-	10	-	ns	
63	tRASS	$\overline{RAS}$ Pulse Width(Self Refresh)	100	-	100	-	100	-	µs	
64	tRPS	$\overline{RAS}$ Precharge Time(Self Refresh)	120	-	130	-	150	-	ns	
65	tCHS	$\overline{CAS}$ Hold Time from $\overline{RAS}$(Self Refresh)	-50	-	-50	-	-50	-	ns	

AC CHARACTERISTICS IN TEST MODE NOTE 18

#	SYMBOL	PARAMETER	HY514410BJ/BT/BR/BLJ/BLT/BLR/BSLJ/BSLT/BSLR						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	95	-	115	-	135	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	135	-	155	-	185	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	80	-	85	-	100	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	55	-	65	-	75	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	20	-	20	-	25	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	45	ns	4
13	tRAS	$\overline{RAS}$ Pulse Width	55	10K	65	10K	75	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	55	200K	65	200K	75	200K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	55	-	65	-	75	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	20	10K	20	10K	25	10K	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	40	-	40	-	50	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	75	-	85	-	100	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	50	-	55	-	65	-	ns	8
49	tOEA	$\overline{OE}$ Access Time	-	20	-	20	-	25	ns	
50	tOED	$\overline{OE}$ to Data Delay	20	-	20	-	25	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	15	0	15	0	20	ns	5
52	tOEH	$\overline{OE}$ Command Hold Time	20	-	20	-	25	-	ns	

NOTE :

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle before proper device operation is achieved.
2. If $\overline{RAS}$= Vss during power-up, the HY514410B could begin an active cycle. These condition results in higher current than necessary which is demanded from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with Vcc during power-up or be held at a valid V_{IH} in order to minimize the power-up current
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min.) and V_{IL}(max.), and are assumed to be 5ns for all inputs.
4. Measured at V_{OH}= 2.4V and V_{OL}= 0.4V with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) and t_{OEZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WB}/\overline{WE}$ leading edge in Read-Modify-Write cycles.
8. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.), and $t_{CPWD} \geq t_{CPWD}$(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. t_{REF}(max.)= 128ms is applied to L-Parts (HY514410BLJ/BSLJ, HY514410BLT/BSLT and HY514410BLR/BSLR).
12. A burst of 1024$\overline{CAS}$-before-$\overline{RAS}$ refresh cycles must be executed within 16ms(128ms for L-part) after exiting self refresh.
13. When $\overline{CAS}$ goes low, 4-bits data are written into the device.
14. These parameters are determined by the earlier falling edge of $\overline{CAS}$.
15. These parameters are determined by the later rising edge of $\overline{CAS}$.
16. t_{CWL} must be satisfied by $\overline{CAS}$ for 4-bits access cycles.
17. t_{CP} and t_{CPT} are measured when $\overline{CAS}$ is high state.
18. These specifications are applied to the test Mode.

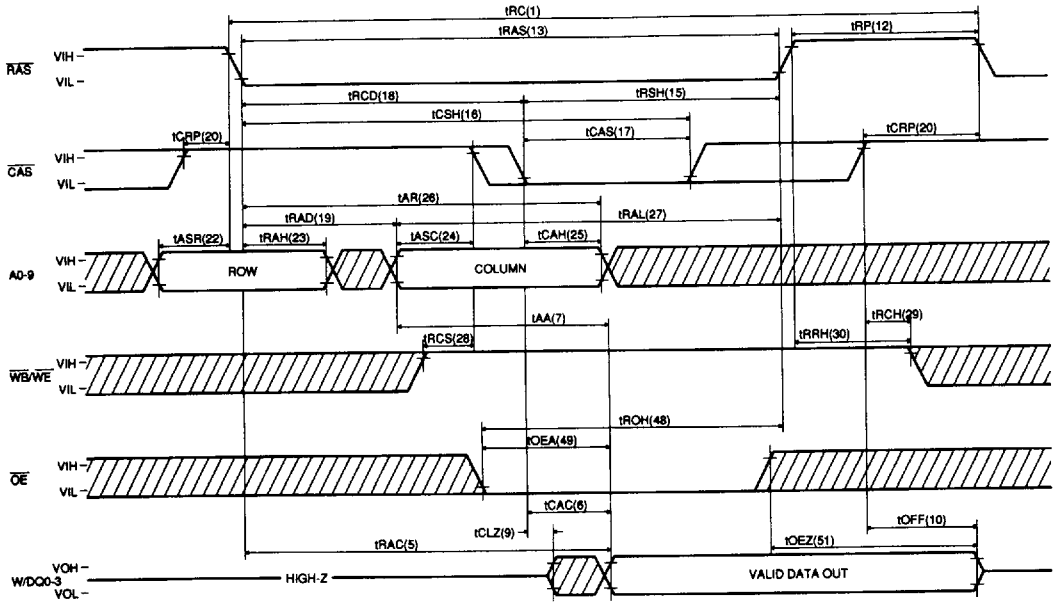
CAPACITANCE

(T_A= 25°C, V_{CC}= 5V± 10%, V_{SS}= 0V, f= 1MHz, unless otherwise noted.)

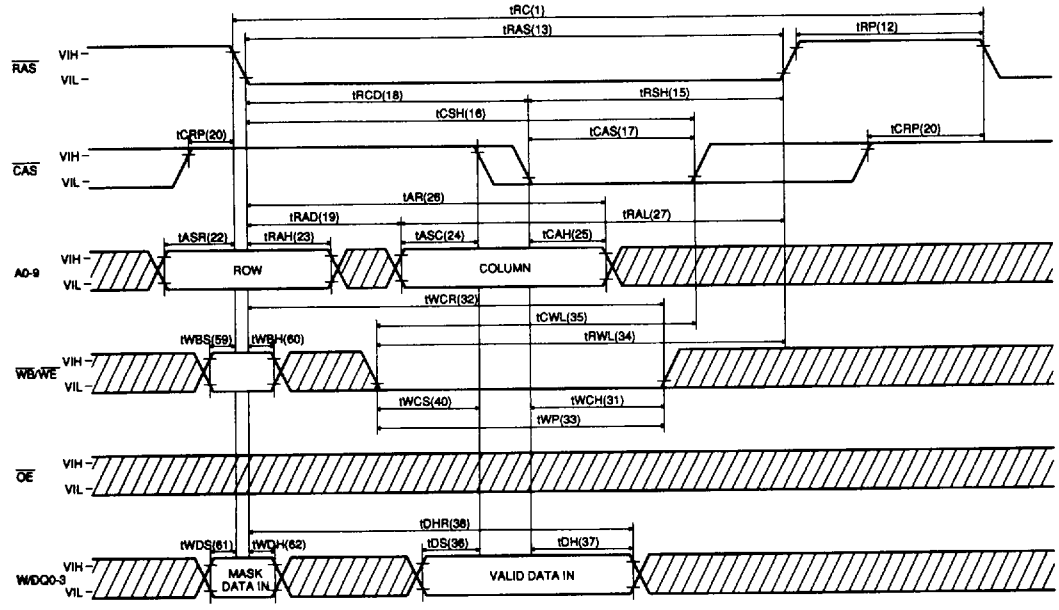
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A9)	-	5	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{OE}$)	-	7	pF
C_{DQ}	Data Input/Output Capacitance (W/DQ0-W/DQ3)	-	7	pF

TIMING DIAGRAM

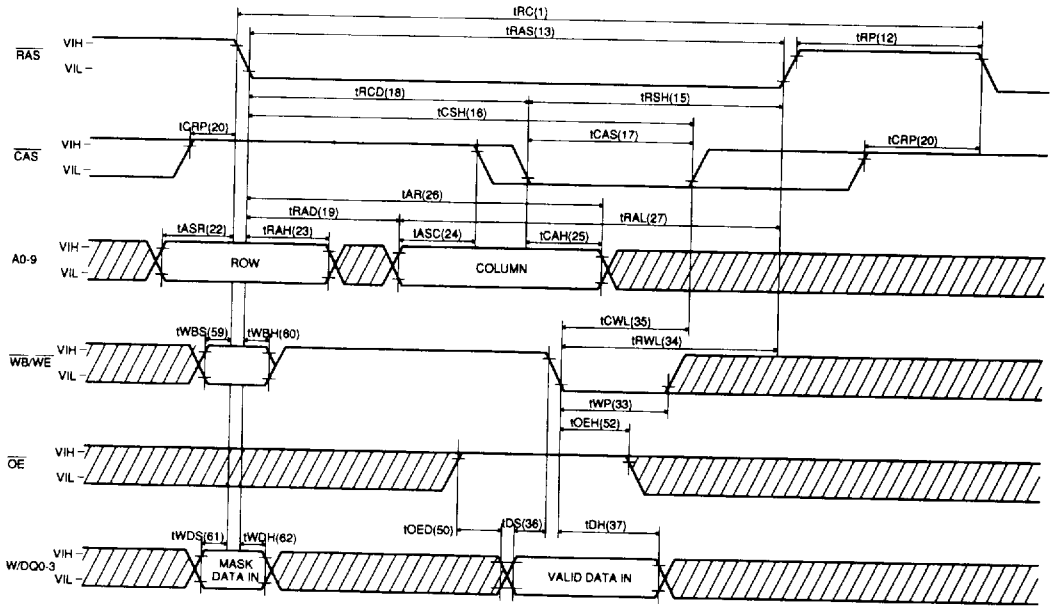
READ CYCLE



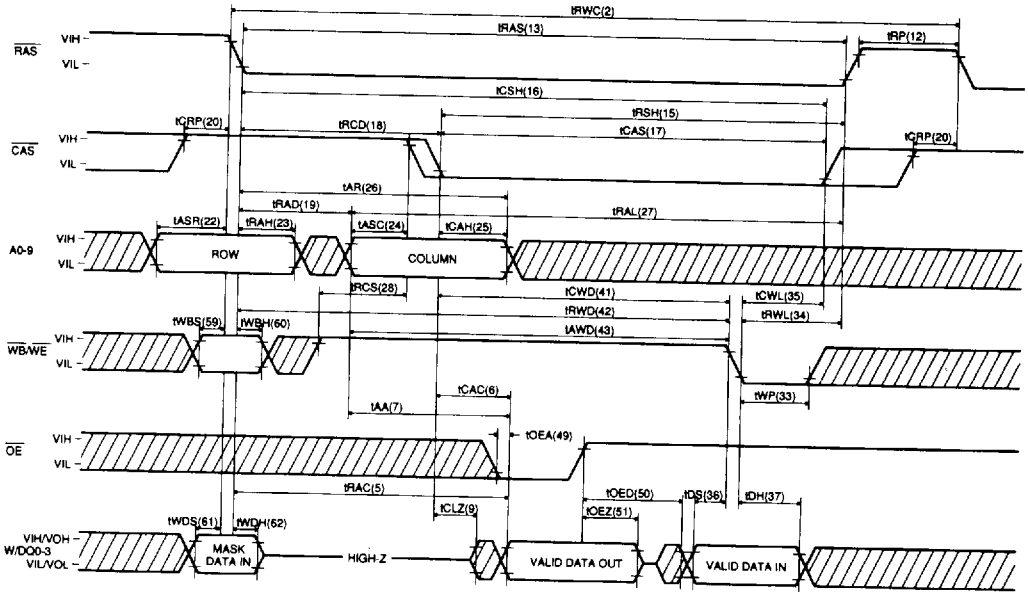
EARLY WRITE CYCLE



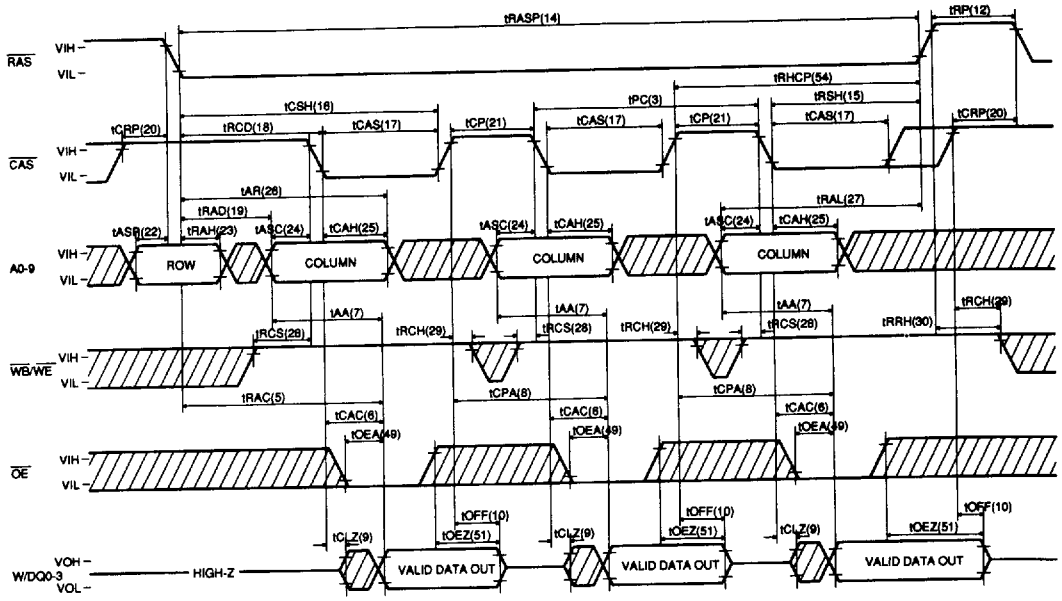
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



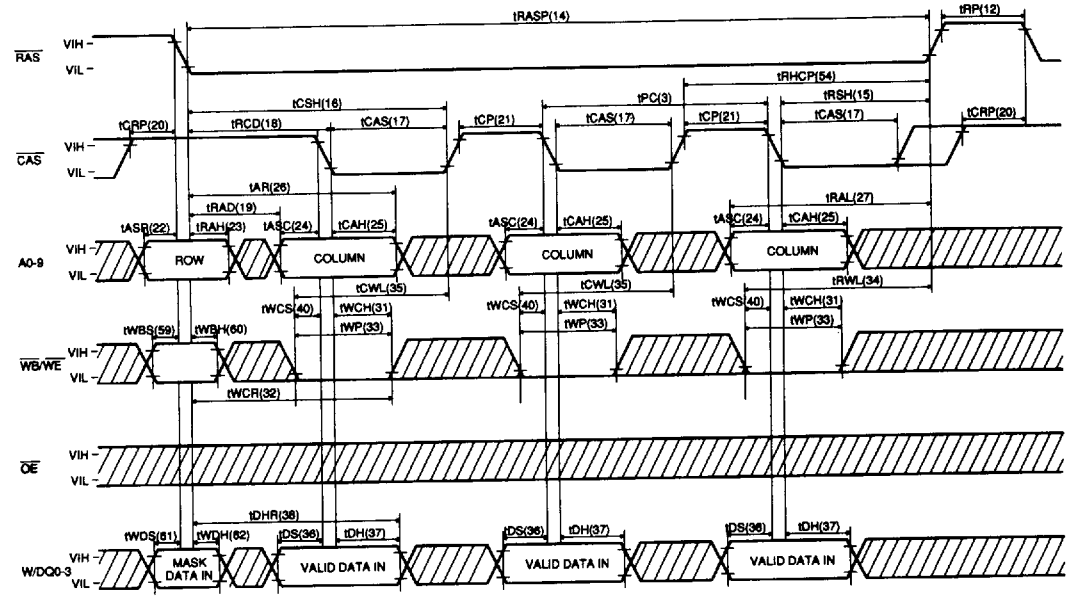
READ-MODIFY-WRITE CYCLE



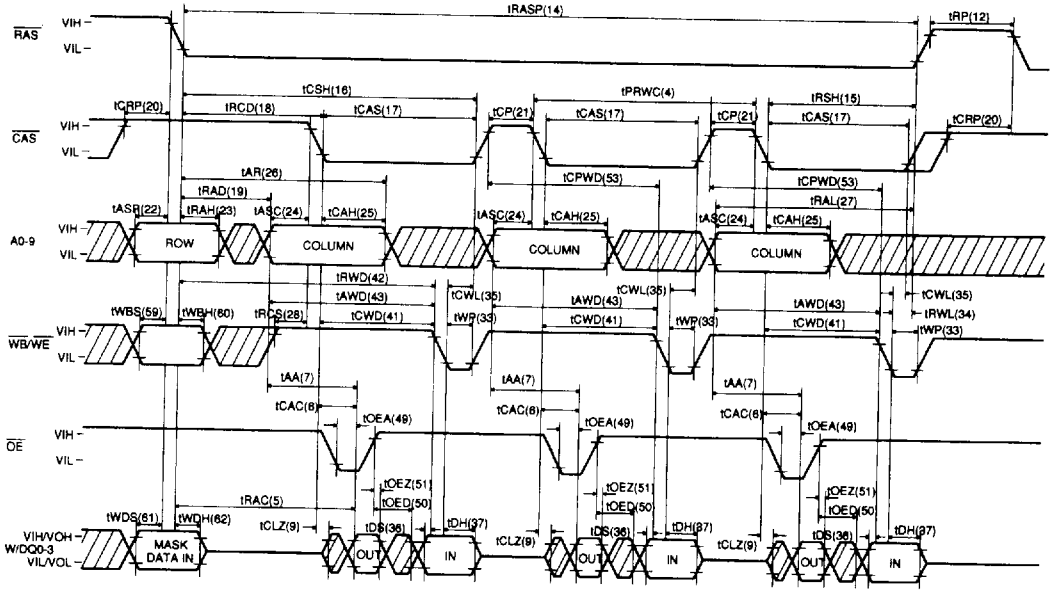
FAST PAGE MODE READ CYCLE



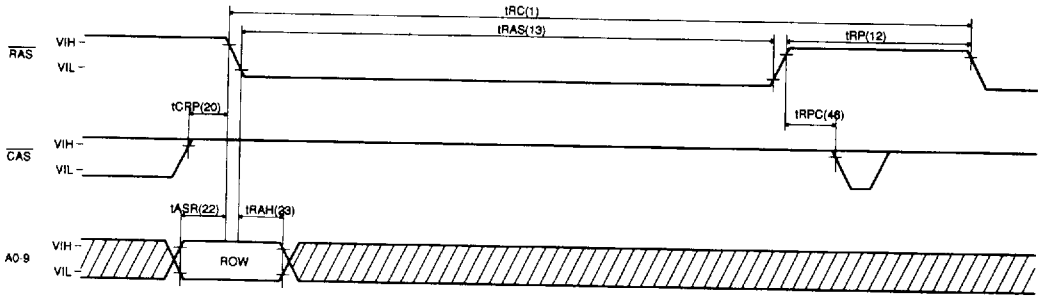
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

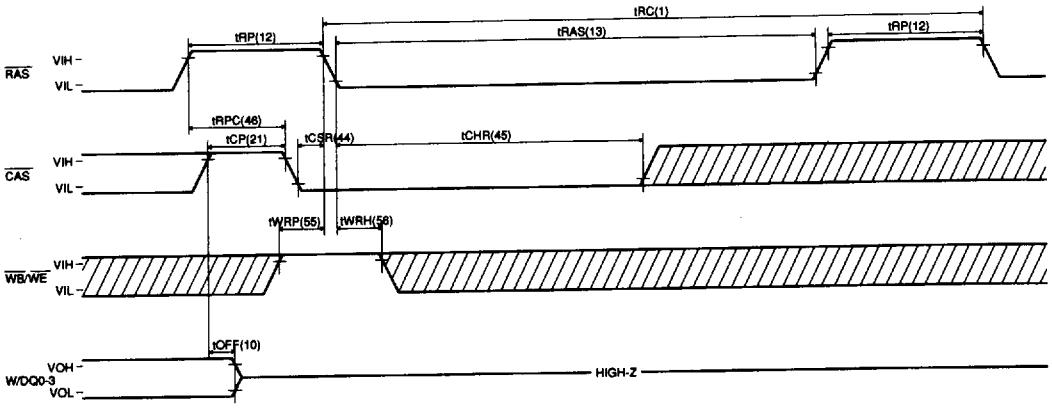


RAS-ONLY REFRESH CYCLE



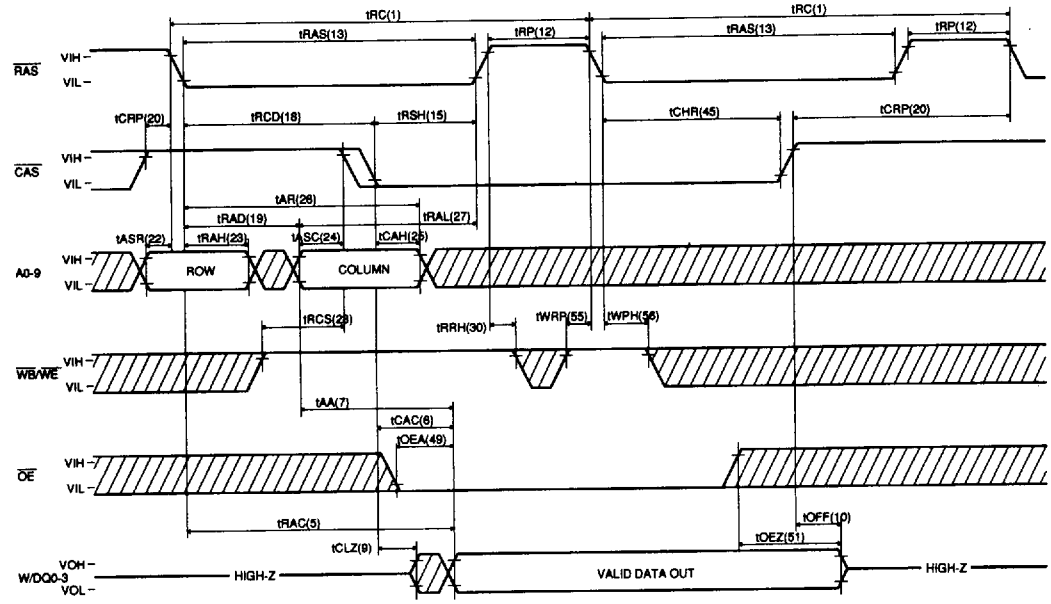
NOTE : $\overline{OE}$ and $\overline{WB/WE}$ = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

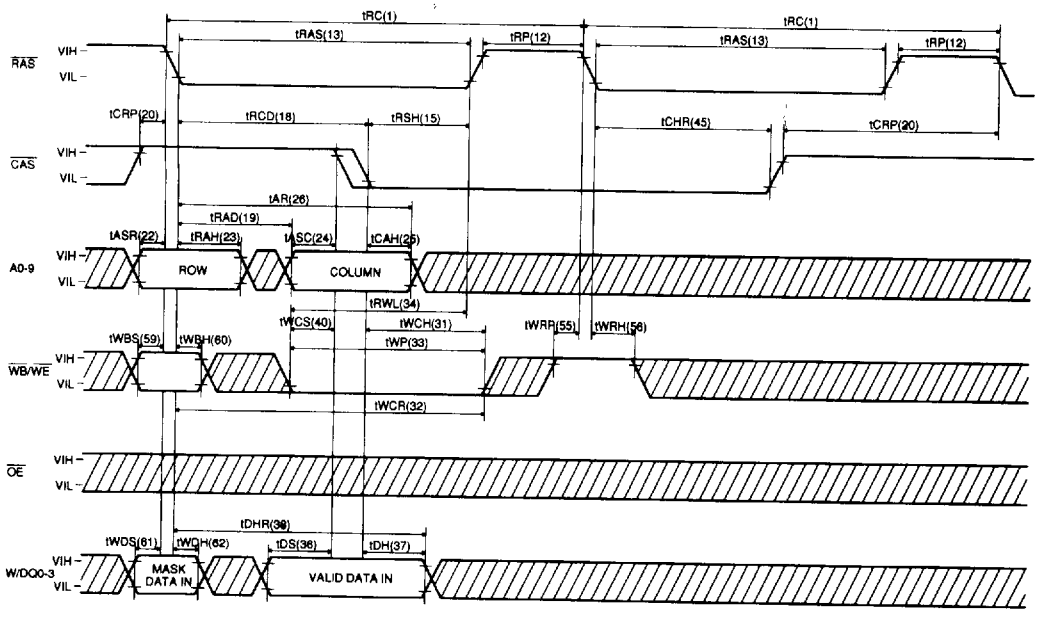


NOTE : A0-9 and $\overline{OE}$ = "H" or "L"

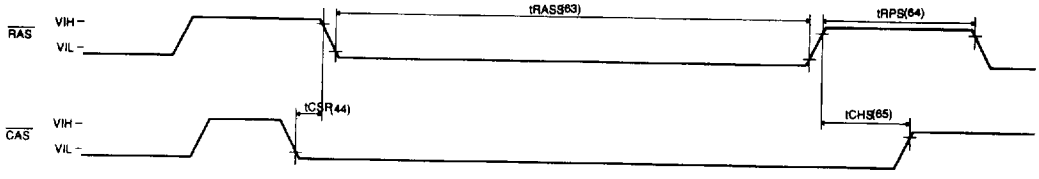
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

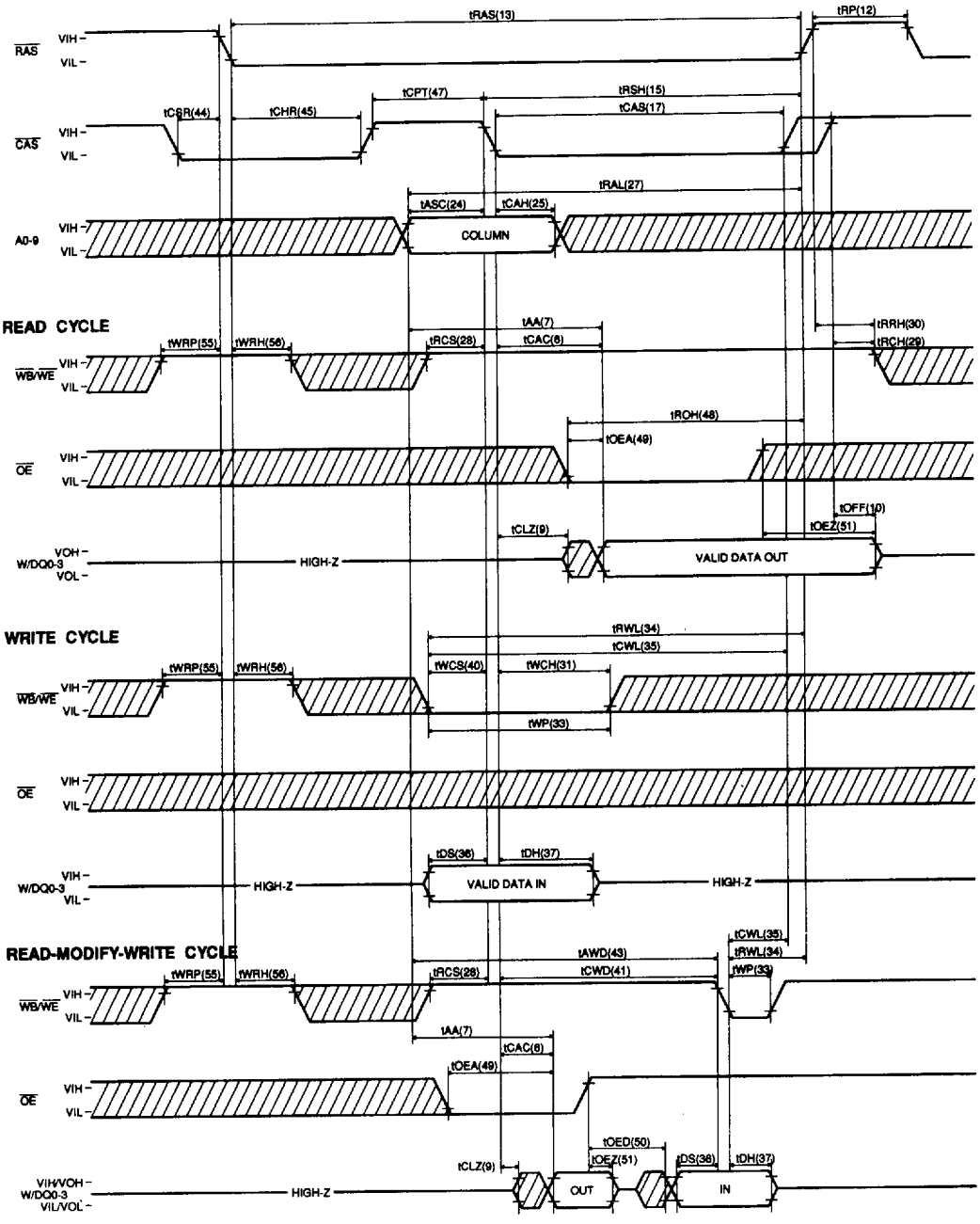


CAS-BEFORE-RAS SELF REFRESH CYCLE



NOTE : A0-9, WB/WE and OE = "H" and "L"

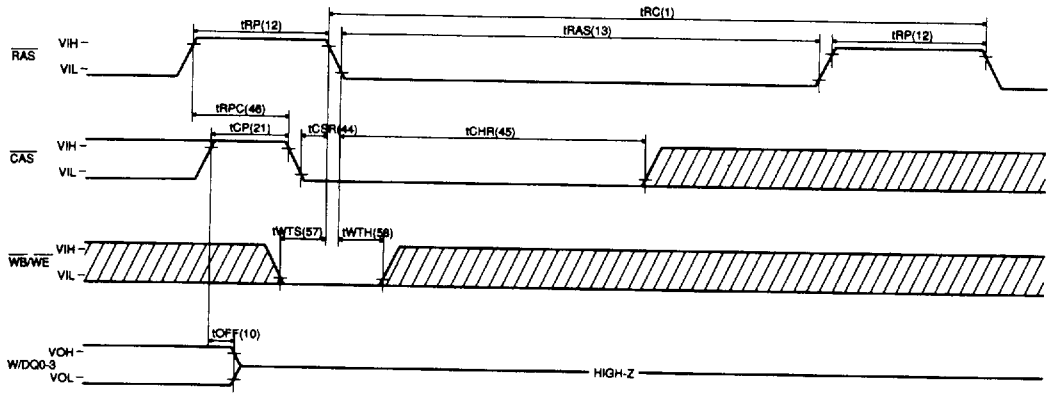
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



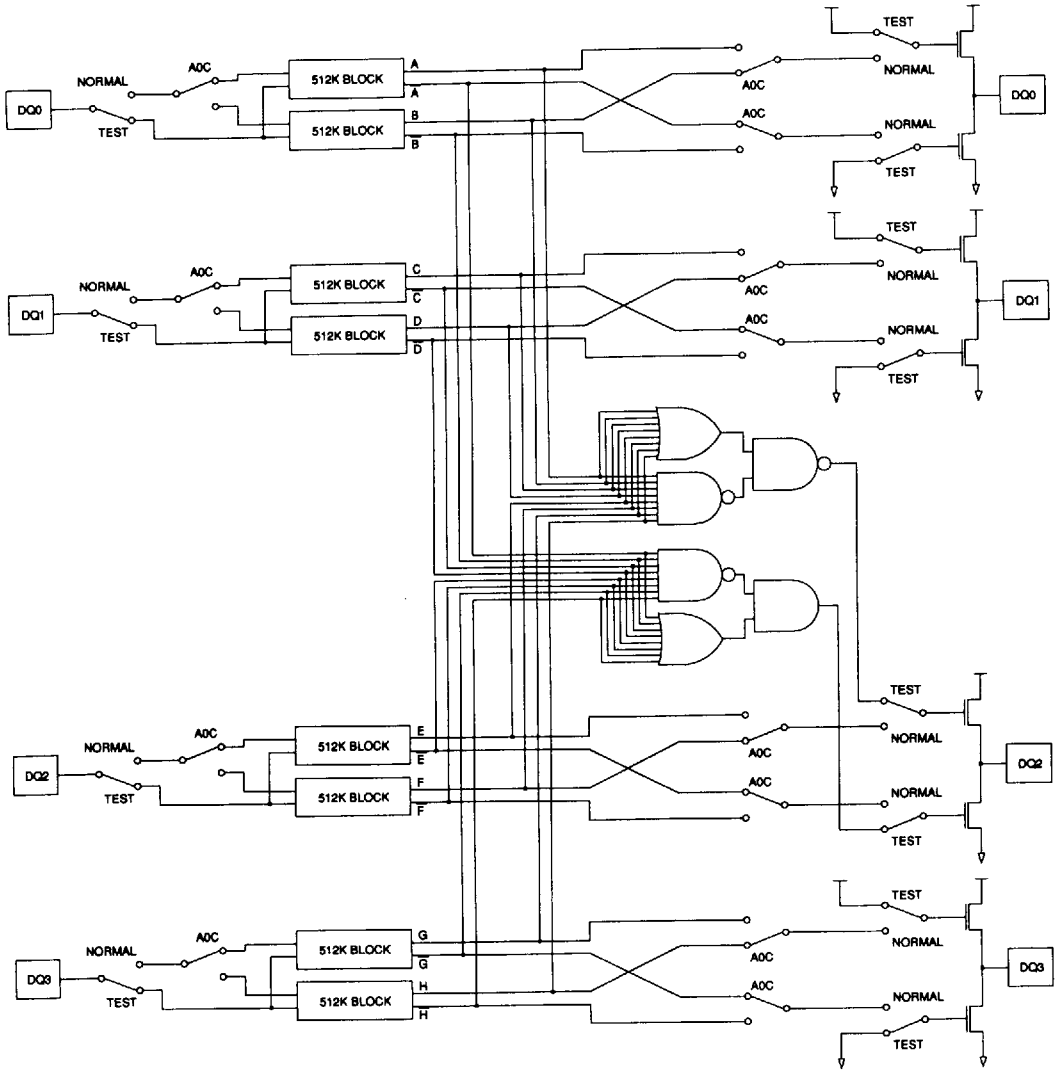
TEST MODE

The HY514410B is a DRAM organized 1,048,576 x 4-bit. It is internally organized 524,288 x 8-bit. In Test Mode, data are written into 8 sectors (Each is composed of 512K bits) in parallel and retrieved the same way. Column address A0 is not used. If, upon reading, all 8-bit data from 8 sectors are equal (all "1"s or "0"s), the DQ2 pin indicates a "1". If they are not equal, the DQ2 pin indicates a "0". The DQ0, DQ1 and DQ3 pins always indicate a "1" in Test Mode Read cycles. The diagram below shows the timing of the HY514410B to enter Test Mode. In Test Mode, the 1Mx4 DRAM can be tested as if it were a 512Kx4 DRAM. $\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$ cycle (Test Mode In Cycle) puts the HY514410B into Test Mode and $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycle puts it back into Normal Mode. In Test Mode, $\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$ cycle shall be used for the refresh operation. The Test Mode function reduces test time.(1/2 in case of N test pattern)

TEST MODE IN CYCLE



BLOCK DIAGRAM IN TEST MODE



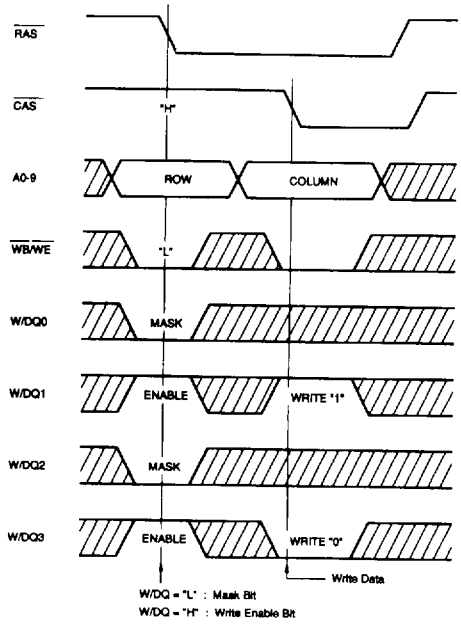
WRITE-PER-BIT FUNCTION

The Write-Per-Bit function selectively controls the internal write enable circuit of the HY514410B. When $\overline{WB/WE}$ is held "Low" at the falling edge of $\overline{RAS}$ during a random access operation, the write mask is enabled. At the sametime, the mask data on the W/DQ pins is located onto the write mask register (WMR). When a "0" is sensed on any of the W/DQ pins, their corresponding write circuits are disabled and new data will not be written. When "1" is sensed on any of the W/DQ pins, their corresponding write circuit will remain enabled so that new data is written. The truth table of the Write-Per-Bit function and an example of the Write-Per-Bit function illustrating its application to displays are shown below.

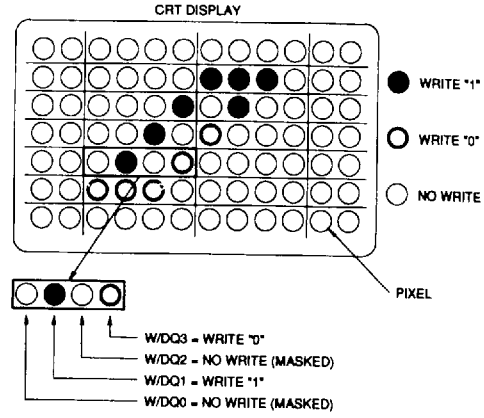
TRUTH TABLE FOR WRITE-PER-BIT FUNCTION

at the falling edge of $\overline{RAS}$			
$\overline{CAS}$	$\overline{WB/WE}$	W/DQ0-3	Function
H	H	Don't Care	Write Enable
H	L	1	Write Enable
		0	Write Mask

WRITE-PER-BIT TIMING DIAGRAM

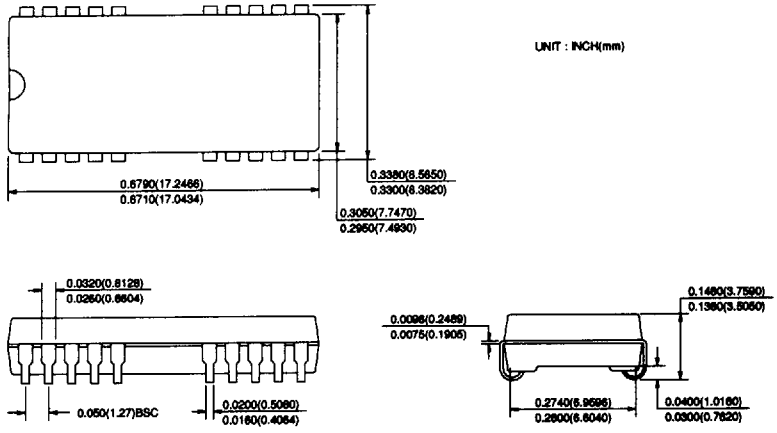


CORRESPONDING BIT MAP

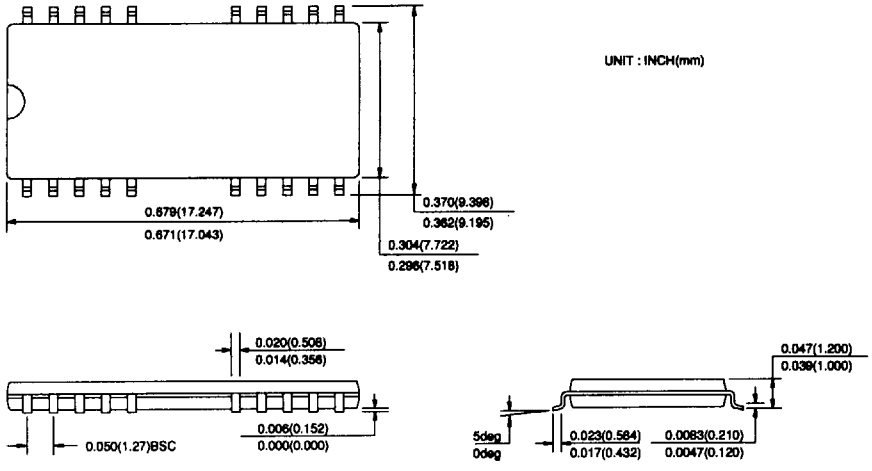


PACKAGE INFORMATION

300 mil 20/26 pin Small Outline J-form Package (J)



300 mil 20/26 pin Thin Small Outline Package (T) (R)

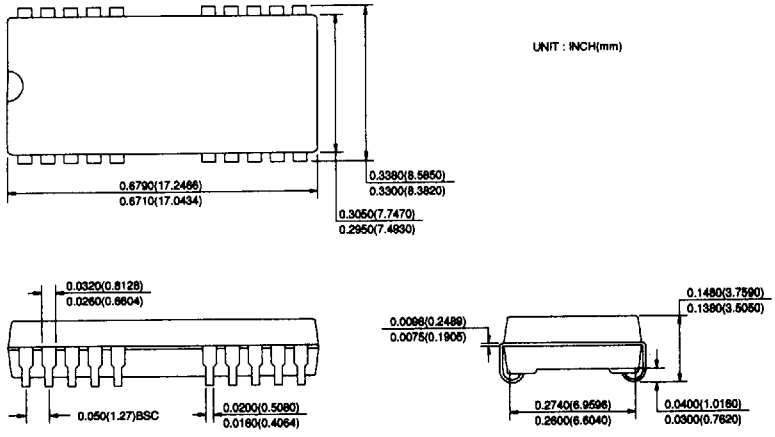


ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY514410BJ	50/60/70		SOJ
HY514410BLJ	50/60/70	L-part	SOJ
HY514410BSLJ	50/60/70	SL-part	SOJ
HY514410BT	50/60/70		TSOP-II
HY514410BLT	50/60/70	L-part	TSOP-II
HY514410BSLT	50/60/70	SL-part	TSOP-II
HY514410BR	50/60/70		TSOP-II(R)
HY514410BLR	50/60/70	L-part	TSOP-II(R)
HY514410BSLR	50/60/70	SL-part	TSOP-II(R)

PACKAGE INFORMATION

300 mil 20/26 pin Small Outline J-form Package (J)



300 mil 20/26 pin Thin Small Outline Package (T) (R)