APR 13 1993

DPZ128X16A3

128K x 16 FLASH EEPROM DENSE-STACK MODULE

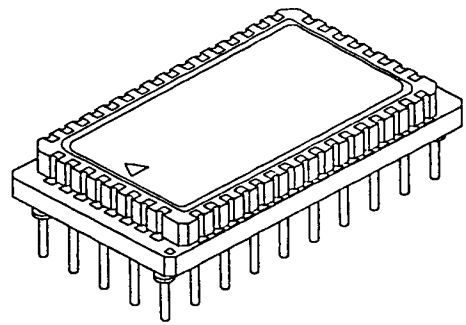
PRELIMINARY

DESCRIPTION:

The DPZ128X16A3 "DENSE-STACK" module is a revolutionary new memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC) mounted on a co-fired ceramic substrate. It offers 2 Megabits of FLASH EEPROM in a single package envelope of .990" x .540" x .205".

The DPZ128X16A3 is built with a SLCC package containing two 128K x 8 FLASH memory devices. Each SLCC is hermetically sealed making the module suitable for commercial, industrial and military applications.

By using SLCCs, the "Dense-Stack" family of modules offers a higher board density of memory than available with conventional through-hole, surface mount, module, or most hybrid techniques.

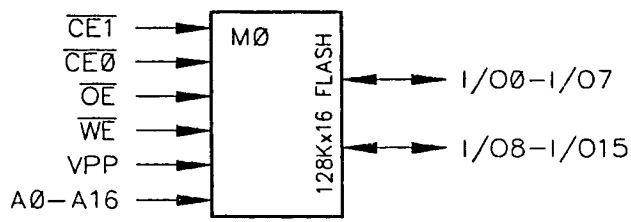


FEATURES:

- Organization: 128K x 16 or 256K x 8
- Fast Access Times:
  120*, 150, 170, 200, 250ns (max.)
- Fully Static Operation
  - No clock or refresh required
- TTL Compatible Inputs and Outputs
- Common Data Inputs and Outputs
- Automatic Erase Function
  - Reduces CPU overhead
- 10,000 Erase/Program Cycles (min.)
- 50 - Pin PGA "DENSE-STACK" Package

* Available in commercial only.
** $\overline{CE0}$ controls I/O0 - I/O7, $\overline{CE1}$ controls I/O8 - I/O15.

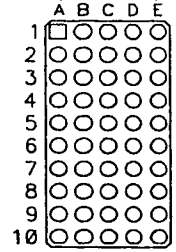
FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM

	A	B	C	D	E
1	$\overline{CE1}$	N.C.	N.C.	N.C.	N.C.
2	VSS	N.C.	N.C.	VPP	VDD
3	N.C.	A16	$\overline{WE}$	N.C.	A15
4	A14	A12	A7	A8	A13
5	A6	A5	$\overline{OE}$	A11	A9
6	A4	A3	A2	$\overline{CE0}$	A10
7	A1	A0	I/O13	I/O12	I/O11
8	I/O10	I/09	I/O8	I/O15	I/O14
9	VSS	I/01	I/03	I/05	VDD
10	I/O0	I/02	I/04	I/06	I/O7

(TOP VIEW)



PIN NAMES

A0 - A16	Address Inputs
I/O0 - I/O15	Data Input/Output
$\overline{CE0}$, $\overline{CE1}$	Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{PP}	Programming Voltage (+12.5V)
V_{DD}	Power (+5V)
V_{SS}	Ground

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DEVICE OPERATION:

The FLASH devices are electrically erasable and programmable memory that functions similar to an EPROM device, but can be erased without being removed from the system and exposed to ultraviolet light. Each 128K x 8 device can be erased individually eliminating the need to re-program the entire module when partial code changes are required.

READ:

With V_{PP} = 0V to V_{DD} *(V_{PPLO})*, the devices are read-only memories and can be read like a standard EPROM. By selecting the device to be read *(see Truth Table and Functional Block Diagram)*, the data programmed into the device will appear on the appropriate I/O pins.

When V_{PP} = +12.5V ± 5.0V *(V_{PPHI})*, reads can be accomplished in the same manner as described above but must be preceded by writing 00H to the command register prior to reading the device. When V_{PP} is raised to V_{PPHI} the contents of the command register default to 00H and remain that way until the command register is altered.

STANDBY:

When the appropriate $\overline{CE}$'s are raised to a logic-high level, the standby operation disables the FLASH devices reducing the power consumption substantially. The outputs are placed in a high- impedance state, independent of the $\overline{OE}$ input. If the module is deselected during programming, erasure, or autoerase, the device upon which the operation was being performed, will continue to draw active current until the operation is completed.

PROGRAM:

The programming and erasing functions are accessed via the command register when high voltage is applied to V_{PP}. The contents of the command register control the functions of the memory device *(see Command Definition Table)*.

The command register is not an addressable memory location. The register stores the address, data, and command information required to execute the command. When V_{PP} = V_{PPLO} the command register is reset to 00H returning the device to the read-only mode.

The command register is written by enabling the device upon which that the operation is to be performed *(see Functional Block Diagram)*. While the device is enabled bring $\overline{WE}$ to a logic-low (V_{IL}), the address is latched on the falling edge of $\overline{WE}$ and data is latched on the rising edge of $\overline{WE}$. Programming is initiated by writing 40H *(program setup command)* to the command register. On the next falling edge of $\overline{WE}$ the address to be programmed will be latched followed by the data being latched on the rising edge of $\overline{WE}$ *(see AC Operating and Characteristics Table)*.

PROGRAM VERIFY:

The FLASH devices are programmed one byte at a time. Each byte may be programmed sequentially or at random. Following each programming operation, the byte must be verified.

To initiate the program-verify mode, C0H must be written to the command register of the device just programmed. The programming operation is terminated on the rising edge of $\overline{WE}$ the program-verify command is written to the command register.

After the program-verify command is written to the command register, the memory device applies an internally generated margin voltage to the byte just written. After waiting 6µs the data byte can be verified by doing a read. If true data is read from the device, the byte write was successful and the next byte may be programmed.

If the device fails to verify, the program/verify operation is repeated up to 20 times.

ERASE:

The erase function is a command-only operation and can only be executed while V_{PP} = V_{PPHI}.

To setup the chip-erase, 20H must be written to the command register. The chip-erase is then executed by once again writing 20H to the command register *(see AC Operating and Characterstics Table)*.

To ensure a reliable erasure, all bits in the device to be erased should be programmed to their charged state *(data = 00H)* prior to starting the erase operation. With the algorithm provided, this operation should take approximately 2 minutes.

ERASE VERIFY:

The erase operation erases all bytes in the device selected in parallel. Upon completion of the erase operation, each byte must be verified. This operation is initiated by writing A0H to the command register. The address to be verified must be supplied because it is latched on the falling edge of $\overline{WE}$.

The memory device internally generates a margin voltage and applies it to the addressed byte. If FFH is read from the device, it indicates the byte is erased. The erase/verify command is issued prior to each byte verification to latch the address of the byte to be verified. This continues until FFH is not read from the device or the last address for the device being erased is read.

If FFH is not read from the byte being verified, an additional erase operation is performed. Verification then resumes from the last byte verified. Once all locations in the device being erased are verified, the erase operation is complete. The verify opertation should now be terminated by writing a valid command such as program set-up to the command register.

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AUTOMATIC ERASE:

An automatic erase function is also available eliminating the need to program all locations to 00H or do an erase verify. The automatic erase will program all locations to 00H and do a continuous erase/verify until all locations in the device are erased.

To setup the chip-erase, 30H must be written to the command register. The chip-erase is then executed by once again writing 30H to the command register *(see AC Operating Characteristics Table)*.

To determine if the automatic erase cycle is complete, the most-significant (MSB) I/O pin for the device being erased (I/O7, I/O15) is read. If the data = 0 on each of these bits, the cycle is not complete. The erase cycle is complete when the data = 1 on the MSB of the device being erased.

DESIGN CONSIDERATIONS:

V_{PP} traces should use similar trace widths and layout considerations as the V_{DD} power bus. The V_{PP} supply traces should also be decoupled to help decrease voltage spikes.

Power-up sequencing should be such that V_{PP} doesn't go above V_{DD} + 2.0V before V_{DD} reaches a steady state voltage, while on power-down V_{PP} should be below V_{DD} + 2.0V before V_{DD} is lowered.

It is recommended that a 4.7µF to 10µF electrolytic capacitor be placed near the memory module connected accross V_{DD} and V_{SS} for bulk storage. Decoupling capacitors should also be placed near the module connected across V_{PP} and V_{SS}.

COMMAND DEFINITION TABLE

COMMAND	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation	Address	Data	Operation	Address	Data
Read Memory	1	Write	X	00H	-	-	-
Setup Erase / Erase	2	Write	X	20H	Write	X	20H
Erase Verify	2	Write	EA	A0H	Read	X	EVD
Setup Autoerase / Autoerase	2	Write	X	30H	Write	X	30H
Setup Program / Program	2	Write	X	40H	Write	PA	PD
Program Verify	2	Write	X	C0H	Read	X	PVD
Reset	2	Write	X	FFH	Write	X	FFH

EA = Address to Verify
EVD = Data Read from Location EA

PA = Address to Program
PD = Data to be Programmed at Location PA
PVA = Data to be Read from Location PA at Program Verify

TRUTH TABLE

MODE	DESCRIPTION	$\overline{CE}$n	$\overline{WE}$	$\overline{OE}$	V_{PP}	I/O Pins	Supply Current
READ ONLY	Not Selected	H	X	X	V_{PPLO}	High-Z	Standby
	Output Disable	L	H	H	V_{PPLO}	High-Z	Active
	Read	L	H	L	V_{PPLO}	DOUT	Active
COMMAND PROGRAM	Not Selected	H	X	X	V_{PPHI}	High-Z	Standby
	Output Disable	L	H	H	V_{PPHI}	High-Z	Active
	Read	L	H	L	V_{PPHI}	DOUT	Active
	Write	L	L	H	V_{PPHI}	DIN	Active

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PRELIMINARY

RECOMMENDED OPERATING RANGE[1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{PP}	Programming Voltage [2]	12.0	12.5	13.0	V
V_{IL}	Input LOW Voltage	-0.3[3]		0.8	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+1.0	V
T_A	Operating Temp.	-55	+25	+125	°C

CAPACITANCE [5]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	20	pF	V_{IN}[3] = 0V
C_{CE}	Chip Enable	15		
C_{WE}	Write Enable	20		
C_{OE}	Output Enable	20		
$C_{I/O}$	Data Input/Output	15		

ABSOLUTE MAXIMUM RATINGS [4]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
$V_{I/O}$	Input/Output Voltage [1]	-0.6 to +7.0 [3]	V
V_{PP}	V_{PP} Supply Voltage [1] During Erase/Program	-0.6 to +14.0	V
V_{DD}	Supply Voltage [1]	-0.6 to +7.0	V

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH}= -400µA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL}=2.1mA	-	0.45	V

DC OPERATING CHARACTERISTICS: Over operating ranges							
Symbol	Characteristics	Test Conditions		TYP. (*)	Limits Min.	Limits Max.	Unit
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}		-	-4	+4	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}		-	-2	+2	µA
I_{CC1}	Active Supply Current	$\overline{CE0}$ = V_{IL}, $\overline{CE1}$ = V_{IH} or $\overline{CE1}$ = V_{IL}, $\overline{CE0}$ = V_{IH}; V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 0mA, f = 0MHz	x8	7		16	mA
			x16	15		35	
I_{CC2}	Operating Supply Current	$\overline{CE0}$ = V_{IL}, $\overline{CE1}$ = V_{IH} or $\overline{CE1}$ = V_{IL}, $\overline{CE0}$ = V_{IH}; V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 0mA, f = 8MHz	x8	25		50	mA
			x16	50		100	
I_{CC3}	V_{DD} Programming Current	Programming in Progress	x8	3		20	mA
			x16	5		40	
I_{CC4}	V_{DD} Erase Current	Erasure in Progress	x8	15		45	mA
			x16	20		80	
I_{SB1}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}				2	mA
I_{SB2}	Full Standby Supply Current (CMOS)	$\overline{CE}$ = V_{DD} -0.2V				400	µA
I_{PPS}	V_{PP} Leakage Current	V_{PP} = V_{PPLO}				40	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPHI}				2.5	mA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPHI}, Programming in Progress	x8	5		35	mA
			x16	8		60	
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPHI}, Erasure in Progress	x8	35		80	mA
			x16	70		160	

* Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.

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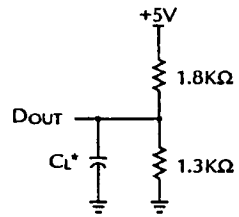
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Timing Reference Levels During Verify	0.8V and 2.4V

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	100 pF	except t_{DF}
2	30 pF	t_{DF}

Figure 1. Output Load

* Including Probe and Jig Capacitance.



AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges												
No.	Symbol	Parameter	-120		-150		-170		-200		-250		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{CE}	Chip Enable Access Time		120		150		170		200		250	ns
2	t_{ACC}	Address Access Time		120		150		170		200		250	ns
3	t_{OE}	Output Enabe Access Time		60		70		75		80		90	ns
4	t_{DF}	Output Disable to Output in HIGH-Z [5, 6]	0	40	0	50	0	55		60		70	ns
5	t_{OH}	Output Hold from Address Change	5		5		5		5		5		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges												
No.	Symbol	Parameter	-120		-150		-170		-200		-250		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
6	t_{CWC}	Write Cycle Time	120		150		170		200		250		ns
7	t_{AS}	Address Setup Time	0		0		0		0		0		ns
8	t_{AH}	Address Hold Time	60		60		60		60		60		ns
9	t_{DS}	Data Setup Time	50		50		50		50		50		ns
10	t_{DH}	Data Hold Time	10		10		10		10		10		ns
11	t_{CES}	Chip Enable Setup Time	0		0		0		0		0		ns
12	t_{CEH}	Chip Enable Hold Time	15		15		15		15		15		ns
13	t_{VPS}	V_{PP} Setup Time [7, 8]	100		100		100		100		100		ns
14	t_{VPH}	V_{PP} Hold Time [7, 8]	100		100		100		100		100		ns
15	t_{WEP}	Write Enable Pulse Width	70		70		80		80		90		ns
16	t_{WEH}	Write Enable Pulse Width HIGH Time	20		20		20		20		20		ns
17	t_{OEWS}	Output Enable Setup Time before Command Programming	0		0		0		0		0		ns
18	t_{OERS}	Output Enable Setup Time before Verify	6		6		6		6		6		µs
19	t_{VA}	Verify Access Time		120		150		170		200		250	ns
20	t_{OEPS}	Output Enable Setup Time before Status Polling	20		20		20		20		20		ns
21	t_{SPA}	Status Polling Access Time		120		150		170		200		250	ns
22	t_{PPW}	Standby Time before Programming	25		25		25		25		25		µs
23	t_{ET}	Standby Time in Erase	11		11		11		11		11		ms
24	t_{AET}	Total Erase Time in Autoerase [9]	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	S

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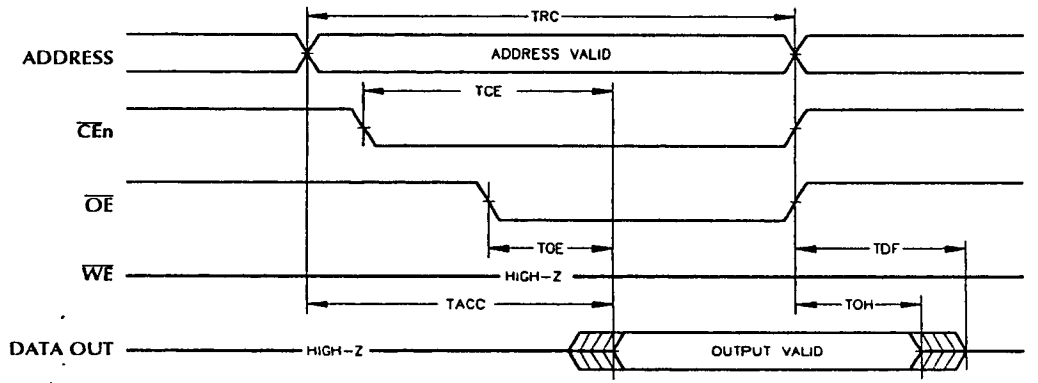
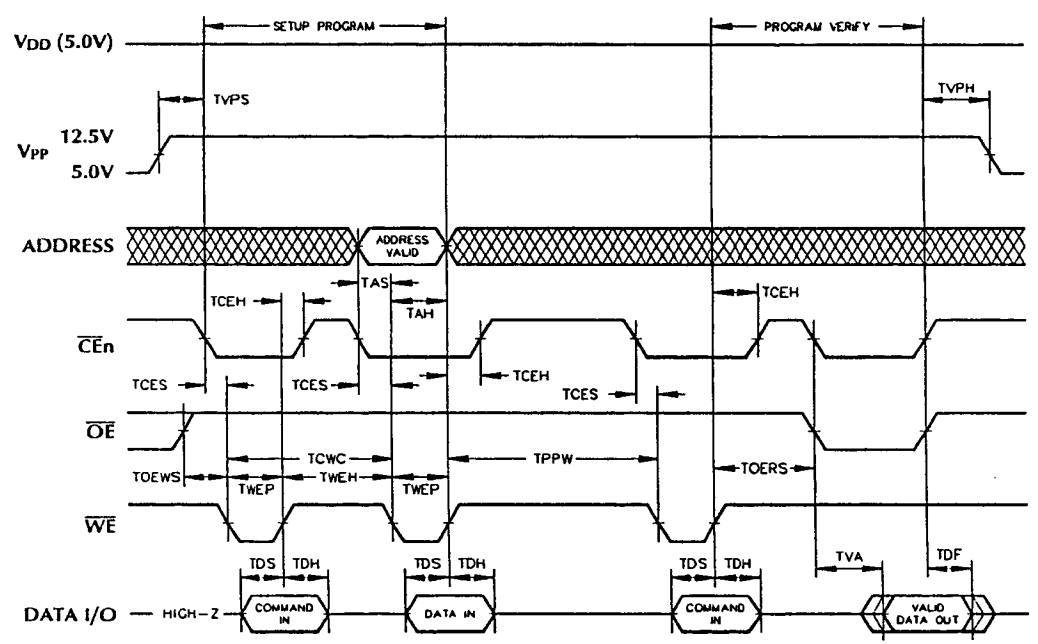
READ CYCLE



PROGRAMMING CYCLE



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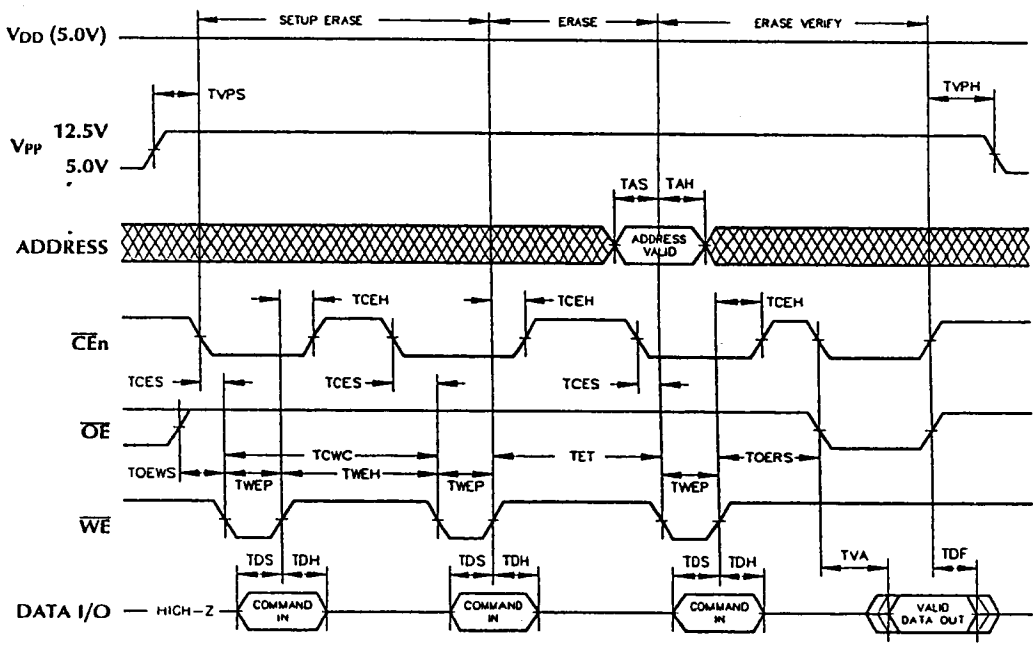
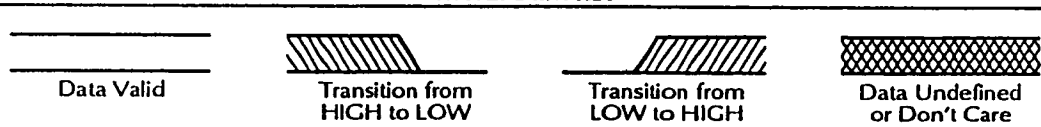
ERASE CYCLE



WAVEFORM KEY



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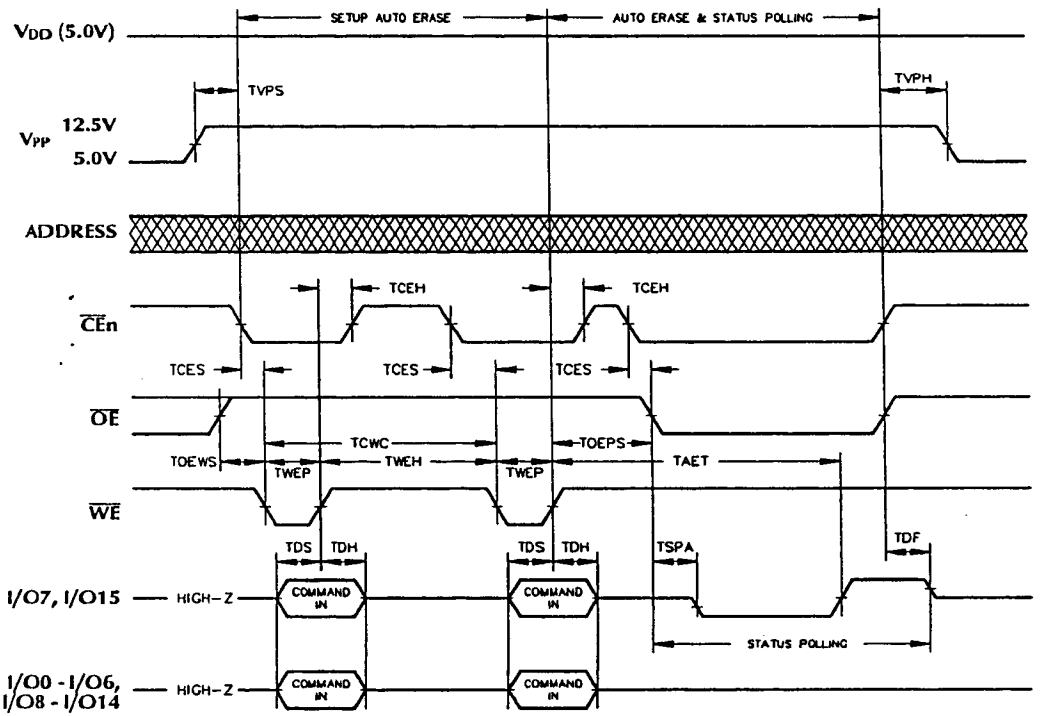
AUTOMATIC ERASE CYCLE



NOTES:

1. All voltages are with respect to V_{SS}.
2. When operating device at temperatures less than 0°C (-55°C to 0°C), V_{PP} must be 7.4 Vdc above V_{DD} durring Program/Erase functions.
3. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.6V at DC level).
4. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. This parameter is guaranteed and not 100% tested.
6. Transition is measured at the point of ±500mV from steady state voltage.
7. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
8. V_{PP} must not exceed 14V, including overshoot.
9. The total erase times shown are for one (1) 128Kx8 device, to erase the entire module would be 2x the times shown.

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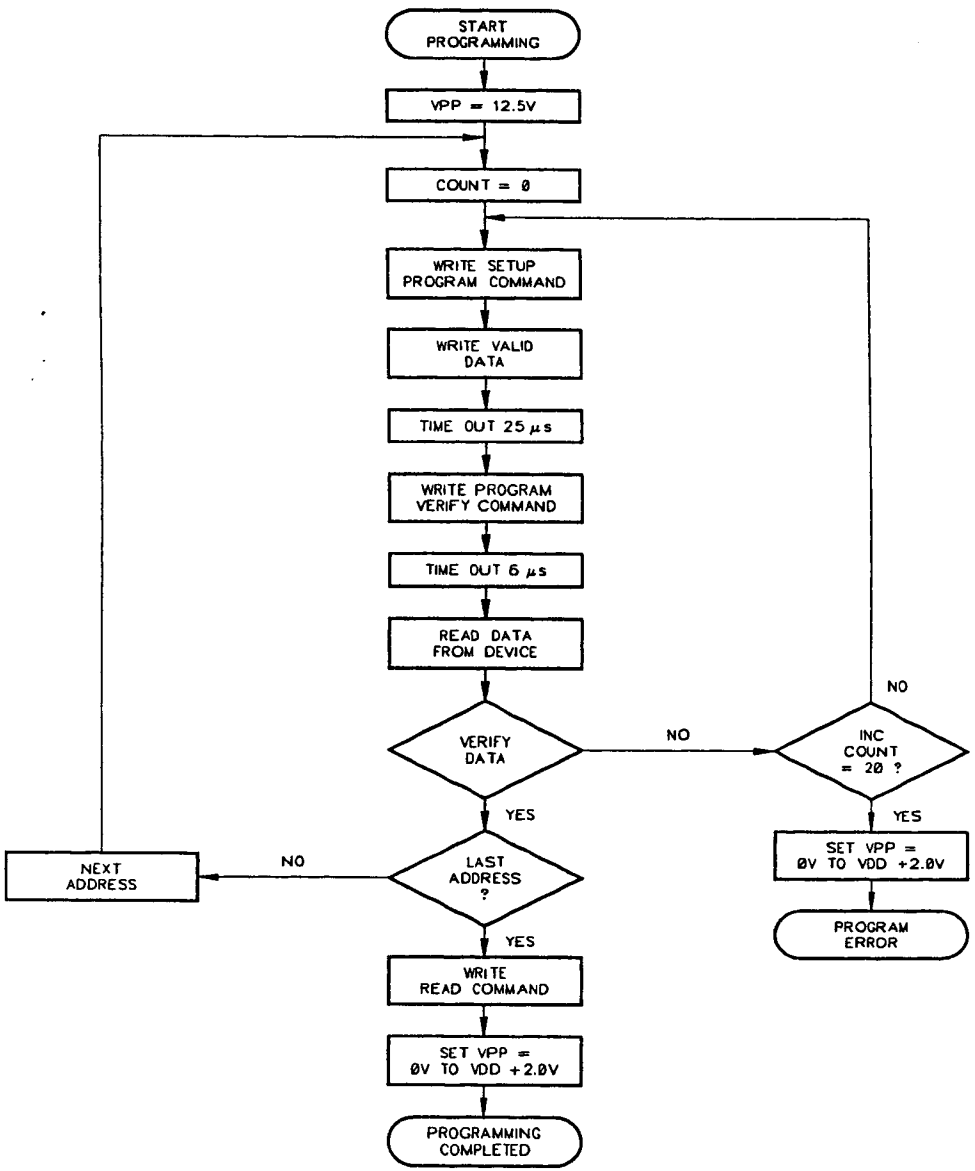
WRITE ALGORITHM



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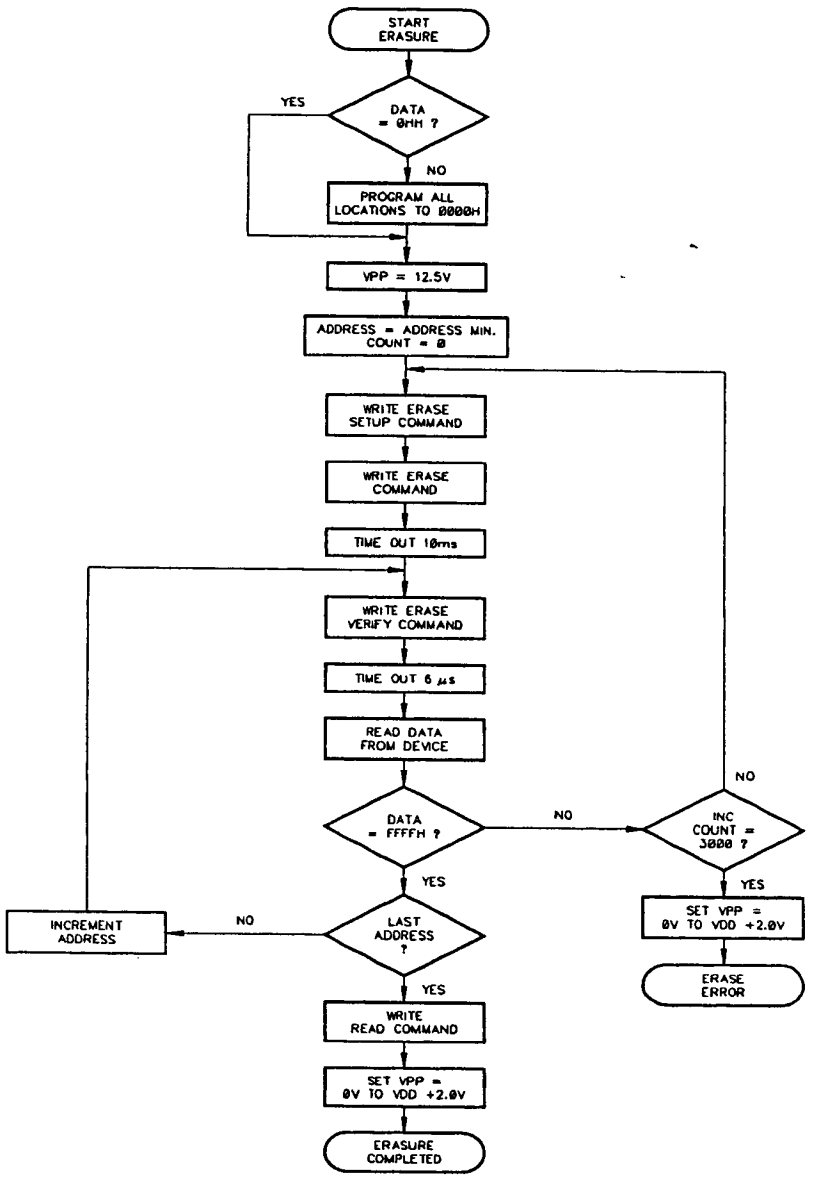
ERASE ALGORITHM



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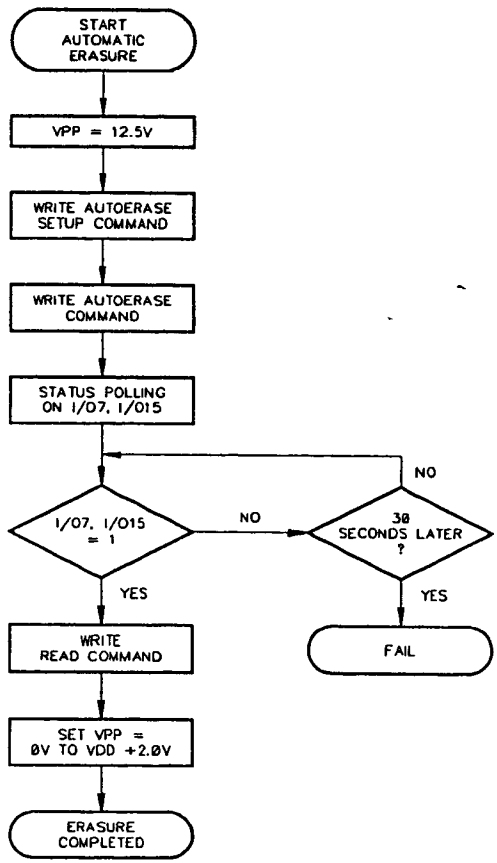
AUTOMATIC ERASE



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PRELIMINARY

ORDERING INFORMATION

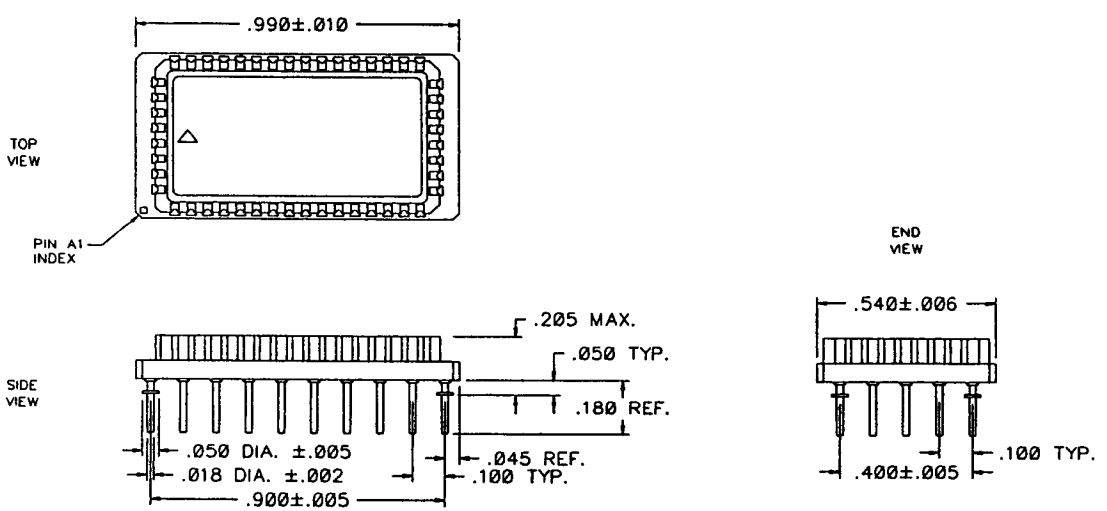
DP Z 128 X 16 A3 – XX X
PREFIX TYPE DEPTH DESIG. WIDTH PACKAGE SPEED GRADE

C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	-40°C to +85°C
M	MILITARY	-55°C to +125°C
B	MIL-PROCESSED	-55°C to +125°C

12 120ns (COMMERCIAL ONLY)
15 150ns
17 170ns
20 200ns
25 250ns

50 PIN PGA/3-D DENSE-STACK
BYTE CONTROLLED WITHOUT LOGIC
FLASH EEPROM

MECHANICAL DRAWING



Dense-Pac Microsystems, Inc.
7321 Lincoln Way ◆ Garden Grove, California 92641-1428
(714) 898-0007 ◆ (800) 642-4477 (Outside CA) ◆ FAX: (714) 897-1772

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