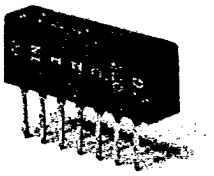
SERIES DL6250 7 PIN SINGLE-IN-LINE DIGITAL DELAY MODULES

- Minimum Board Space Required • Low Profile Encapsulation Construction • 4 Equally Space Taps
- TTL and DTL Compatible

Specifications



- Supply Voltage : 4.75 to 5.25VDC
- Logic 1 Input Current : 50μA Max
- Logic 0 Input Current : −2mA Max
- Logic 1 Volt Out : 2.5v Min
- Logic 0 Volt Out : 0.5v Max
- Logic 1 Fan-Out : 20/Tap Max
- Logic 0 Fan-Out : 10/Tap Max
- Power Dissipation : 240mW Total
- Operating Temp Range : 0°C to 70°C
- Temp Coefficient : 100PPM/°C

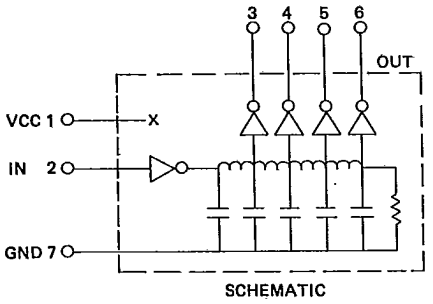
Input Test Conditions

- Input Pulse Voltage : 3.2v
- Input Rise Time : ⩽ 3NS
- Input Current : 60mA Typ.
- Pulse Width : Min 40% of Total Delay

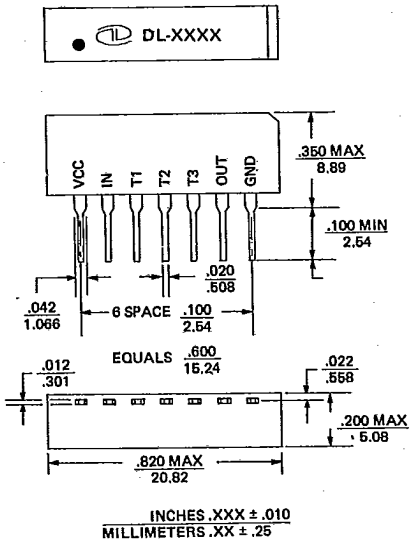
Electrical Specifications at 25°C (measured with no loads on Taps)

Part Number	Total Delay Nanosecond	Tap to Tap Delay NS (1)	Rise Time NS Max (2)
DL6251*	5 ± 1	1.2 ± 0.5	2
DL6252*	6 ± 1	1.5 ± 0.5	2
DL6253*	8 ± 2	2.0 ± 0.5	2
DL6254*	10 ± 2	2.5 ± 1.0	2
DL6255*	12 ± 2	3.0 ± 1.0	2
DL6256*	16 ± 2	4.0 ± 1.0	2
DL6257	20 ± 3	5.0 ± 2.0	3
DL6258	30 ± 3	7.5 ± 2.0	3
DL6259	32 ± 3	8.0 ± 2.0	3
DL6260	40 ± 3	10.0 ± 2.0	3
DL6261	48 ± 3	12.0 ± 2.0	3
DL6262	50 ± 3	12.5 ± 2.0	4
DL6263	60 ± 3	15.0 ± 2.0	4
DL6264	80 ± 3	20.0 ± 2.0	4
DL6265	100 ± 3	25.0 ± 2.0	5
DL6236	120 ± 3	30.0 ± 2.0	5
DL6267	160 ± 3	40.0 ± 2.0	5
DL6268	200 ± 3	50.0 ± 2.5	5

Note: (1) Measured at 1.5v level leading edge, Tol. ±5% or ±2NS, whichever is greater.
(2) Measured from 0.75v to 2.4v.
* Time Delay measurements referenced to 1st Tap



SCHEMATIC



INCHES .XXX ± .010
MILLIMETERS .XX ± .25