ALPHA SEMICONDUCTOR

Excellence in Analog Power Products

AS429

6A, Single High-Speed CMOS Power MOSFET Drivers

FEATURES

- Latch Up Protected > 1.5A
- Logic Input Swing Negative 5V
- ESD 4kv
- Matched Rise and Fall Times 20ns
- Pin-to-Pin Compatible with TC429

APPLICATIONS

- Motor Controls
- Switch-Mode Power Supplies
- Pulse Transformer Driver
- Class D Switching Amplifiers

PRODUCT DESCRIPTION

The ALPHA Semiconductor AS429 is a high-speed, single CMOS-level translator and driver. Designed specifically to drive highly capacitive power MOSFET gates, the AS429 features 2.5Ω output impedance and 6A peak output current drive.

A 2500 pF capacitive load will be driven 18V in 25ns. Delay time through the devices is 60ns. The rapid switching times with large capacitive loads minimize MOSFET transition power loss.

The CMOS design minimizes quiescent power supply current. With a logic 1 input, power supply current is 5mA maximum and decreases to 0.5mA for logic 0 inputs.

For dual devices, see the AS426/AS427/AS428 data sheet.

For non-inverting applications, or applications requiring latch-up protection, see the AS4420/AS4429 data sheet.

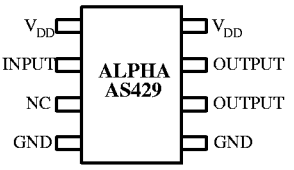
ORDERING INFORMATION

Part Number	Temperature Range	Package Type
AS429XP	0°C to +70°C	8-Pin PDIP
AS429XP	-40°C to +85°C	8-Pin PDIP
AS429XP	-55°C to +125°C	8-Pin PDIP
AS429XS	0°C to +70°C	SOIC-8
AS429XS	-40°C to +85°C	SOIC-8
AS429XS	-55°C to +125°C	SOIC-8

X= I Industrial; C Commercial; M Military

PIN CONNECTIONS

8-Pin Surface Mount/PDIP



Top View

ABSOLUTE MAXIMUM RATINGS

Supply Voltage..... +20V
Input Voltage, Any Terminal..... V_{DD} +0.3V to GND -0.3V
Power Dissipation
Plastic..... 500 mW
CERDIP..... 800 mW
Derating Factors
Plastic..... 5.6mW/°C Above 36°C
CERDIP..... 6mW/°C

Operating Temperature Range
C Version..... 0°C to +70°C
I Version..... -25°C to +85°C
M Version..... -55°C to +125°C

Maximum Chip Temperature..... +150°C
Storage Temperature Range..... -65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

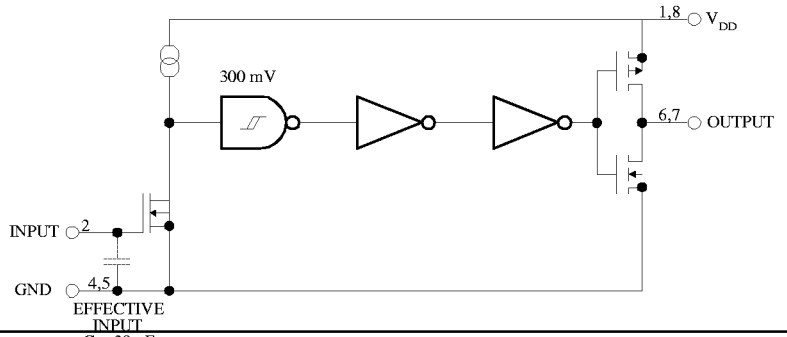
ELECTRICAL CHARACTERISTICS

T_A = +25°C with 7V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input						
Logic 1, High Input Voltage	V_{IH}		2.4	1.8	-	V
Logic 0, Low Input Voltage	V_{IL}		-	1.3	0.8	V
Input Current	I_{IN}	0V ≤ V_{IN} ≤ V_{DD}	-10	-	10	µA
Output						
High Output Voltage	V_{OH}		V_{DD} - 0.025	-	-	V
Low Output Voltage	V_{OL}		-	-	0.025	V
Output Resistance	R_O	V_{IN} = 0.8V I_{OUT} = 10mA, v_{DD} = 18V V_{IN} = 2.4V I_{OUT} = 10mA, v_{DD} = 18V	- -	1.8 1.5	2.5 2.5	Ω Ω
Peak Output Current	I_{PK}	V_{DD} = 18V (See Figure 3)	-	6	-	A
Switching Time (Note 1)						
Rise Time	t_R	Figure 1, C_L = 2500pF	-	23	35	ns
Fall Time	t_F	Figure 1, C_L = 2500 F	-	25	35	ns
Delay Time	t_{D1}	Figure 1	-	53	75	ns
Delay Time	t_{D2}	Figure 1	-	60	75	ns
Power Supply						
Power Supply Current	I_S	V_{IN} = 3V V_{IN} = 0V	- -	3.5 0.3	5 0.5	mA mA

Notes: Switching times guaranteed by design.

TYPICAL APPLICATION



ELECTRICAL CHARACTERISTICS

Over operating temperature with 7V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input						
Logic 1, High Input Voltage	V_{IH}		2.4	-	-	V
Logic 0, Low Input Voltage	V_{IL}		-	-	0.8	V
Input Current	I_{IN}	0V ≤ V_{IN} ≤ V_{DD}	-10	-	10	µA
Output						
High Output Voltage	V_{OH}		V_{DD} - 0.025	-	-	V
Low Output Voltage	V_{OL}		-	-	0.025	V
Output Resistance	R_O	V_{IN} = 0.8V I_{OUT} = 10mA, v_{DD} = 18V	-	-	5	Ω
		V_{IN} = 2.4V I_{OUT} = 10mA, V_{DD} = 18V	-	-	5	Ω
Switching Time (Note 1)						
Rise Time	t_R	Figure 1, C_L = 2500pF	-	-	70	ns
Fall Time	t_F	Figure 1, C_L = 2500pF	-	-	70	ns
Delay Time	t_{D1}	Figure 1	-	-	100	ns
Delay Time	t_{D2}	Figure 1	-	-	120	ns
Power Supply						
Power Supply Current	I_S	V_{IN} = 3V	-	-	12	mA
		V_{IN} = 0V	-	-	1	mA

Notes: **Switching times guaranteed by design.**

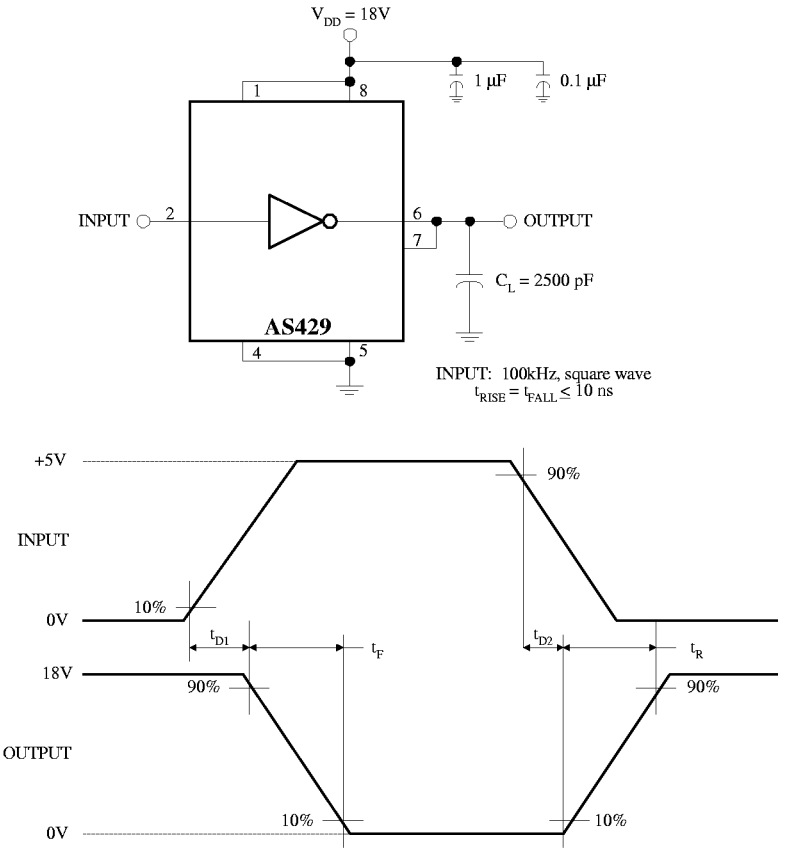


Figure 1. Inverting Driver Switching Time Test Circuit

SUPPLY BYPASSING

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 2500pF pad 18V in 25ns requires a 1.8A current from the device's power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic disk capacitors with short lead lengths (<0.5 in.) should be used. A 1µF film capacitor in parallel with one or two 0.1 µF ceramic disk capacitors normally provides adequate bypassing.

GROUNDING

The high-current capability of the AS429 demands careful PC board layout for best performance. Since the AS429 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. The feedback is especially noticeable with slow rise-time inputs, such as those produced by an open-collector includes about 300mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 2 shows the feedback effect in detail. As the AS429 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05Ω of PC trace resistance can produce hundreds of millivolts at the AS429 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillations may result.

To ensure optimum device performance, separate ground traces should be provided for the logic and power connections. Connecting logic ground directly to the AS429 GND pins ensures full logic drive to the input and fast output switching. Both GND pins should be connected to power ground.

INPUT STAGE

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 3mA current source load. With a logic "1" input, the maximum quiescent supply current is 5mA. Logic "0" input level signals reduce quiescent current to 500µA maximum.

The AS429 input is designed to provide 300 mV of hysteresis, providing clean transitions and minimizing output stage current spiking when changing states. Input voltage levels are approximately 1.5V, making the device TTL compatible over the 7V to 18V operating supply range. Input current is less than 10µA over this range.

The AS429 can be directly driven by LT494, SG1526/1527, SG1524, SE5560 or similar switch-mode power supply integrated circuits. By off-loading the power-driving duties to the AS429, the power supply controller can operate at lower dissipation, improving performance and reliability.

POWER DISSIPATION

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as the 4000 and 74C have outputs that can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The AS429, however, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

The supply current versus frequency and supply current versus capacitive load characteristic curves will aid in determining power dissipation calculations. Table 1 lists the maximum power dissipation calculations. Table 1 lists the maximum operating frequency for several power supply voltages when driving a 2500pF load. More accurate power dissipation figures can be obtained by summing the three power sources.

Input signal duty cycle, power supply voltage, and capacitive load influence package power dissipation. Given power dissipation and package thermal resistance, the maximum ambient operation temperature is easily calculated. The 8-pin CERDIP junction-to-ambient thermal resistance is 150 °C/W. At +25°C, the package is rated at 800mW maximum dissipation. Maximum allowable chip temperature is +150°C.

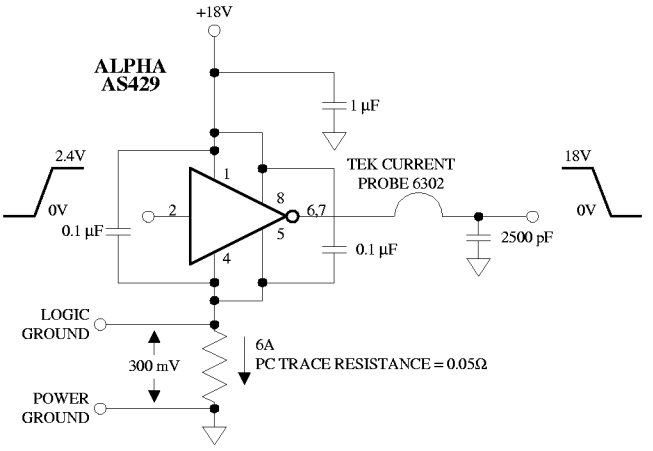


Figure 2. Switching Time Degradation die to Negative Feedback

Three Components make up total package power dissipation.

(1) Capacitive load dissipation (P_C)
(2) Quiescent power (P_Q)
(3) Transition power (P_T)

The capacitive load-caused dissipation is a direct function of frequency, capacitive load, and supply voltage. The package power dissipation is

$$P_C = f\ C\ V_S^2,$$

where: f = Switching frequency
C = Capacitive load
V_S = Supply voltage

Quiescent power dissipation depends on input signal duty cycle. A logic low input results in a low-power dissipation mode with only 0.5 mA total current drain. Logic high signals raise the current to 5mA maximum. The queiscent power dissipation is:

$$P_Q = V_S\ (D\ (I_H) + (1\text{-}D)\ I_L),$$

where: I_H = Quiescent current with input high (5mA max)
I_L = Quiescent current with input low (0.5mA max)
D = Duty cycle

Transition power dissipation arises because the ouput stage N- and P- channel MOS transistors are ON simultaneously for a very short period when the output changes. The transition package power dissipation is approximately:

$$P_T = f\ V_S\ (3.3 \times 10^{-9}\ A \bullet Sec)$$

An example shows the relative magnitude for each item.

Example 1:

C = 2500pF
V_S =15V
D = 50%
f = 200kHz
P_D = Package power dissipation = $P_C + P_T + P_Q$
= 113mW + 10mW + 41mW
= 164mW

Maximum operating temperature = $T_J - \theta_{JA}\ (P_D)$
= 125°C

where: T_J = Maximum allowable junction temperature (+150°C)
θ_{JA} = Junction-to-ambient thermal resistance (150 °C/W, CerDIP)

Note: Ambient operating temperature should not exceed +85°C for IJA devices or + 125°C for MJA devices.

Table 1. Maximum Operating Frequencies

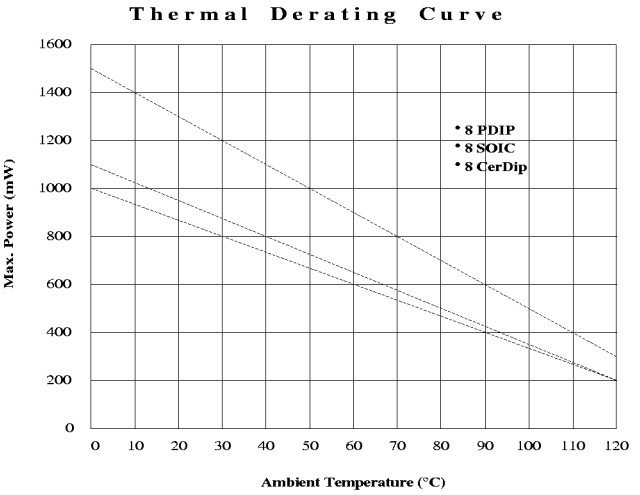
V_S	f_{Max}
18V	500kHz
15V	700kHz
10V	1.3MHz
5V	>2MHz

CONDITIONS: 1. CERDIP package (θ_{JA} = 150°C/W)
2. T_A = +25C
3. C_L = 2500pF

POWER-ON OSCILLATION

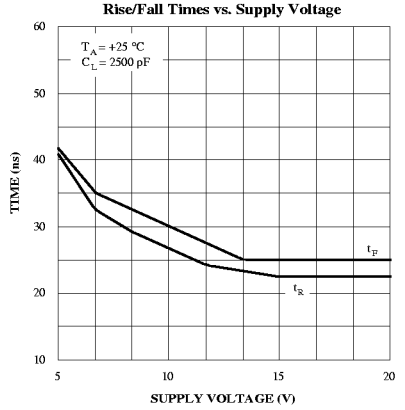
It is extremely important that all MOSFET DRIVE applications be evaluated for the possibility of having HIGH-POWER OSCILLATIONS occurring during the POWER-ON cycle.

POWER-ON OSCILLATIONS are due to trace size and layout as well as component placement. A "quick fix" for more applications which exhibit POWER-ON OSCILLATION problems is to place approximately 10kΩ in series with the input of the MOSFET drive.

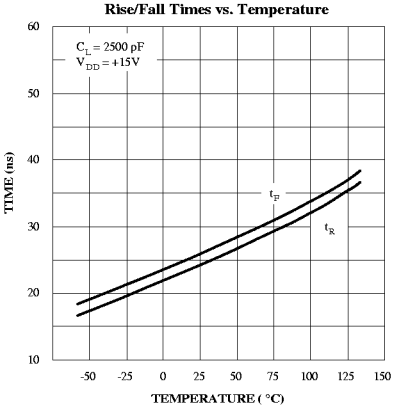


TYPICAL CHARACTERISTICS CURVES

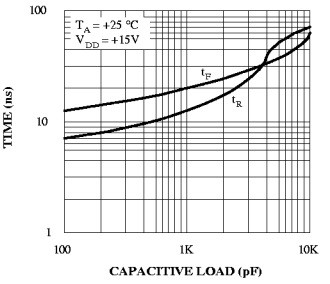
Rise/Fall Times vs. Supply Voltage



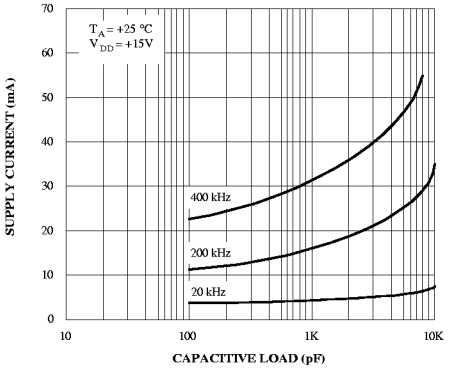
Rise/Fall Times vs. Temperature



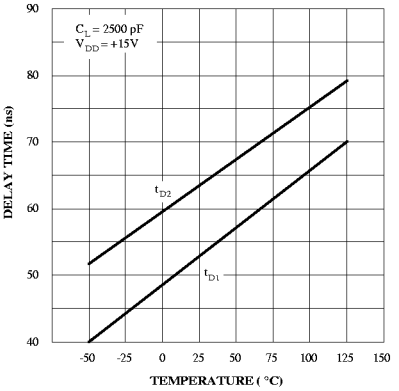
Rise/Fall Times vs. Capacitive Load



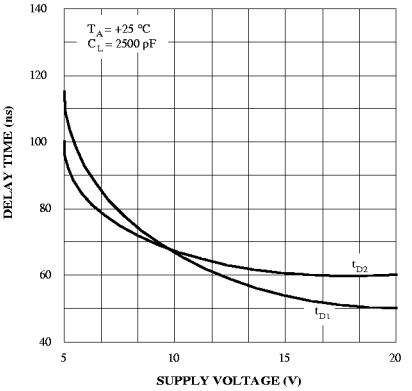
Supply Current vs. Capacitive Load



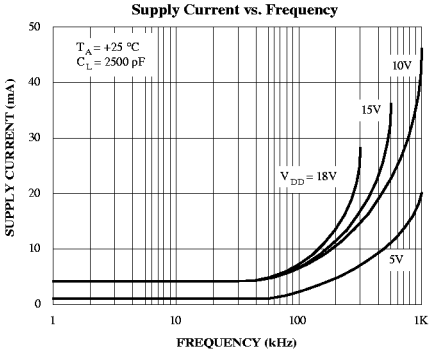
Delay Times vs. Temperature



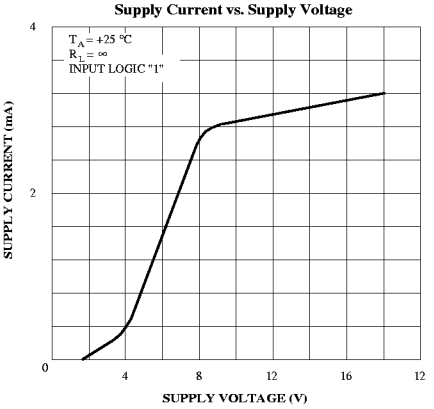
Delay Times vs. Supply Voltage



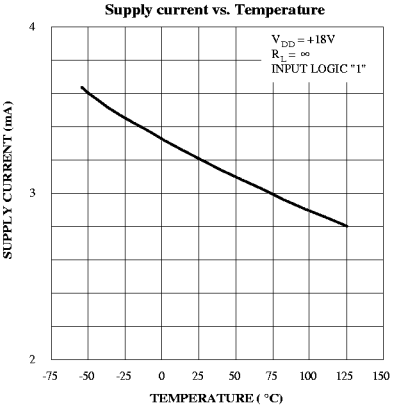
Supply Current vs. Frequency



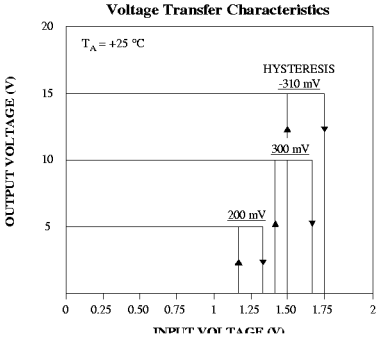
Supply Current vs. Supply Voltage



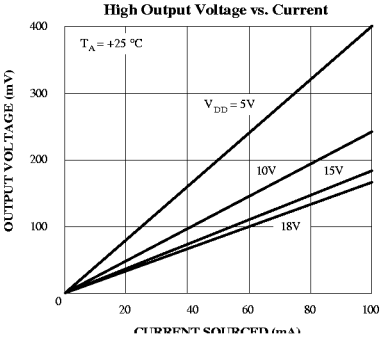
Supply current vs. Temperature



Voltage Transfer Characteristics



High Output Voltage vs. Current



Low Output Voltage vs. Current