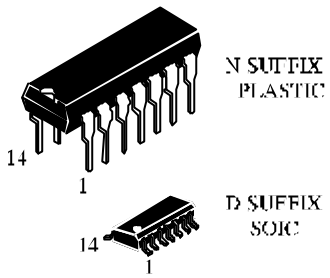
IN74HCU04

Hex Unbuffered Inverter
High-Performance Silicon-Gate CMOS

The IN74HCU04A is identical in pinout to the LS/ALS04. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

This device consists of six single-stage inverters. These inverters are well suited for use as oscillators, pulse shapers, and in many other applications requiring a high-input impedance amplifier. For digital applications, the HC04 is recommended.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V; 2.5 to 6 V in Oscillator Configurations.
- Low Input Current: 1.0 µA
- High Noise Immunity Characteristic of CMOS Devices

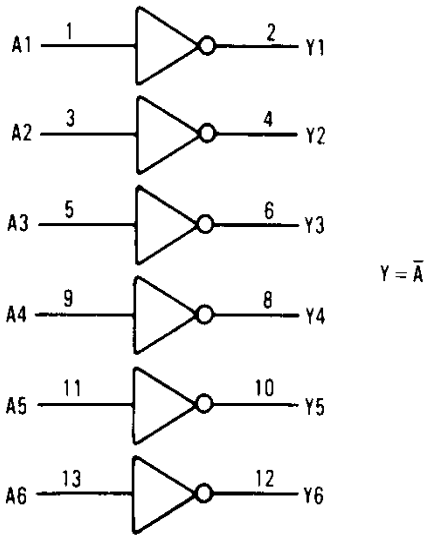


ORDERING INFORMATION

IN74HCU04N	Plastic
IN74HCU04D	SOIC
IZ74HCU04	Chip

T_A = -55° to 125° C for all packages

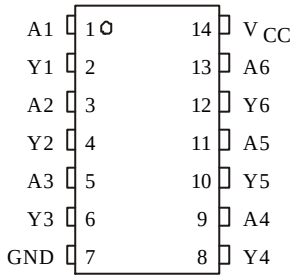
LOGIC DIAGRAM



$Y = \bar{A}$

PIN 14 =V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs	Output
A	Y
L	H
H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP ** SOIC Package **	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
** Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =2.0 Â V_{CC} =4.5 Â V_{CC} =6.0 Â	-	1000 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V * $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	1.7 3.6 4.8	1.7 3.6 4.8	1.7 3.6 4.8	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}= V_{CC}-0.1 V * $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	0.3 0.8 1.1	0.3 0.8 1.1	0.3 0.8 1.1	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	1.8 4.0 5.5	1.8 4.0 5.5	1.8 4.0 5.5	V
		V_{IN}=V_{IL} $\|I_{OUT}\| \le 4.0$ mA $\|I_{OUT}\| \le 5.2$ mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=V_{IH} $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	0.2 0.5 0.5	0.2 0.5 0.5	0.2 0.5 0.5	V
		V_{IN}=V_{IH} $\|I_{OUT}\| \le 4.0$ mA $\|I_{OUT}\| \le 5.2$ mA	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND I_{OUT}=0µA	6.0	2.0	20	40	µA

* For V_{CC} = 2.0 V, V_{OUT} = 0.2 V or V_{CC} – 0.2 V.

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	70 15 13	85 18 16	100 22 19	ns
C_{IN}	Maximum Input Capacitance	-	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$ For load considerations, see Chepter 4.	T_A=25?Ñ, V_{CC}=5.0 V 15				pF

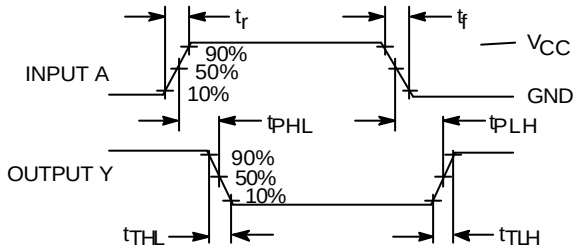
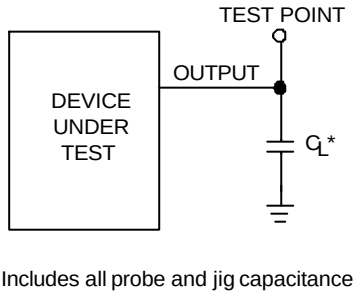


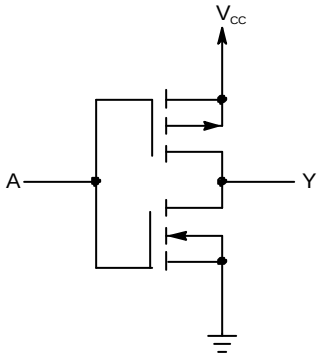
Figure 1. Switching Waveforms.



* Includes all probe and jig capacitance

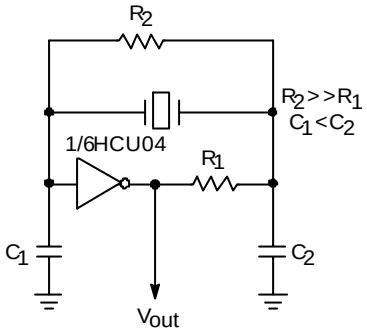
Figure 2. Test Circuit

LOGIC DETAIL
(1/6 of Device Show)

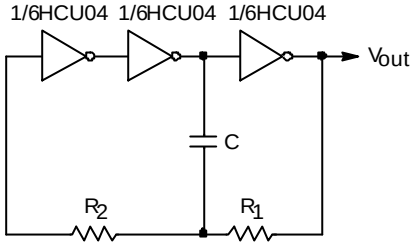


TYPICAL APPLICATIONS

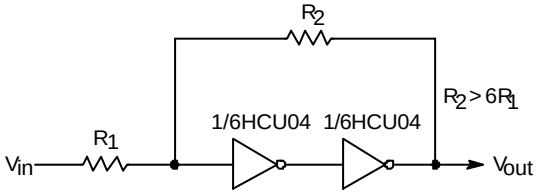
Crystal Oscillator



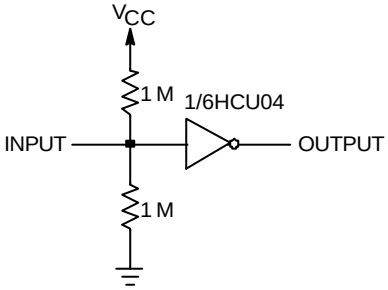
Stable RC Oscillator



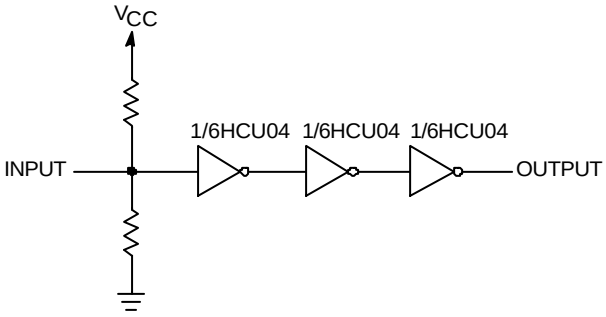
Schmitt Trigger



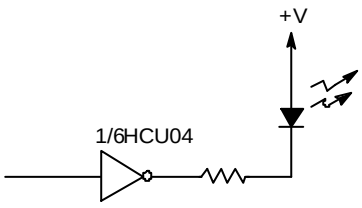
High Input Single-Stage Amplifier with a 2 to 6 V Supply Range



Multi-Stage Amplifier

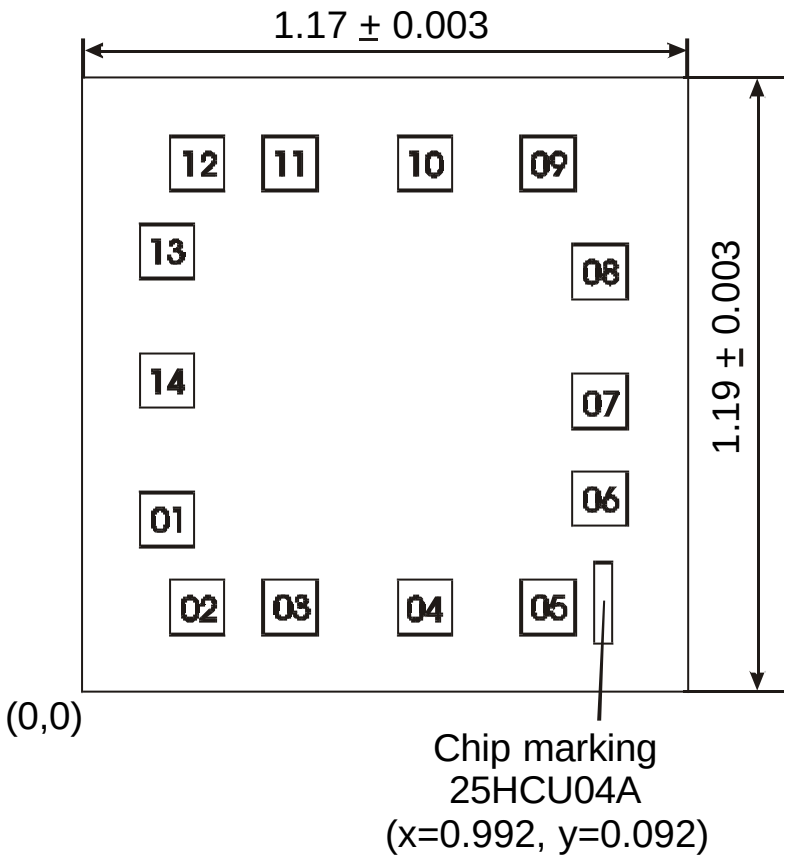


LED Driver



For reduced power suplly current, use high-efficiency LEDs such as the Hewlett-Packard HLMP series or equivalent

CHIP PAD DIAGRAM IZ74HCU04



Thickness of chip 0.46 ± 0,02 mm

PAD LOCATION

Pad No	Symbol	X	Y	Pad size* , mm
01	A1	0.110	0.280	0.105x0.105
02	Y1	0.170	0.110	0.105x0.105
03	A2	0.350	0.110	0.105x0.105
04	Y2	0.610	0.110	0.105x0.105
05	A3	0.850	0.110	0.105x0.105
06	Y3	0.950	0.320	0.105x0.105
07	GND	0.950	0.510	0.105x0.105
08	Y4	0.950	0.760	0.105x0.105
09	A4	0.850	0.970	0.105x0.105
10	Y5	0.610	0.970	0.105x0.105
11	A5	0.350	0.970	0.105x0.105
12	Y6	0.170	0.970	0.105x0.105
13	A6	0.110	0.800	0.105x0.105
14	V_{CC}	0.110	0.550	0.105x0.105

* Pad size is given as per metallization layer