

MOS INTEGRATED CIRCUIT

μ PD44325084, 44325094, 44325184, 44325364

36M-BIT QDR™II SRAM

4-WORD BURST OPERATION

Description

The μ PD44325084 is a 4,194,304-word by 8-bit, the μ PD44325094 is a 4,194,304-word by 9-bit, the μ PD44325184 is a 2,097,152-word by 18-bit and the μ PD44325364 is a 1,048,576-word by 36-bit synchronous quad data rate static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell.

The μ PD44325084, μ PD44325094, μ PD44325184 and μ PD44325364 integrate unique synchronous peripheral circuitry and a burst counter. All input registers controlled by an input clock pair (K and /K) are latched on the positive edge of K and /K.

These products are suitable for application which require synchronous operation, high speed, low voltage, high density and wide bit configuration.

These products are packaged in 165-pin PLASTIC FBGA.

Features

- 1.8 ± 0.1 V power supply and HSTL I/O
- DLL circuitry for wide output data valid window and future frequency scaling
- Separate independent read and write data ports with concurrent transactions
- 100% bus utilization DDR READ and WRITE operation
- Four-tick burst for reduced address frequency
- Two input clocks (K and /K) for precise DDR timing at clock rising edges only
- Two output clocks (C and /C) for precise flight time
and clock skew matching-clock and data delivered together to receiving device
- Internally self-timed write control
- Clock-stop capability with μ s restart
- User programmable impedance output
- ★ Fast clock cycle time : 3.3 ns (300 MHz) , 4.0 ns (250 MHz) , 5.0 ns (200 MHz)
- Simple control logic for easy depth expansion
- JTAG boundary scan

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★ Ordering Information

| Part number | Cycle Time ns | Clock Frequency MHz | Organization (word x bit) | Core Supply Voltage V | I/O Interface | Package |
|---------------------------------------|---------------|---------------------|---------------------------|-----------------------|---------------|--------------------------------|
| μPD44325084F5-E33-EQ2 ^{Note} | 3.3 | 300 | 4 M x 8-bit | 1.8 ± 0.1 | HSTL | 165-pin PLASTIC FBGA (13 x 15) |
| μPD44325084F5-E40-EQ2 | 4.0 | 250 | | | | |
| μPD44325084F5-E50-EQ2 | 5.0 | 200 | | | | |
| μPD44325094F5-E33-EQ2 ^{Note} | 3.3 | 300 | 4 M x 9-bit | | | |
| μPD44325094F5-E40-EQ2 | 4.0 | 250 | | | | |
| μPD44325094F5-E50-EQ2 | 5.0 | 200 | | | | |
| μPD44325184F5-E33-EQ2 ^{Note} | 3.3 | 300 | 2 M x 18-bit | | | |
| μPD44325184F5-E40-EQ2 | 4.0 | 250 | | | | |
| μPD44325184F5-E50-EQ2 | 5.0 | 200 | | | | |
| μPD44325364F5-E33-EQ2 ^{Note} | 3.3 | 300 | 1M x 36-bit | | | |
| μPD44325364F5-E40-EQ2 | 4.0 | 250 | | | | |
| μPD44325364F5-E50-EQ2 | 5.0 | 200 | | | | |

Note Under development

Pin Configurations

/xxx indicates active low signal.

165-pin PLASTIC FBGA (13 x 15)

(Top View)

[μPD44325084F5-EQ2]

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|------|------------------|------------------|------------------|-----------------|-----------------|-----------------|------------------|------------------|------------------|-----|
| A | /CQ | V _{SS} | A | /W | /NW1 | /K | NC | /R | A | A | CQ |
| B | NC | NC | NC | A | NC | K | /NW0 | A | NC | NC | Q3 |
| C | NC | NC | NC | V _{SS} | A | NC | A | V _{SS} | NC | NC | D3 |
| D | NC | D4 | NC | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | NC | NC | NC |
| E | NC | NC | Q4 | V _{DDQ} | V _{SS} | V _{SS} | V _{SS} | V _{DDQ} | NC | D2 | Q2 |
| F | NC | NC | NC | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | NC | NC | NC |
| G | NC | D5 | Q5 | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | NC | NC | NC |
| H | /DLL | V _{REF} | V _{DDQ} | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | V _{DDQ} | V _{REF} | ZQ |
| J | NC | NC | NC | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | NC | Q1 | D1 |
| K | NC | NC | NC | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | NC | NC | NC |
| L | NC | Q6 | D6 | V _{DDQ} | V _{SS} | V _{SS} | V _{SS} | V _{DDQ} | NC | NC | Q0 |
| M | NC | NC | NC | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | NC | NC | D0 |
| N | NC | D7 | NC | V _{SS} | A | A | A | V _{SS} | NC | NC | NC |
| P | NC | NC | Q7 | A | A | C | A | A | NC | NC | NC |
| R | TDO | TCK | A | A | A | /C | A | A | A | TMS | TDI |

- | | | | |
|------------|-----------------------------|------------------|------------------------------|
| A | : Address inputs | TMS | : IEEE 1149.1 Test input |
| D0 to D7 | : Data inputs | TDI | : IEEE 1149.1 Test input |
| Q0 to Q7 | : Data outputs | TCK | : IEEE 1149.1 Clock input |
| /R | : Read input | TDO | : IEEE 1149.1 Test output |
| /W | : Write input | V _{REF} | : HSTL input reference input |
| /NW0, /NW1 | : Nibble Write data select | V _{DD} | : Power Supply |
| K, /K | : Input clock | V _{DDQ} | : Power Supply |
| C, /C | : Output clock | V _{SS} | : Ground |
| CQ, /CQ | : Echo clock | NC | : No connection |
| ZQ | : Output impedance matching | | |
| /DLL | : DLL disable | | |

Remarks 1. Refer to **Package Drawing** for the index mark.

★ 2. 2A and 7A are expansion addresses: 2A for 72Mb and 7A for 144Mb.

165-pin PLASTIC FBGA (13 x 15)

(Top View)

[μPD44325094F5-EQ2]

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|------|------------------|------------------|------------------|-----------------|-----------------|-----------------|------------------|------------------|------------------|-----|
| A | /CQ | V _{SS} | A | /W | NC | /K | NC | /R | A | A | CQ |
| B | NC | NC | NC | A | NC | K | /BW0 | A | NC | NC | Q4 |
| C | NC | NC | NC | V _{SS} | A | NC | A | V _{SS} | NC | NC | D4 |
| D | NC | D5 | NC | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | NC | NC | NC |
| E | NC | NC | Q5 | V _{DDQ} | V _{SS} | V _{SS} | V _{SS} | V _{DDQ} | NC | D3 | Q3 |
| F | NC | NC | NC | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | NC | NC | NC |
| G | NC | D6 | Q6 | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | NC | NC | NC |
| H | /DLL | V _{REF} | V _{DDQ} | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | V _{DDQ} | V _{REF} | ZQ |
| J | NC | NC | NC | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | NC | Q2 | D2 |
| K | NC | NC | NC | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | NC | NC | NC |
| L | NC | Q7 | D7 | V _{DDQ} | V _{SS} | V _{SS} | V _{SS} | V _{DDQ} | NC | NC | Q1 |
| M | NC | NC | NC | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | NC | NC | D1 |
| N | NC | D8 | NC | V _{SS} | A | A | A | V _{SS} | NC | NC | NC |
| P | NC | NC | Q8 | A | A | C | A | A | NC | D0 | Q0 |
| R | TDO | TCK | A | A | A | /C | A | A | A | TMS | TDI |

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|----------|-----------------------------|------------------|------------------------------|
| A | : Address inputs | TMS | : IEEE 1149.1 Test input |
| D0 to D8 | : Data inputs | TDI | : IEEE 1149.1 Test input |
| Q0 to Q8 | : Data outputs | TCK | : IEEE 1149.1 Clock input |
| /R | : Read input | TDO | : IEEE 1149.1 Test output |
| /W | : Write input | V _{REF} | : HSTL input reference input |
| /BW0 | : Byte Write data select | V _{DD} | : Power Supply |
| K, /K | : Input clock | V _{DDQ} | : Power Supply |
| C, /C | : Output clock | V _{SS} | : Ground |
| CQ, /CQ | : Echo clock | NC | : No connection |
| ZQ | : Output impedance matching | | |
| /DLL | : DLL disable | | |

Remarks 1. Refer to **Package Drawing** for the index mark.

★ 2. 2A and 7A are expansion addresses: 2A for 72Mb and 7A for 144Mb.

165-pin PLASTIC FBGA (13 x 15)

(Top View)

[μPD44325184F5-EQ2]

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|------|------------------|------------------|------------------|-----------------|-----------------|-----------------|------------------|------------------|------------------|-----|
| A | /CQ | V _{SS} | A | /W | /BW1 | /K | NC | /R | A | V _{SS} | CQ |
| B | NC | Q9 | D9 | A | NC | K | /BW0 | A | NC | NC | Q8 |
| C | NC | NC | D10 | V _{SS} | A | NC | A | V _{SS} | NC | Q7 | D8 |
| D | NC | D11 | Q10 | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | NC | NC | D7 |
| E | NC | NC | Q11 | V _{DDQ} | V _{SS} | V _{SS} | V _{SS} | V _{DDQ} | NC | D6 | Q6 |
| F | NC | Q12 | D12 | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | NC | NC | Q5 |
| G | NC | D13 | Q13 | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | NC | NC | D5 |
| H | /DLL | V _{REF} | V _{DDQ} | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | V _{DDQ} | V _{REF} | ZQ |
| J | NC | NC | D14 | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | NC | Q4 | D4 |
| K | NC | NC | Q14 | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | NC | D3 | Q3 |
| L | NC | Q15 | D15 | V _{DDQ} | V _{SS} | V _{SS} | V _{SS} | V _{DDQ} | NC | NC | Q2 |
| M | NC | NC | D16 | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | NC | Q1 | D2 |
| N | NC | D17 | Q16 | V _{SS} | A | A | A | V _{SS} | NC | NC | D1 |
| P | NC | NC | Q17 | A | A | C | A | A | NC | D0 | Q0 |
| R | TDO | TCK | A | A | A | /C | A | A | A | TMS | TDI |

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|------------|-----------------------------|------------------|------------------------------|
| A | : Address inputs | TMS | : IEEE 1149.1 Test input |
| D0 to D17 | : Data inputs | TDI | : IEEE 1149.1 Test input |
| Q0 to Q17 | : Data outputs | TCK | : IEEE 1149.1 Clock input |
| /R | : Read input | TDO | : IEEE 1149.1 Test output |
| /W | : Write input | V _{REF} | : HSTL input reference input |
| /BW0, /BW1 | : Byte Write data select | V _{DD} | : Power Supply |
| K, /K | : Input clock | V _{DDQ} | : Power Supply |
| C, /C | : Output clock | V _{SS} | : Ground |
| CQ, /CQ | : Echo clock | NC | : No connection |
| ZQ | : Output impedance matching | | |
| /DLL | : DLL disable | | |

Remarks 1. Refer to **Package Drawing** for the index mark.

★ 2. 2A and 10A are expansion addresses: 10A for 72Mb and 2A for 144Mb.

165-pin PLASTIC FBGA (13 x 15)

(Top View)

[μPD44325364F5-EQ2]

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|------|------------------|------------------|------------------|-----------------|-----------------|-----------------|------------------|------------------|------------------|-----|
| A | /CQ | V _{SS} | NC | /W | /BW2 | /K | /BW1 | /R | A | V _{SS} | CQ |
| B | Q27 | Q18 | D18 | A | /BW3 | K | /BW0 | A | D17 | Q17 | Q8 |
| C | D27 | Q28 | D19 | V _{SS} | A | NC | A | V _{SS} | D16 | Q7 | D8 |
| D | D28 | D20 | Q19 | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | Q16 | D15 | D7 |
| E | Q29 | D29 | Q20 | V _{DDQ} | V _{SS} | V _{SS} | V _{SS} | V _{DDQ} | Q15 | D6 | Q6 |
| F | Q30 | Q21 | D21 | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | D14 | Q14 | Q5 |
| G | D30 | D22 | Q22 | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | Q13 | D13 | D5 |
| H | /DLL | V _{REF} | V _{DDQ} | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | V _{DDQ} | V _{REF} | ZQ |
| J | D31 | Q31 | D23 | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | D12 | Q4 | D4 |
| K | Q32 | D32 | Q23 | V _{DDQ} | V _{DD} | V _{SS} | V _{DD} | V _{DDQ} | Q12 | D3 | Q3 |
| L | Q33 | Q24 | D24 | V _{DDQ} | V _{SS} | V _{SS} | V _{SS} | V _{DDQ} | D11 | Q11 | Q2 |
| M | D33 | Q34 | D25 | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | D10 | Q1 | D2 |
| N | D34 | D26 | Q25 | V _{SS} | A | A | A | V _{SS} | Q10 | D9 | D1 |
| P | Q35 | D35 | Q26 | A | A | C | A | A | Q9 | D0 | Q0 |
| R | TDO | TCK | A | A | A | /C | A | A | A | TMS | TDI |

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|--------------|-----------------------------|------------------|------------------------------|
| A | : Address inputs | TMS | : IEEE 1149.1 Test input |
| D0 to D35 | : Data inputs | TDI | : IEEE 1149.1 Test input |
| Q0 to Q35 | : Data outputs | TCK | : IEEE 1149.1 Clock input |
| /R | : Read input | TDO | : IEEE 1149.1 Test output |
| /W | : Write input | V _{REF} | : HSTL input reference input |
| /BW0 to /BW3 | : Byte Write data select | V _{DD} | : Power Supply |
| K, /K | : Input clock | V _{DDQ} | : Power Supply |
| C, /C | : Output clock | V _{SS} | : Ground |
| CQ, /CQ | : Echo clock | NC | : No connection |
| ZQ | : Output impedance matching | | |
| /DLL | : DLL disable | | |

Remarks 1. Refer to **Package Drawing** for the index mark.

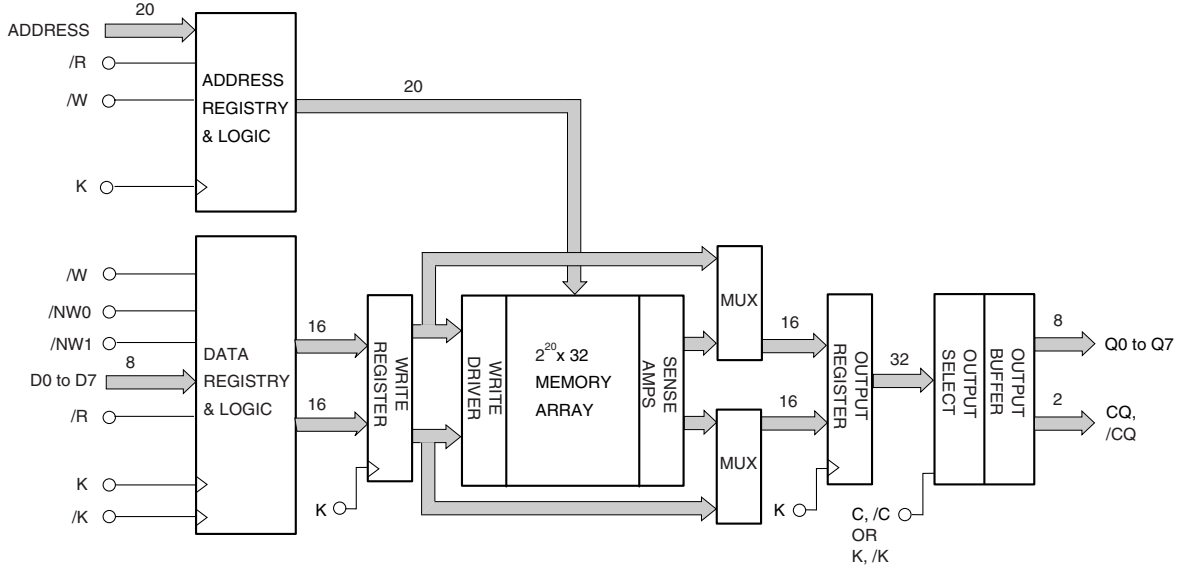
★ 2. 3A and 10A are expansion addresses: 3A for 72Mb and 10A for 144Mb.

Pin Identification

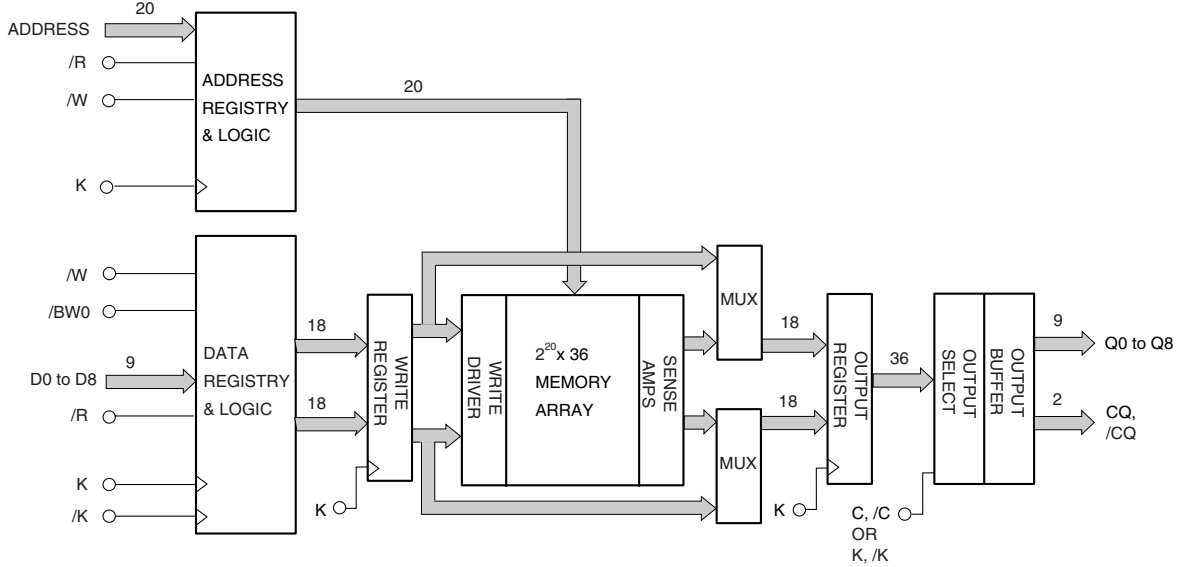
| Symbol | Description |
|--------------|--|
| A | Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. All transactions operate on a burst of four words (two clock periods of bus activity). These inputs are ignored when device is deselected. |
| D0 to Dxx | Synchronous Data Inputs: Input data must meet setup and hold times around the rising edges of K and /K during WRITE operations. See Pin Configurations for ball site location of individual signals. x8 device uses D0 to D7. x9 device uses D0 to D8. x18 device uses D0 to D17. x36 device uses D0 to D35. |
| Q0 to Qxx | Synchronous Data Outputs: Output data is synchronized to the respective C and /C or to K and /K rising edges if C and /C are tied HIGH. This bus operates in response to /R commands. See Pin Configurations for ball site location of individual signals. x8 device uses Q0 to Q7. x9 device uses Q0 to Q8. x18 device uses Q0 to Q17. x36 device uses Q0 to Q35. |
| /R | Synchronous Read: When LOW this input causes the address inputs to be registered and a READ cycle to be initiated. This input must meet setup and hold times around the rising edge of K and is ignored on the subsequent rising edge of K. |
| /W | Synchronous Write: When LOW this input causes the address inputs to be registered and a WRITE cycle to be initiated. This input must meet setup and hold times around the rising edge of K and is ignored on the subsequent rising edge of K. |
| /BWx /NWx | Synchronous Byte Writes (Nibble Writes on x8): When LOW these inputs cause their respective byte or nibble to be registered and written during WRITE cycles. These signals must meet setup and hold times around the rising edges of K and /K for each of the two rising edges comprising the WRITE cycle. See Pin Configurations for signal to data relationships. |
| K, /K | Input Clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of /K. /K is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges. |
| C, /C | Output Clock: This clock pair provides a user controlled means of tuning device output data. The rising edge of /C is used as the output timing reference for first and third output data. The rising edge of C is used as the output reference for second and fourth output data. Ideally, /C is 180 degrees out of phase with C. C and /C may be tied HIGH to force the use of K and /K as the output reference clocks instead of having to provide C and /C clocks. If tied HIGH, C and /C must remain HIGH and not be toggled during device operation. |
| CQ, /CQ | Synchronous Echo Clock Outputs. The rising edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when Q tristates. |
| ZQ | Output Impedance Matching Input: This input is used to tune the device outputs to the system data bus impedance. DQ and CQ output impedance are set to $0.2 \times RQ$, where RQ is a resistor from this bump to ground. This pin cannot be connected directly to GND or left unconnected. |
| /DLL | DLL Disable: When LOW, this input causes the DLL to be bypassed for stable low frequency operation. |
| TMS TDI | IEEE 1149.1 Test Inputs: 1.8V I/O levels. These balls may be left Not Connected if the JTAG function is not used in the circuit. |
| TCK | IEEE 1149.1 Clock Input: 1.8V I/O levels. This pin must be tied to V _{SS} if the JTAG function is not used in the circuit. |
| TDO | IEEE 1149.1 Test Output: 1.8V I/O level. |
| VREF | HSTL Input Reference Voltage: Nominally V _{DDQ} /2. Provides a reference voltage for the input buffers. |
| VDD | Power Supply: 1.8V nominal. See DC Characteristics and Operating Conditions for range. |
| VDDQ | Power Supply: Isolated Output Buffer Supply. Nominally 1.5V. 1.8V is also permissible. See DC Characteristics and Operating Conditions for range. |
| VSS | Power Supply: Ground |
| NC | No Connect: These signals are internally connected and appear in the JTAG scan chain as the logic level applied to the ball sites. These signals may be connected to ground to improve package heat dissipation. |

Block Diagram

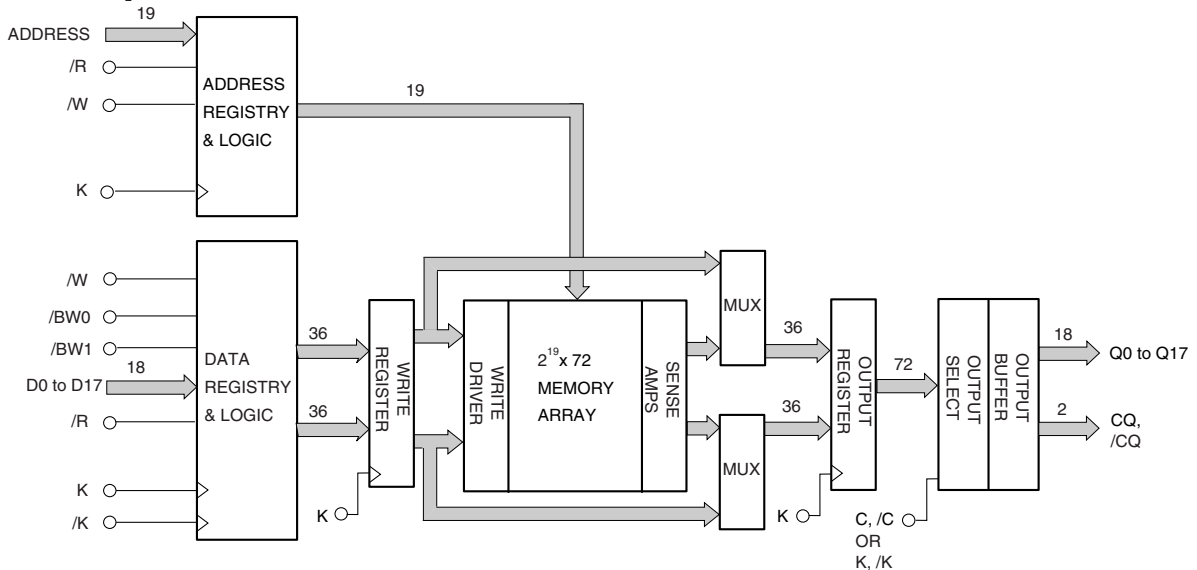
[μ PD44325084]



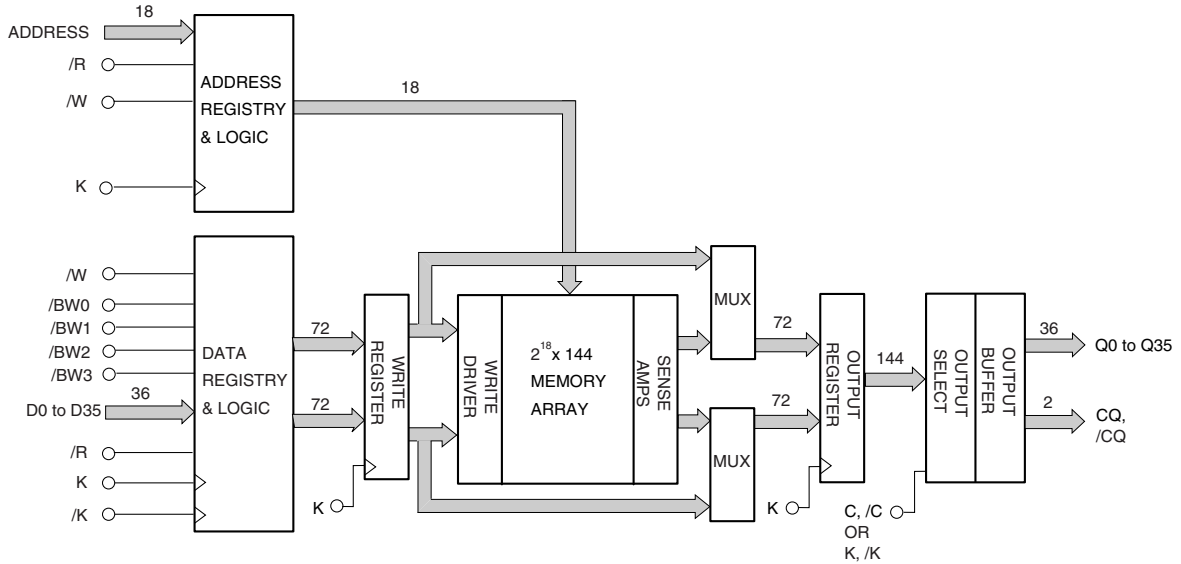
[μ PD44325094]



[μ PD44325184]



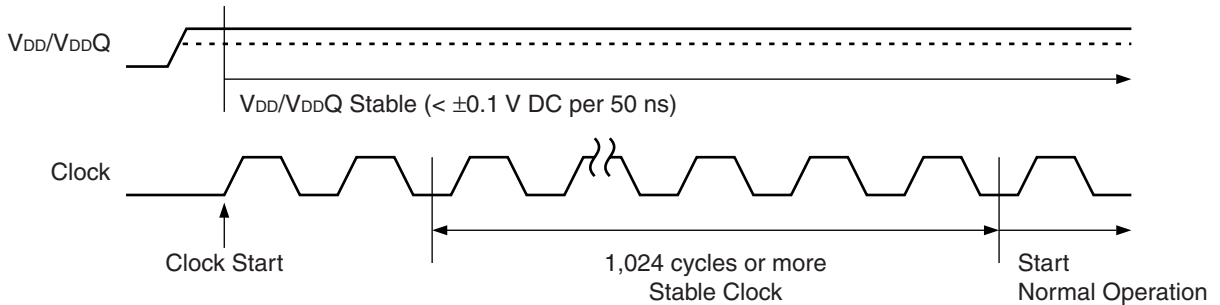
[μ PD44325364]



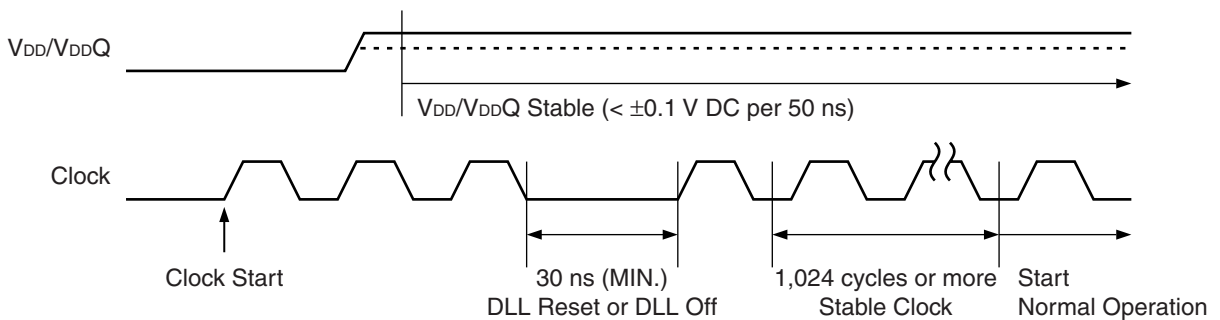
★ Power-on Sequence

The following two timing charts show the recommended power-on sequence, i.e., when starting the clock after V_{DD}/V_{DDQ} stable and when starting the clock before V_{DD}/V_{DDQ} stable.

1. Clock starts after V_{DD}/V_{DDQ} stable



2. Clock starts before V_{DD}/V_{DDQ} stable



Truth Table

| Operation | CLK | /R | /W | D or Q | | | | |
|---|---------|----|----|-----------------|----------------------|----------------------|----------------------|----------------------|
| WRITE cycle Load address, input write data on two consecutive K and /K rising edge | L → H | H | L | Data in | | | | |
| | | | | Input data | D _A (A+0) | D _A (A+1) | D _A (A+2) | D _A (A+3) |
| | | | | Input clock | K(t+1) ↑ | /K(t+1) ↑ | K(t+2) ↑ | /K(t+2) ↑ |
| READ cycle Load address, read data on two consecutive C and /C rising edge | L → H | L | X | Data out | | | | |
| | | | | Output data | Q _A (A+0) | Q _A (A+1) | Q _A (A+2) | Q _A (A+3) |
| | | | | Output clock | /C(t+1) ↑ | C(t+2) ↑ | /C(t+2) ↑ | C(t+3) ↑ |
| NOP (No operation) | L → H | H | H | D=X or Q=High-Z | | | | |
| STANDBY(Clock stopped) | Stopped | X | X | Previous state | | | | |

- Remarks**
1. H : High level, L : Low level, x : don't care, ↑ : rising edge.
 2. Data inputs are registered at K and /K rising edges. Data outputs are delivered at C and /C rising edges except if C and /C are HIGH then data outputs are delivered at K and /K rising edges.
 3. /R and /W must meet setup/hold times around the rising edge (LOW to HIGH) of K and are registered at the rising edge of K.
 4. This device contains circuitry that will ensure the outputs will be in high impedance during power-up.
 5. Refer to state diagram and timing diagrams for clarification.
 6. It is recommended that K = /(K) = C = /(C) when clock is stopped. This is not essential but permits most rapid restart by overcoming transmission line charging symmetrically.
 7. If /R was LOW to initiate the previous cycle, this signal becomes a don't care for this operation however it is strongly recommended that this signal is brought HIGH as shown in the truth table.
 8. /W during write cycle and /R during read cycle were HIGH on previous K clock rising edge. Initiating consecutive READ or WRITE operations on consecutive K clock rising edges is not permitted. The device will ignore the second request.

Byte Write Operation

[μPD44325084]

| Operation | K | /K | /NW0 | /NW1 |
|----------------|-------|-------|------|------|
| Write D0 to D7 | L → H | – | 0 | 0 |
| | – | L → H | 0 | 0 |
| Write D0 to D3 | L → H | – | 0 | 1 |
| | – | L → H | 0 | 1 |
| Write D4 to D7 | L → H | – | 1 | 0 |
| | – | L → H | 1 | 0 |
| Write nothing | L → H | – | 1 | 1 |
| | – | L → H | 1 | 1 |

- Remarks** 1. H : High level, L : Low level, → : rising edge.
 2. Assumes a WRITE cycle was initiated. /NW0 and /NW1 can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

[μPD44325094]

| Operation | K | /K | /BW0 |
|----------------|-------|-------|------|
| Write D0 to D8 | L → H | – | 0 |
| | – | L → H | 0 |
| Write nothing | L → H | – | 1 |
| | – | L → H | 1 |

- Remarks** 1. H : High level, L : Low level, → : rising edge.
 2. Assumes a WRITE cycle was initiated. /BW0 can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

[μPD44325184]

| Operation | K | /K | /BW0 | /BW1 |
|-----------------|-------|-------|------|------|
| Write D0 to D17 | L → H | – | 0 | 0 |
| | – | L → H | 0 | 0 |
| Write D0 to D8 | L → H | – | 0 | 1 |
| | – | L → H | 0 | 1 |
| Write D9 to D17 | L → H | – | 1 | 0 |
| | – | L → H | 1 | 0 |
| Write nothing | L → H | – | 1 | 1 |
| | – | L → H | 1 | 1 |

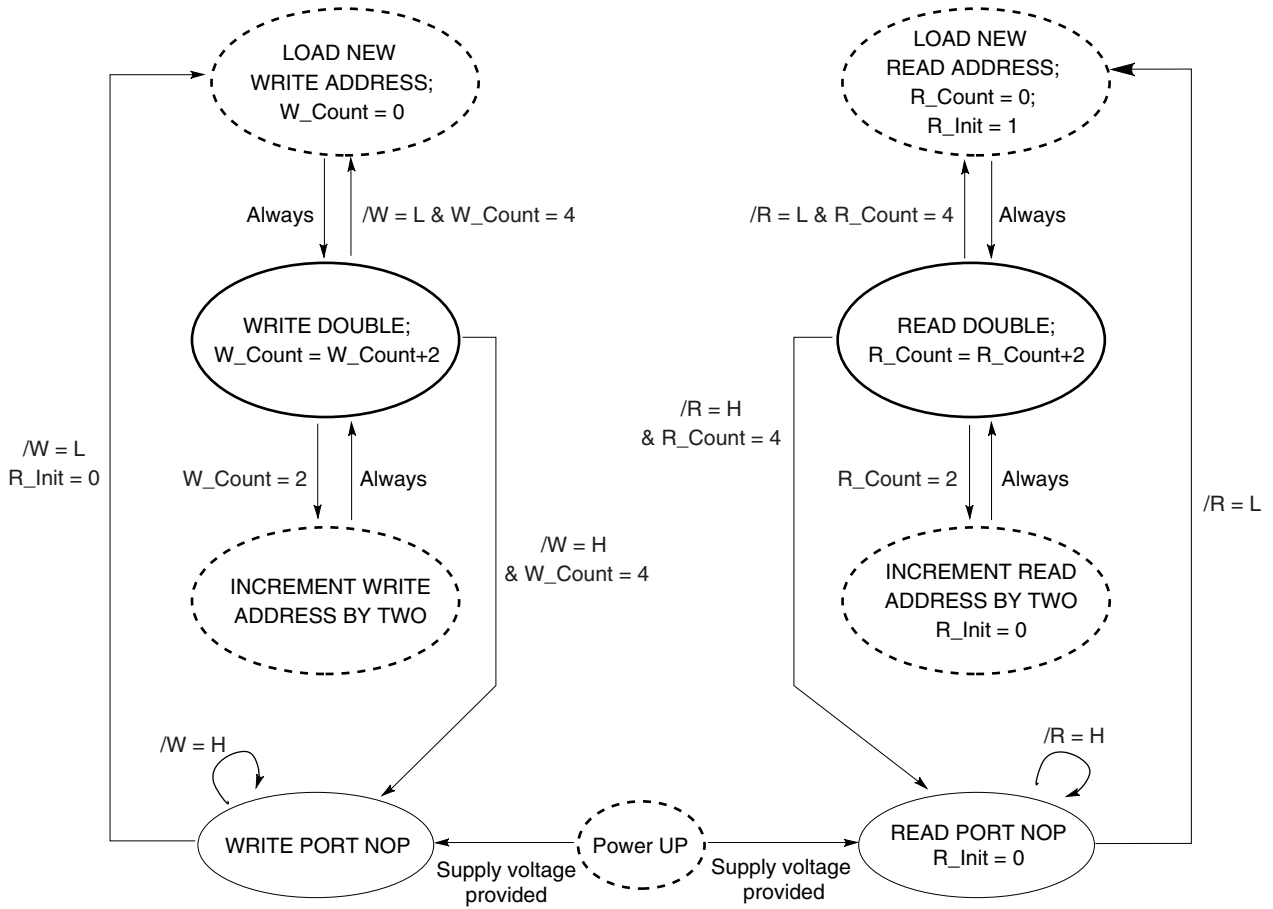
- Remarks** 1. H : High level, L : Low level, → : rising edge.
 2. Assumes a WRITE cycle was initiated. /BW0 and /BW1 can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

[μPD44325364]

| Operation | K | /K | /BW0 | /BW1 | /BW2 | /BW3 |
|------------------|-------|-------|------|------|------|------|
| Write D0 to D35 | L → H | – | 0 | 0 | 0 | 0 |
| | – | L → H | 0 | 0 | 0 | 0 |
| Write D0 to D8 | L → H | – | 0 | 1 | 1 | 1 |
| | – | L → H | 0 | 1 | 1 | 1 |
| Write D9 to D17 | L → H | – | 1 | 0 | 1 | 1 |
| | – | L → H | 1 | 0 | 1 | 1 |
| Write D18 to D26 | L → H | – | 1 | 1 | 0 | 1 |
| | – | L → H | 1 | 1 | 0 | 1 |
| Write D27 to D35 | L → H | – | 1 | 1 | 1 | 0 |
| | – | L → H | 1 | 1 | 1 | 0 |
| Write nothing | L → H | – | 1 | 1 | 1 | 1 |
| | – | L → H | 1 | 1 | 1 | 1 |

- Remarks**
1. H : High level, L : Low level, → : rising edge.
 2. Assumes a WRITE cycle was initiated. /BW0 to /BW3 can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

Bus Cycle State Diagram



- Remarks**
1. The address is concatenated with two additional internal LSBs to facilitate burst operation. The address order is always fixed as: xxx...xxx+0, xxx...xxx+1, xxx...xxx+2, xxx...xxx+3. Bus cycle is terminated at the end of this sequence (burst count = 4).
 2. Read and write state machines can be active simultaneously. Read and write cannot be simultaneously initiated. Read takes precedence.
 3. State machine control timing is controlled by K.

Electrical Specifications

Absolute Maximum Ratings

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------|------------------|------------|------|------|-------------------------------------|------|
| Supply voltage | V _{DD} | | -0.5 | | +2.5 | V |
| Output supply voltage | V _{DDQ} | | -0.5 | | V _{DD} | V |
| Input voltage | V _{IN} | | -0.5 | | V _{DD} + 0.5 (2.5 V MAX.) | V |
| Input / Output voltage | V _{I/O} | | -0.5 | | V _{DDQ} + 0.5 (2.5 V MAX.) | V |
| Operating ambient temperature | T _A | | 0 | | 70 | °C |
| Storage temperature | T _{stg} | | -55 | | +125 | °C |

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70 °C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | Note |
|--------------------------|----------------------|------------|------------------------|------|------------------------|------|------|
| Supply voltage | V _{DD} | | 1.7 | | 1.9 | V | |
| Output supply voltage | V _{DDQ} | | 1.4 | | V _{DD} | V | 1 |
| High level input voltage | V _{IH} (DC) | | V _{REF} + 0.1 | | V _{DDQ} + 0.3 | V | 1, 2 |
| Low level input voltage | V _{IL} (DC) | | -0.3 | | V _{REF} - 0.1 | V | 1, 2 |
| Clock input voltage | V _{IN} | | -0.3 | | V _{DDQ} + 0.3 | V | 1, 2 |
| Reference voltage | V _{REF} | | 0.68 | | 0.95 | V | |

- Notes**
1. During normal operation, V_{DDQ} must not exceed V_{DD}.
 2. Power-up: V_{IH} ≤ V_{DDQ} + 0.3 V and V_{DD} ≤ 1.7 V and V_{DDQ} ≤ 1.4 V for t ≤ 200 ms

Recommended AC Operating Conditions (T_A = 0 to 70 °C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | Note |
|--------------------------|----------------------|------------|------------------------|------|------------------------|------|------|
| High level input voltage | V _{IH} (AC) | | V _{REF} + 0.2 | | - | V | 1 |
| Low level input voltage | V _{IL} (AC) | | - | | V _{REF} - 0.2 | V | 1 |

- Note**
1. Overshoot: V_{IH} (AC) ≤ V_{DD} + 0.7 V for t ≤ TKHKH/2
 Undershoot: V_{IL} (AC) ≥ -0.5 V for t ≤ TKHKH/2
 Control input signals may not have pulse widths less than TKHKL (MIN.) or operate at cycle rates less than TKHKH (MIN.).

DC Characteristics (T_A = 0 to 70°C, V_{DD} = 1.8 ± 0.1 V)

| Parameter | Symbol | Test condition | MIN. | TYP. | MAX. | | | Unit | Note |
|--|----------------------|---|----------------------------|------|----------------------------|---------------------|-----------------------|------|------|
| | | | | | x8, x9 | x18 | x36 | | |
| Input leakage current | I _{LI} | | -2 | - | +2 | | | μA | |
| I/O leakage current | I _{LO} | | -2 | - | +2 | | | μA | |
| ★ Operating supply current (Read Write cycle) | I _{DD} | V _{IN} ≤ V _{IL} or V _{IN} ≥ V _{IH} , I _{I/O} = 0 mA Cycle = MAX. | -E33 -E40 -E50 | | 800 700 600 | 1,100 950 800 | 1,250 1,050 900 | mA | |
| ★ Standby supply current (NOP) | I _{SB1} | V _{IN} ≤ V _{IL} or V _{IN} ≥ V _{IH} , I _{I/O} = 0 mA Cycle = MAX. | -E33 -E40 -E50 | | 450 400 350 | | | mA | |
| High level output voltage | V _{OH(Low)} | I _{OH} ≤ 0.1 mA | V _{DDQ} - 0.2 | - | V _{DDQ} | | | V | 3,4 |
| | V _{OH} | Note1 | V _{DDQ} /2 - 0.12 | - | V _{DDQ} /2 + 0.12 | | | V | 3,4 |
| Low level output voltage | V _{OL(Low)} | I _{OL} ≤ 0.1 mA | V _{SS} | - | 0.2 | | | V | 3,4 |
| | V _{OL} | Note2 | V _{DDQ} /2 - 0.12 | - | V _{DDQ} /2 + 0.12 | | | V | 3,4 |

- Notes**
1. Outputs are impedance-controlled. |I_{OH}| = (V_{DDQ}/2)/(R_Q/5) for values of 175 Ω ≤ R_Q ≤ 350 Ω.
 2. Outputs are impedance-controlled. I_{OL} = (V_{DDQ}/2)/(R_Q/5) for values of 175 Ω ≤ R_Q ≤ 350 Ω.
 3. AC load current is higher than the shown DC values.
 4. HSTL outputs meet JEDEC HSTL Class I and Class II standards.

Capacitance (T_A = 25 °C, f = 1MHz)

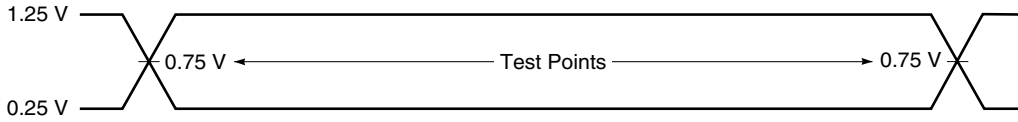
| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------------|------------------|------------------------|------|------|------|------|
| Input capacitance(Address, Control) | C _{IN} | V _{IN} = 0 V | | 4 | 5 | pF |
| Input / Output capacitance(D, Q) | C _{I/O} | V _{I/O} = 0 V | | 6 | 7 | pF |
| Clock Input capacitance | C _{clk} | V _{clk} = 0 V | | 5 | 6 | pF |

Remark These parameters are periodically sampled and not 100% tested.

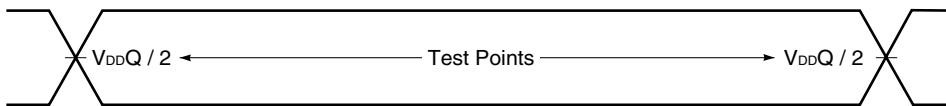
AC Characteristics ($T_A = 0$ to $70\text{ }^\circ\text{C}$, $V_{DD} = 1.8 \pm 0.1\text{ V}$)

AC Test Conditions

Input waveform (Rise / Fall time $\leq 0.3\text{ ns}$)

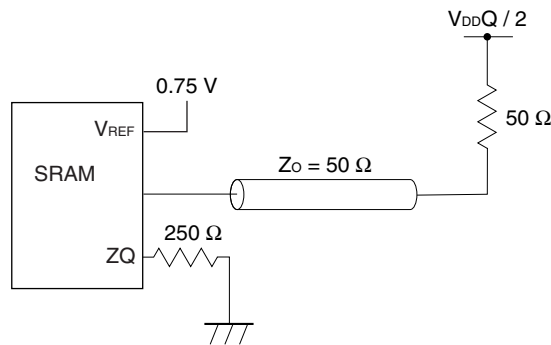


Output waveform



Output load condition

Figure 1. External load at test



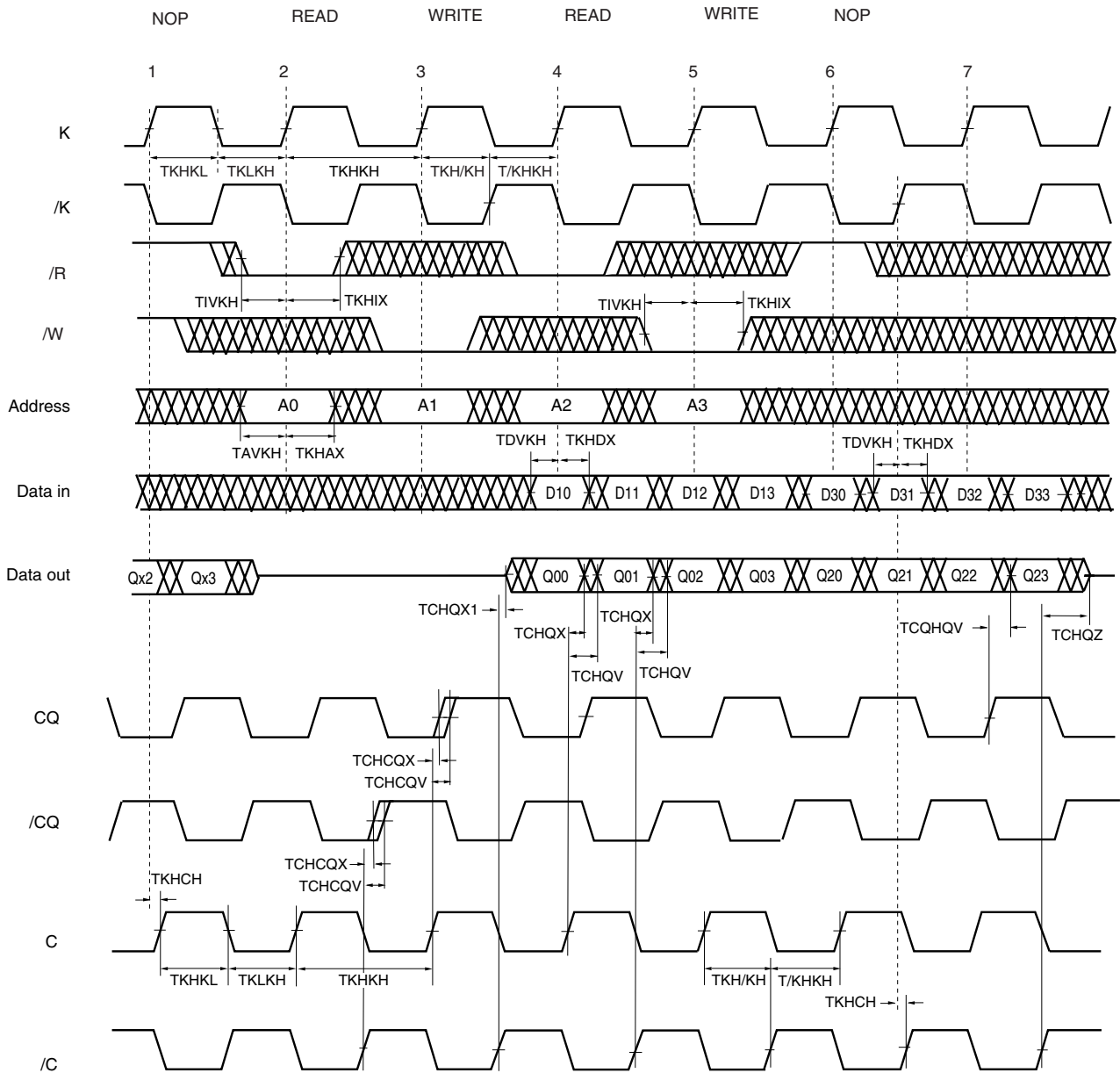
Read and Write Cycle

| Parameter | Symbol | -E33 (300 MHz) | | -E40 (250 MHz) | | -E50 (200 MHz) | | Unit | Note | |
|--|-----------|-------------------|------|-------------------|------|-------------------|------|-------|------|--|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | | |
| | | Clock | | | | | | | | |
| Average Clock cycle time (K, /K, C, /C) | TKHKH | 3.3 | 8.4 | 4.0 | 8.4 | 5.0 | 8.4 | ns | 1 | |
| Clock phase jitter (K, /K, C, /C) | TKC var | – | 0.2 | – | 0.2 | – | 0.2 | ns | 2 | |
| Clock HIGH time (K, /K, C, /C) | TKHKL | 1.32 | – | 1.6 | – | 2.0 | – | ns | | |
| Clock LOW time (K, /K, C, /C) | TKLKH | 1.32 | – | 1.6 | – | 2.0 | – | ns | | |
| Clock to /clock (K→/K, C→/C.) | TKH /KH | 1.49 | – | 1.8 | – | 2.2 | – | ns | | |
| Clock to /clock (/K→K, /C→C.) | T /KHKH | 1.49 | – | 1.8 | – | 2.2 | – | ns | | |
| Clock to data clock (K→C., /K→/C.) | TKHCH | 250 to 300 MHz | 0 | 1.45 | – | – | – | – | ns | |
| | | 200 to 250 MHz | 0 | 1.8 | 0 | 1.8 | – | – | | |
| | | 167 to 200 MHz | 0 | 2.3 | 0 | 2.3 | 0 | 2.3 | | |
| | | 133 to 167 MHz | 0 | 2.8 | 0 | 2.8 | 0 | 2.8 | | |
| | | < 133 MHz | 0 | 3.55 | 0 | 3.55 | 0 | 3.55 | | |
| DLL lock time (K, C) | TKC lock | 1,024 | – | 1,024 | – | 1,024 | – | Cycle | 3 | |
| K static to DLL reset | TKC reset | 30 | – | 30 | – | 30 | – | ns | | |
| Output Times | | | | | | | | | | |
| C, /C HIGH to output valid | TCHQV | – | 0.45 | – | 0.45 | – | 0.45 | ns | | |
| C, /C HIGH to output hold | TCHQX | – 0.45 | – | – 0.45 | – | – 0.45 | – | ns | | |
| C, /C HIGH to echo clock valid | TCHCQV | – | 0.45 | – | 0.45 | – | 0.45 | ns | | |
| C, /C HIGH to echo clock hold | TCHCQX | – 0.45 | – | – 0.45 | – | – 0.45 | – | ns | | |
| CQ, /CQ HIGH to output valid | TCQHQV | – | 0.27 | – | 0.3 | – | 0.35 | ns | 4 | |
| CQ, /CQ HIGH to output hold | TCQHQX | – 0.27 | – | – 0.3 | – | – 0.35 | – | ns | 4 | |
| C HIGH to output High-Z | TCHQZ | – | 0.45 | – | 0.45 | – | 0.45 | ns | | |
| C HIGH to output Low-Z | TCHQX1 | – 0.45 | – | – 0.45 | – | – 0.45 | – | ns | | |
| Setup Times | | | | | | | | | | |
| Address valid to K rising edge | TAVKH | 0.4 | – | 0.5 | – | 0.6 | – | ns | 5 | |
| Control inputs (/R, /W) valid to K rising edge | TIVKH | 0.4 | – | 0.5 | – | 0.6 | – | ns | 5 | |
| Data inputs and write data select inputs (/BWx, /NWx) valid to K, /K rising edge | TDVKH | 0.3 | – | 0.35 | – | 0.4 | – | ns | 5 | |
| Hold Times | | | | | | | | | | |
| K rising edge to address hold | TKHAX | 0.4 | – | 0.5 | – | 0.6 | – | ns | 5 | |
| K rising edge to control inputs (/R, /W) hold | TKHIX | 0.4 | – | 0.5 | – | 0.6 | – | ns | 5 | |
| K, /K rising edge to data inputs and write data select inputs (/BWx, /NWx) hold | TKHDX | 0.3 | – | 0.35 | – | 0.4 | – | ns | 5 | |

- Notes**
1. The device will operate at clock frequencies slower than TKHKH(MAX.).
 2. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
 3. V_{DD} slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention.
DLL lock time begins once V_{DD} and input clock are stable.
It is recommended that the device is kept inactive during these cycles.
 4. Echo clock is very tightly controlled to data valid / data hold. By design, there is a ± 0.1 ns variation from echo clock to data. The data sheet parameters reflect tester guardbands and test setup variations.
 5. This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.

- Remarks**
1. This parameter is sampled.
 2. Test conditions as specified with the output loading as shown in AC Test Conditions unless otherwise noted.
 3. Control input signals may not be operated with pulse widths less than TKHKL (MIN.).
 4. If C, /C are tied HIGH, K, /K become the references for C, /C timing parameters.
 5. V_{DDQ} is 1.5 V DC.

Read and Write Timing



- Remarks**
1. Q00 refers to output from address A0+0.
Q01 refers to output from the next internal burst address following A0, i.e., A0+1.
 2. Outputs are disable (high impedance) one clock cycle after a NOP.
 3. In this example, if address A0=A1, data Q00=D10, Q01=D11.
Write data is forwarded immediately as read results.

JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

Test Access Port (TAP) Pins

| Pin name | Pin assignments | Description |
|----------|-----------------|---|
| TCK | 2R | Test Clock Input. All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK. |
| TMS | 10R | Test Mode Select. This is the command input for the TAP controller state machine. |
| TDI | 11R | Test Data Input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction. |
| TDO | 1R | Test Data Output. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO. |

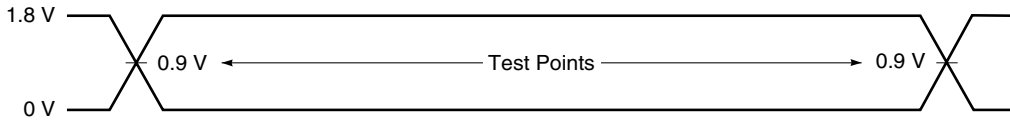
Remark The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held high for five rising edges of TCK. The TAP controller state is also reset on the SRAM POWER-UP.

JTAG DC Characteristics (T_A = 0 to 70°C, V_{DD} = 1.8 ± 0.1 V, unless otherwise noted)

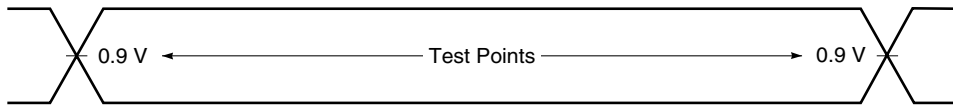
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | Note |
|----------------------------|------------------|--|------|------|----------------------|------|------|
| JTAG Input leakage current | I _{LI} | 0 V ≤ V _{IN} ≤ V _{DD} | -5.0 | - | +5.0 | μA | |
| JTAG I/O leakage current | I _{LO} | 0 V ≤ V _{IN} ≤ V _{DDQ} , Outputs disabled | -5.0 | - | +5.0 | μA | |
| JTAG input high voltage | V _{IH} | | 1.3 | - | V _{DD} +0.3 | V | |
| JTAG input low voltage | V _{IL} | | -0.3 | - | +0.5 | V | |
| JTAG output high voltage | V _{OH1} | I _{OHC} = 100 μA | 1.6 | - | - | V | |
| | V _{OH2} | I _{OHT} = 2 mA | 1.4 | - | - | V | |
| JTAG output low voltage | V _{OL1} | I _{OLC} = 100 μA | - | - | 0.2 | V | |
| | V _{OL2} | I _{OLT} = 2 mA | - | - | 0.4 | V | |

JTAG AC Test Conditions

Input waveform (Rise / Fall time ≤ 1 ns)

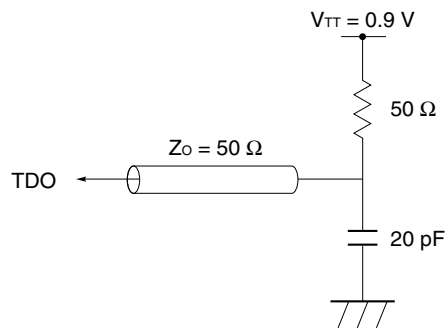


Output waveform



Output load

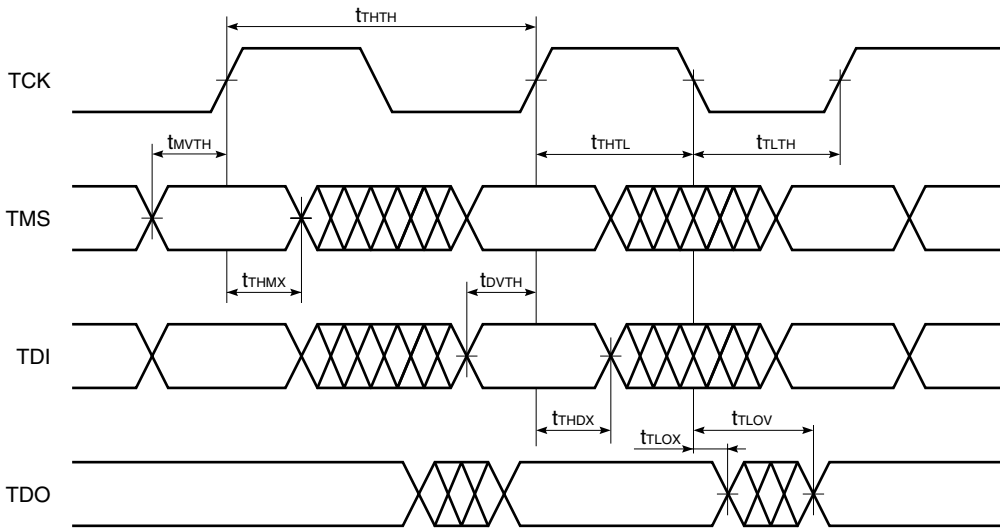
Figure 2. External load at test



JTAG AC Characteristics (T_A = 0 to 70 °C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | Note |
|-------------------------|-------------------|------------|------|------|------|------|------|
| Clock | | | | | | | |
| Clock cycle time | t _{THTH} | | 100 | – | – | ns | |
| Clock frequency | f _{TF} | | – | – | 10 | MHz | |
| Clock high time | t _{THTL} | | 40 | – | – | ns | |
| Clock low time | t _{TLTH} | | 40 | – | – | ns | |
| Output time | | | | | | | |
| TCK low to TDO unknown | t _{TLOX} | | 0 | – | – | ns | |
| TCK low to TDO valid | t _{TLOV} | | – | – | 20 | ns | |
| TDI valid to TCK high | t _{dvTH} | | 10 | – | – | ns | |
| TCK high to TDI invalid | t _{thDX} | | 10 | – | – | ns | |
| Setup time | | | | | | | |
| TMS setup time | t _{mvTH} | | 10 | – | – | ns | |
| Capture setup time | t _{cs} | | 10 | – | – | ns | |
| Hold time | | | | | | | |
| TMS hold time | t _{thMX} | | 10 | – | – | ns | |
| Capture hold time | t _{ch} | | 10 | – | – | ns | |

JTAG Timing Diagram



Scan Register Definition (1)

| Register name | Description |
|----------------------|--|
| Instruction register | The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run-test/idle or the various data register state. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state. |
| Bypass register | The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible. |
| ID register | The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state. |
| Boundary register | The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register. The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The second column is the name of the input or I/O at the bump and the third column is the bump number. |

Scan Register Definition (2)

| Register name | Bit size | Unit |
|----------------------|----------|------|
| Instruction register | 3 | bit |
| Bypass register | 1 | bit |
| ID register | 32 | bit |
| Boundary register | 109 | bit |

ID Register Definition

| Part number | Organization | ID [31:28] vendor revision no. | ID [27:12] part no. | ID [11:1] vendor ID no. | ID [0] fix bit |
|-------------|--------------|--------------------------------|---------------------|-------------------------|----------------|
| μPD44325084 | 4M x 8 | XXXX | 0000 0000 0100 1101 | 00000010000 | 1 |
| μPD44325094 | 4M x 9 | XXXX | 0000 0000 0100 1110 | 00000010000 | 1 |
| μPD44325184 | 2M x 18 | XXXX | 0000 0000 0100 1111 | 00000010000 | 1 |
| μPD44325364 | 1M x 36 | XXXX | 0000 0000 0101 0000 | 00000010000 | 1 |

SCAN Exit Order

| Bit no. | Signal name | | | | Bump ID |
|---------|-------------|----|-----|-----|---------|
| | x8 | x9 | x18 | x36 | |
| 1 | /C | | | | 6R |
| 2 | C | | | | 6P |
| 3 | A | | | | 6N |
| 4 | A | | | | 7P |
| 5 | A | | | | 7N |
| 6 | A | | | | 7R |
| 7 | A | | | | 8R |
| 8 | A | | | | 8P |
| 9 | A | | | | 9R |
| 10 | NC | Q0 | Q0 | Q0 | 11P |
| 11 | NC | D0 | D0 | D0 | 10P |
| 12 | NC | NC | NC | D9 | 10N |
| 13 | NC | NC | NC | Q9 | 9P |
| 14 | NC | NC | Q1 | Q1 | 10M |
| 15 | NC | NC | D1 | D1 | 11N |
| 16 | NC | NC | NC | D10 | 9M |
| 17 | NC | NC | NC | Q10 | 9N |
| 18 | Q0 | Q1 | Q2 | Q2 | 11L |
| 19 | D0 | D1 | D2 | D2 | 11M |
| 20 | NC | NC | NC | D11 | 9L |
| 21 | NC | NC | NC | Q11 | 10L |
| 22 | NC | NC | Q3 | Q3 | 11K |
| 23 | NC | NC | D3 | D3 | 10K |
| 24 | NC | NC | NC | D12 | 9J |
| 25 | NC | NC | NC | Q12 | 9K |
| 26 | Q1 | Q2 | Q4 | Q4 | 10J |
| 27 | D1 | D2 | D4 | D4 | 11J |
| 28 | ZQ | | | | 11H |
| 29 | NC | NC | NC | D13 | 10G |
| 30 | NC | NC | NC | Q13 | 9G |
| 31 | NC | NC | Q5 | Q5 | 11F |
| 32 | NC | NC | D5 | D5 | 11G |
| 33 | NC | NC | NC | D14 | 9F |
| 34 | NC | NC | NC | Q14 | 10F |
| 35 | Q2 | Q3 | Q6 | Q6 | 11E |
| 36 | D2 | D3 | D6 | D6 | 10E |

| Bit no. | Signal name | | | | Bump ID |
|---------|-----------------|------|------|------|---------|
| | x8 | x9 | x18 | x36 | |
| 37 | NC | NC | NC | D15 | 10D |
| 38 | NC | NC | NC | Q15 | 9E |
| 39 | NC | NC | Q7 | Q7 | 10C |
| 40 | NC | NC | D7 | D7 | 11D |
| 41 | NC | NC | NC | D16 | 9C |
| 42 | NC | NC | NC | Q16 | 9D |
| 43 | Q3 | Q4 | Q8 | Q8 | 11B |
| 44 | D3 | D4 | D8 | D8 | 11C |
| 45 | NC | NC | NC | D17 | 9B |
| 46 | NC | NC | NC | Q17 | 10B |
| 47 | CQ | | | | 11A |
| 48 | V _{SS} | | | | 10A |
| 49 | A | | | | 9A |
| 50 | A | | | | 8B |
| 51 | A | | | | 7C |
| 52 | NC | | | | 6C |
| 53 | /R | | | | 8A |
| 54 | NC | NC | NC | /BW1 | 7A |
| 55 | /NW0 | /BW0 | /BW0 | /BW0 | 7B |
| 56 | K | | | | 6B |
| 57 | /K | | | | 6A |
| 58 | NC | NC | NC | /BW3 | 5B |
| 59 | /NW1 | NC | /BW1 | /BW2 | 5A |
| 60 | /W | | | | 4A |
| 61 | A | | | | 5C |
| 62 | A | | | | 4B |
| 63 | A | A | A | NC | 3A |
| 64 | V _{SS} | | | | 2A |
| 65 | /CQ | | | | 1A |
| 66 | NC | NC | Q9 | Q18 | 2B |
| 67 | NC | NC | D9 | D18 | 3B |
| 68 | NC | NC | NC | D27 | 1C |
| 69 | NC | NC | NC | Q27 | 1B |
| 70 | NC | NC | Q10 | Q19 | 3D |
| 71 | NC | NC | D10 | D19 | 3C |
| 72 | NC | NC | NC | D28 | 1D |

| Bit no. | Signal name | | | | Bump ID |
|---------|-------------|----|-----|-----|----------|
| | x8 | x9 | x18 | x36 | |
| 73 | NC | NC | NC | Q28 | 2C |
| 74 | Q4 | Q5 | Q11 | Q20 | 3E |
| 75 | D4 | D5 | D11 | D20 | 2D |
| 76 | NC | NC | NC | D29 | 2E |
| 77 | NC | NC | NC | Q29 | 1E |
| 78 | NC | NC | Q12 | Q21 | 2F |
| 79 | NC | NC | D12 | D21 | 3F |
| 80 | NC | NC | NC | D30 | 1G |
| 81 | NC | NC | NC | Q30 | 1F |
| 82 | Q5 | Q6 | Q13 | Q22 | 3G |
| 83 | D5 | D6 | D13 | D22 | 2G |
| 84 | /DLL | | | | 1H |
| 85 | NC | NC | NC | D31 | 1J |
| 86 | NC | NC | NC | Q31 | 2J |
| 87 | NC | NC | Q14 | Q23 | 3K |
| 88 | NC | NC | D14 | D23 | 3J |
| 89 | NC | NC | NC | D32 | 2K |
| 90 | NC | NC | NC | Q32 | 1K |
| 91 | Q6 | Q7 | Q15 | Q24 | 2L |
| 92 | D6 | D7 | D15 | D24 | 3L |
| 93 | NC | NC | NC | D33 | 1M |
| 94 | NC | NC | NC | Q33 | 1L |
| 95 | NC | NC | Q16 | Q25 | 3N |
| 96 | NC | NC | D16 | D25 | 3M |
| 97 | NC | NC | NC | D34 | 1N |
| 98 | NC | NC | NC | Q34 | 2M |
| 99 | Q7 | Q8 | Q17 | Q26 | 3P |
| 100 | D7 | D8 | D17 | D26 | 2N |
| 101 | NC | NC | NC | D35 | 2P |
| 102 | NC | NC | NC | Q35 | 1P |
| 103 | A | | | | 3R |
| 104 | A | | | | 4R |
| 105 | A | | | | 4P |
| 106 | A | | | | 5P |
| 107 | A | | | | 5N |
| 108 | A | | | | 5R |
| 109 | - | | | | Internal |

JTAG Instructions

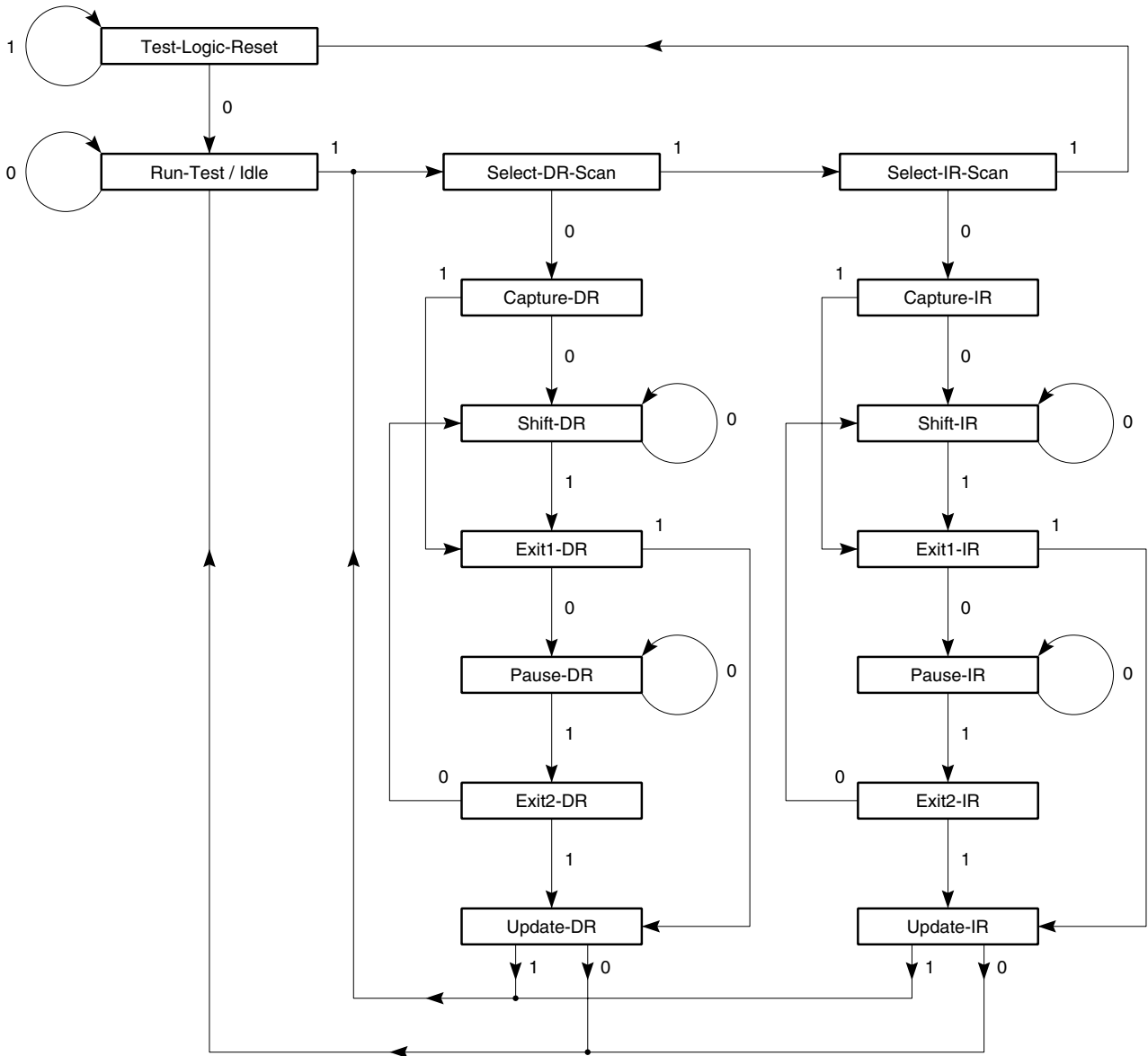
| Instructions | Description |
|------------------|---|
| EXTEST | The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output pins are used to apply test vectors, while those at input pins capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output drive is turned on and the PRELOAD data is driven onto the output pins. |
| IDCODE | The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test-logic-reset state. |
| BYPASS | The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path. |
| SAMPLE / PRELOAD | SAMPLE / PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and Q pins into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t_{cs} plus t_{ch}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO pins. |
| SAMPLE-Z | If the SAMPLE-Z instruction is loaded in the instruction register, all RAM Q pins are forced to an inactive drive state (high impedance) and the boundary register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state. |

JTAG Instruction Coding

| IR2 | IR1 | IR0 | Instruction | Note |
|-----|-----|-----|------------------|------|
| 0 | 0 | 0 | EXTEST | |
| 0 | 0 | 1 | IDCODE | |
| 0 | 1 | 0 | SAMPLE-Z | 1 |
| 0 | 1 | 1 | RESERVED | |
| 1 | 0 | 0 | SAMPLE / PRELOAD | |
| 1 | 0 | 1 | RESERVED | |
| 1 | 1 | 0 | RESERVED | |
| 1 | 1 | 1 | BYPASS | |

Note 1. TRISTATE all Q pins and CAPTURE the pad values into a SERIAL SCAN LATCH.

TAP Controller State Diagram



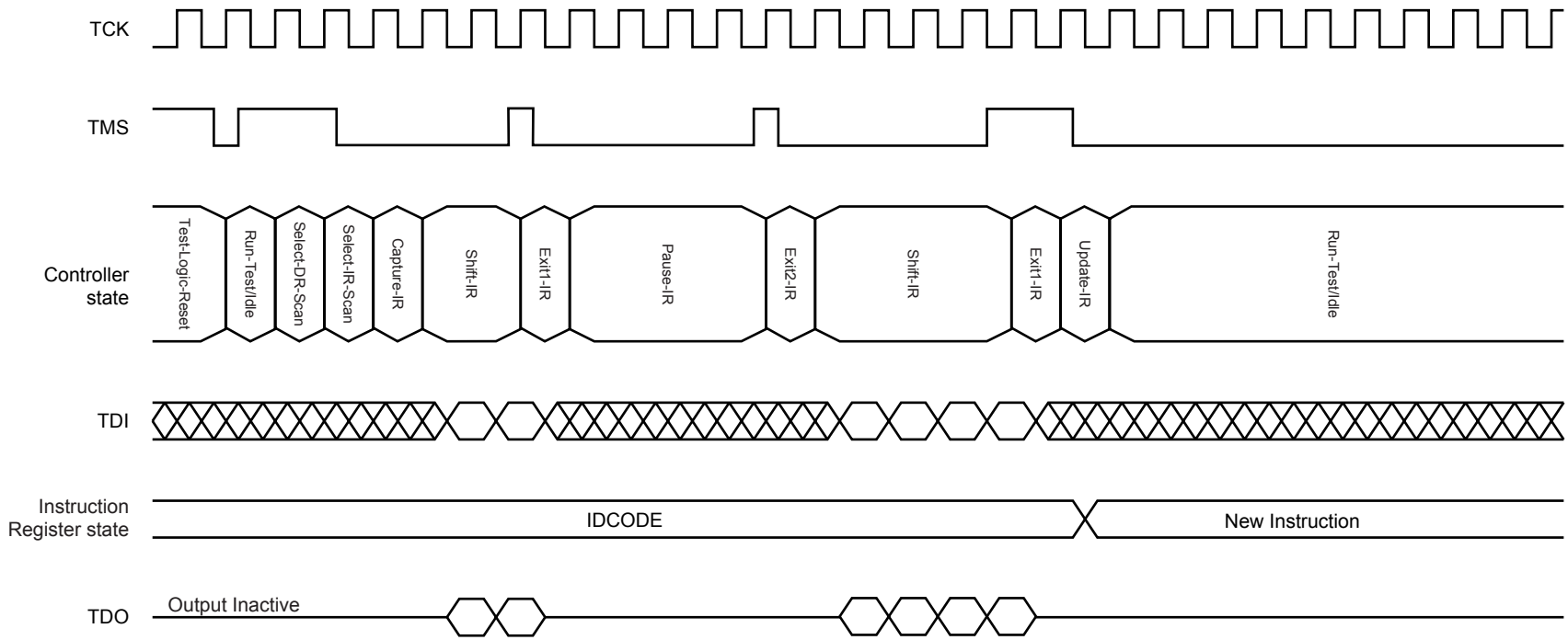
Disabling the Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to Vss to preclude mid level inputs.

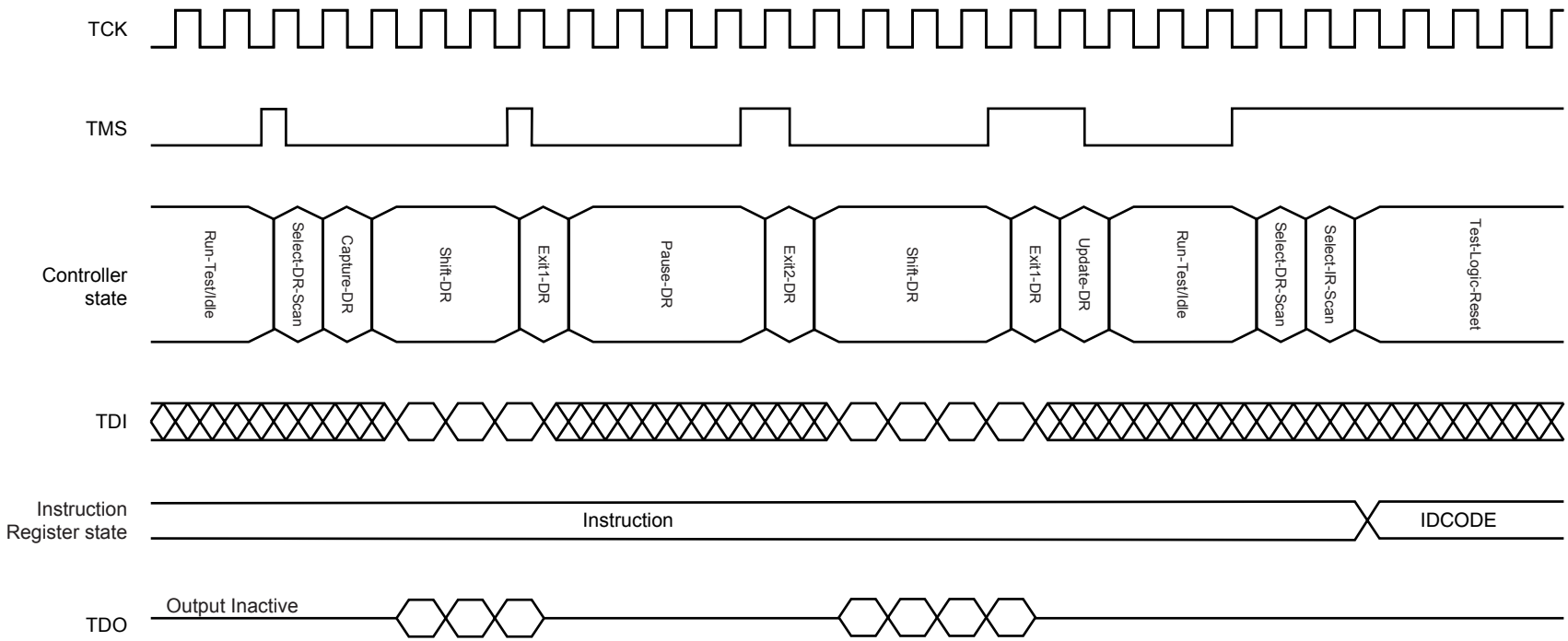
TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a 1 kΩ resistor.

TDO should be left unconnected.

Test Logic Operation (Instruction Scan)

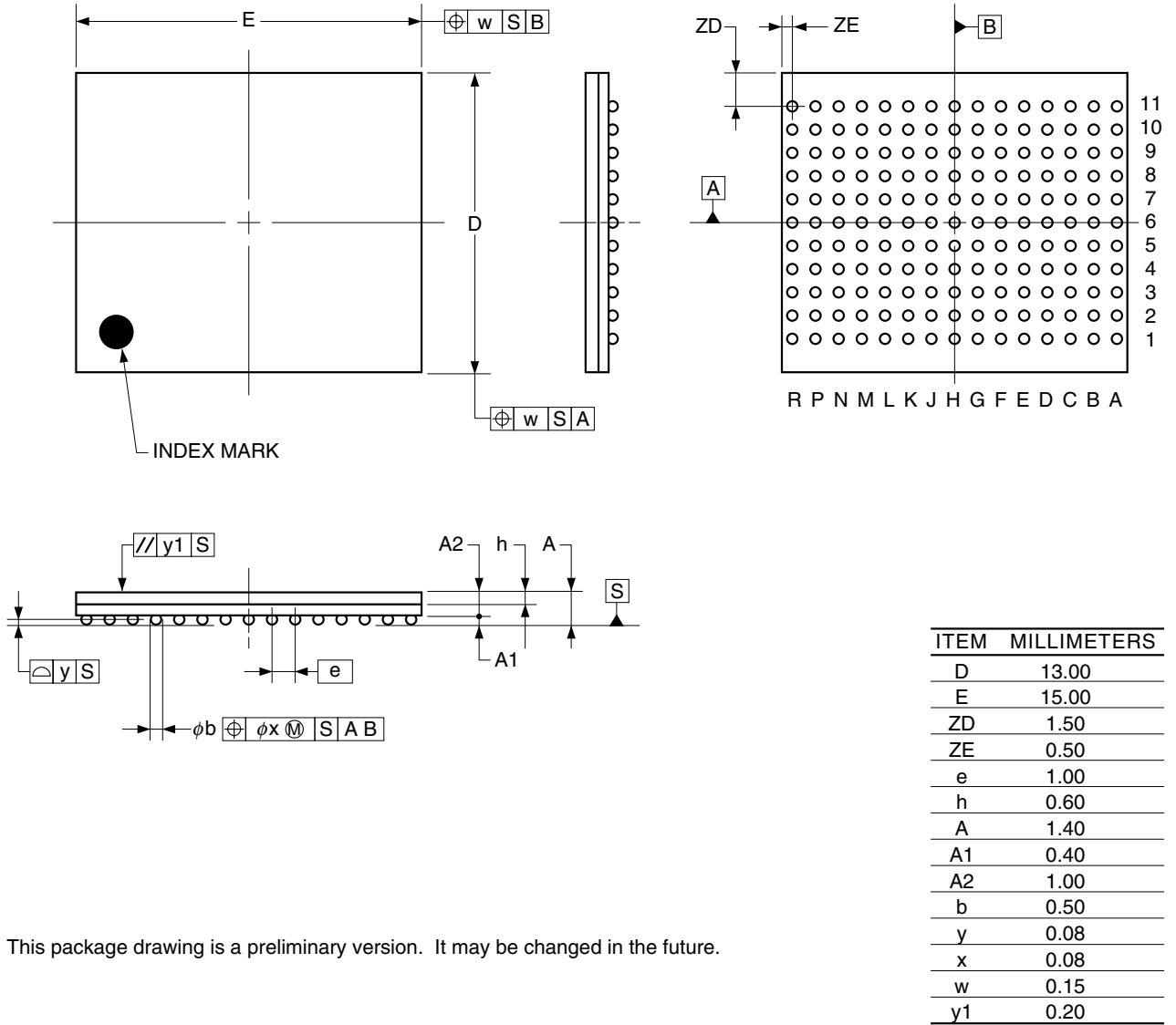


Test Logic (Data Scan)



Package Drawing

165-PIN PLASTIC FBGA (13x15)



This package drawing is a preliminary version. It may be changed in the future.

Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of these products.

★ Types of Surface Mount Devices

μ PD44325084F5-EQ2: 165-pin PLASTIC FBGA (13 x 15)

μ PD44325094F5-EQ2: 165-pin PLASTIC FBGA (13 x 15)

μ PD44325184F5-EQ2: 165-pin PLASTIC FBGA (13 x 15)

μ PD44325364F5-EQ2: 165-pin PLASTIC FBGA (13 x 15)

Revision History

| Edition/ Date | Page | | Type of revision | Location | Description (Previous edition → This edition) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|-----------------|---------------------|--|--|---|------|--|--|------|--------|-----|-----|------|-----|-----|-----|------|------|-----|------|-----|------|-----|------|-----|--|------|--------|-----|------|--------|-----|-----|------|------|-------|-------|------|------|-----|-----|-------|------|-----|-----|-----|
| | This edition | Previous edition | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1st edition/ Oct. 2004 | Throughout | Throughout | Modification | — | Preliminary Product Information → Preliminary Data sheet | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | Package Code | F5-EQ1 → F5-EQ2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Deletion | — | -E60 (167MHz) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | p.2 | p.2 | Addition | Ordering Information | "Note Under development" has been added to -E33. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | pp.3-6 | pp.3-6 | | Pin Configurations | Remark 2 has been added | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | p.9 | — | | Power-on Sequence | Power-on sequence has been added | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| p.15 | p.15 | Modification | DC Characteristics I _{DD} (MAX.) | <table border="1"> <thead> <tr> <th rowspan="2"></th> <th colspan="3">MAX.</th> <th rowspan="2">Unit</th> </tr> <tr> <th>x8, x9</th> <th>x18</th> <th>x36</th> </tr> </thead> <tbody> <tr> <td>-E33</td> <td>840</td> <td>860</td> <td>910</td> <td rowspan="3">mA</td> </tr> <tr> <td>-E40</td> <td>730</td> <td>750</td> <td>800</td> </tr> <tr> <td>-E50</td> <td>630</td> <td>650</td> <td>700</td> </tr> </tbody> </table> → <table border="1"> <thead> <tr> <th rowspan="2"></th> <th colspan="3">MAX.</th> <th rowspan="2">Unit</th> </tr> <tr> <th>x8, x9</th> <th>x18</th> <th>x36</th> </tr> </thead> <tbody> <tr> <td>-E33</td> <td>800</td> <td>1,100</td> <td>1,250</td> <td rowspan="3">mA</td> </tr> <tr> <td>-E40</td> <td>700</td> <td>950</td> <td>1,050</td> </tr> <tr> <td>-E50</td> <td>600</td> <td>800</td> <td>900</td> </tr> </tbody> </table> | | MAX. | | | Unit | x8, x9 | x18 | x36 | -E33 | 840 | 860 | 910 | mA | -E40 | 730 | 750 | 800 | -E50 | 630 | 650 | 700 | | MAX. | | | Unit | x8, x9 | x18 | x36 | -E33 | 800 | 1,100 | 1,250 | mA | -E40 | 700 | 950 | 1,050 | -E50 | 600 | 800 | 900 |
| | MAX. | | | Unit | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | x8, x9 | x18 | x36 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| -E33 | 840 | 860 | 910 | mA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| -E40 | 730 | 750 | 800 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| -E50 | 630 | 650 | 700 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | MAX. | | | Unit | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | x8, x9 | x18 | x36 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| -E33 | 800 | 1,100 | 1,250 | mA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| -E40 | 700 | 950 | 1,050 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| -E50 | 600 | 800 | 900 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | DC Characteristics I _{SB1} (MAX.) | <table border="1"> <thead> <tr> <th rowspan="2"></th> <th colspan="3">MAX.</th> <th rowspan="2">Unit</th> </tr> <tr> <th>x8, x9</th> <th>x18</th> <th>x36</th> </tr> </thead> <tbody> <tr> <td>-E33</td> <td colspan="2">290</td> <td rowspan="3">mA</td> </tr> <tr> <td>-E40</td> <td colspan="2">250</td> </tr> <tr> <td>-E50</td> <td colspan="2">210</td> </tr> </tbody> </table> → <table border="1"> <thead> <tr> <th rowspan="2"></th> <th colspan="3">MAX.</th> <th rowspan="2">Unit</th> </tr> <tr> <th>x8, x9</th> <th>x18</th> <th>x36</th> </tr> </thead> <tbody> <tr> <td>-E33</td> <td colspan="2">450</td> <td rowspan="3">mA</td> </tr> <tr> <td>-E40</td> <td colspan="2">400</td> </tr> <tr> <td>-E50</td> <td colspan="2">350</td> </tr> </tbody> </table> | | MAX. | | | Unit | x8, x9 | x18 | x36 | -E33 | 290 | | mA | -E40 | 250 | | -E50 | 210 | | | MAX. | | | Unit | x8, x9 | x18 | x36 | -E33 | 450 | | mA | -E40 | 400 | | -E50 | 350 | | | | | | | |
| | MAX. | | | Unit | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | x8, x9 | x18 | x36 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| -E33 | 290 | | mA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| -E40 | 250 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| -E50 | 210 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | MAX. | | | Unit | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | x8, x9 | x18 | x36 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| -E33 | 450 | | mA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| -E40 | 400 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| -E50 | 350 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

[MEMO]

[MEMO]

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NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

QDR RAMs and Quad Data Rate RAMs comprise a new series of products developed by Cypress Semiconductor, Renesas, IDT, Micron Technology, Inc., NEC Electronics, and Samsung.

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