Si5350A

FACTORY-PROGRAMMABLE ANY-FREQUENCY CMOS CLOCK GENERATOR

Features

- Generates up to 8 non-integer frequencies from 8 kHz to 125 MHz
- Exact frequency synthesis at each output (0 ppm error)
- Glitchless frequency changes
- Low output period jitter: 100 ps pp
- Configurable Spread Spectrum selectable at each output
- User-configurable control pins:
  - Output Enable (OEB_0/1/2)
  - Power Down (PDN)
  - Frequency Select (FS_0/1)
  - Spread Spectrum Enable (SSEN)
- Operates from a low-cost, fixed frequency crystal: 25 or 27 MHz
- Separate voltage supply pins:
  - Core VDD: 2.5 V or 3.3 V
  - Output VDDO: 2.5 V or 3.3 V
- Excellent PSRR eliminates external power supply filtering
- Very low power consumption (<15 mA)
- Available in 3 packages types:
  - 10-MSOP: 3 outputs
  - 24-QSOP: 8 outputs
  - 20-QFN (4x4 mm): 8 outputs

10-MSOP

24-QSOP

20-QFN

Ordering Information:

See page 18

Applications

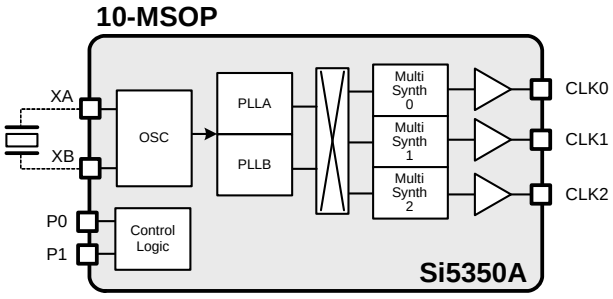
- HDTV, DVD/Blu-ray, set-top box
- Audio/video equipment, gaming
- Printers, scanners, projectors
- Residential gateways
- Networking/communication
- Servers, storage

Description

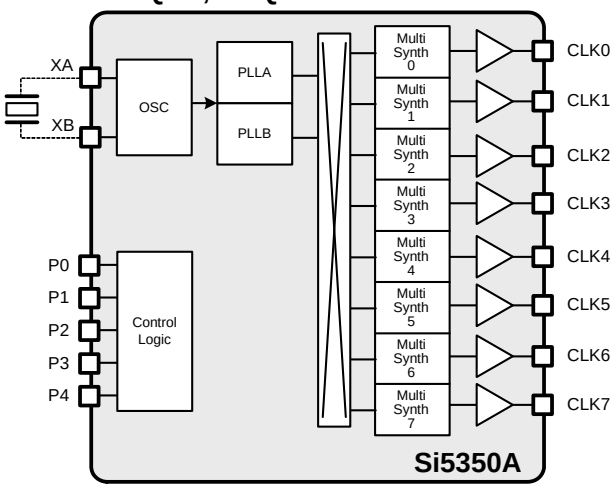
The Si5350A is a user-definable custom clock generator that is ideally suited for replacing crystals and crystal oscillators in cost-sensitive applications. Based on a PLL + high resolution fractional divider MultiSynth™ architecture, the Si5350A can generate any frequency up to 125 MHz on each of its outputs with 0 ppm error. Spread spectrum is selectable (on/off) on any of the outputs. Custom pin-controlled Si5350A devices can be requested using the ClockBuilder web-based part number utility (www.silabs.com/ClockBuilder).

Functional Block Diagram

10-MSOP



20-QFN, 24-QSOP



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Core Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
Output Buffer Voltage	V_{DDOx}		2.25	2.5	2.75	V
			2.97	3.3	3.63	V
Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.						

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD_max}		–0.5 to 3.8	V
Input Voltage	V_{IN_P1-4}	Pins P1, P2, P3, P4	–0.5 to 3.8	V
	V_{IN_P0}	P0	–0.5 to (V_{DD}+0.3)	V
	$V_{IN\_XA/B}$	Pins XA, XB	–0.5 to 1.3 V	V
Storage Temperature Range	T_{STG}		–55 to 150	°C
Operating Junction Temperature	T_{JCT}		–55 to 150	°C
Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.				

Table 3. DC Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current	I_{DD}	Enabled 3 outputs	—	20	26	mA
		Enabled 8 outputs	—	25	38	mA
		Power Down (PDN = V_{DD})	—	50	—	µA
Output Buffer Supply Current	I_{DDOx}	C_L = 5 pF	—	2.5	4	mA
Input Current	I_{P1-P4}	Pins P1, P2, P3, P4 Vin < 3.6V	—	—	10	µA
	I_{P0}	Pin P0	—	—	30	µA

Table 4. AC Characteristics

((V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power-up Time	T_{RDY}	From V_{DD} = V_{DDmin} to valid output clock, C_L = 15 pF, f_{CLKn} > 1 MHz	—	1	10	ms
Output Enable Time	T_{OE}	From OEB assertion to valid clock output, C_L = 15 pF, f_{CLKn} > 1 MHz	—	—	10	µs
Output Frequency Transition Time	T_{FREQ}	Time to settle to within ± 20 ppm of specified frequency upon change in frequency plan via FS pin, f_{CLKn} > 1 MHz	—	100	—	µs
Minimum Pulse Width	T_{PW_PDN}	Power down pin (PDN)	100	—	—	ms
	T_{PW_P0-4}	Control pin (P0-P4)	200	—	—	ns
Spread Spectrum Frequency Deviation	SS_{DEV}	Down spread	–0.5	—	–2.5	%
Spread Spectrum Modulation Rate	SS_{MOD}		30	31.5	33	kHz

Table 5. Thermal Characteristics

Parameter	Symbol	Test Condition	Package	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	10-MSOP	131	°C/W
			24-QSOP	80	°C/W
			20-QFN	51	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	10-MSOP	43	°C/W
			24-QSOP	31	°C/W
			20-QFN	16	°C/W

Table 6. Input Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Crystal Frequency	f_{XTAL}		25	—	27	MHz
P0-P4 Input Low Voltage	$V_{IL\text{-}P0\text{-}4}$		–0.1	—	0.3 x V_{DD}	V
P0-P4 Input High Voltage	$V_{IH\_P0\text{-}4}$		0.7 x V_{DD}	—	3.63	V

Table 7. Output Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency Range	F_{CLK}		0.008		125	MHz
Load Capacitance	C_L	F_{CLK} < 100 MHz	—	5	15	pF
Duty Cycle	DC	Measured at $V_{DD}/2$	45	50	55	%
Rise/Fall Time	t_r/t_f	20%–80%, C_L = 5 pF	0.6	1	1.3	ns
Output High Voltage	V_{OH}		V_{DD} – 0.6	—	—	V
Output Low Voltage	V_{OL}		—	—	0.6	V
Period Jitter	J_{PER}	Measured over 10k cycles	—	35	100	ps pk-pk
Cycle-to-Cycle Jitter	J_{CC}	Measured over 10k cycles	—	30	90	ps pk-pk
RMS Phase Jitter	J_{RMS}	12 kHz–20 MHz	—	3.5	11	ps rms

Table 8. 25 MHz Crystal Requirements[1,2]

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	—	25	—	MHz
Load Capacitance	C_L	6	—	12	pF
Equivalent Series Resistance	r_{ESR}	—	—	150	Ω
Crystal Max Drive Level	d_L	—	—	150	µW

Notes:
1. Crystals which require load capacitances of 6, 8, or 10 pF should use the device's internal load capacitance for optimum performance. See register 183 bits 7:6. A crystal with a 12 pF load capacitance requirement should use a combination of the internal 10 pF load capacitors in addition to external 2 pF load capacitors.
2. Refer to "AN551: Crystal Selection Guide" for more details.

Table 9. 27 MHz Crystal Requirements[1,2]

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	—	27	—	MHz
Load Capacitance	C_L	6	—	12	pF
Equivalent Series Resistance	r_{ESR}	—	—	150	Ω
Crystal Max Drive Level Spec	d_L	—	—	150	µW

Notes:
1. Crystals which require load capacitances of 6, 8, or 10 pF should use the device's internal load capacitance for optimum performance. See register 183 bits 7:6. A crystal with a 12 pF load capacitance requirement should use a combination of the internal 10 pF load capacitors in addition to external 2 pF load capacitors.
2. Refer to "AN551: Crystal Selection Guide" for more details.

2. Typical Application

The Si5350A is a user-definable custom clock generator that is ideally suited for replacing crystals and crystal oscillators in cost-sensitive applications. An example application is shown in Figure 1.

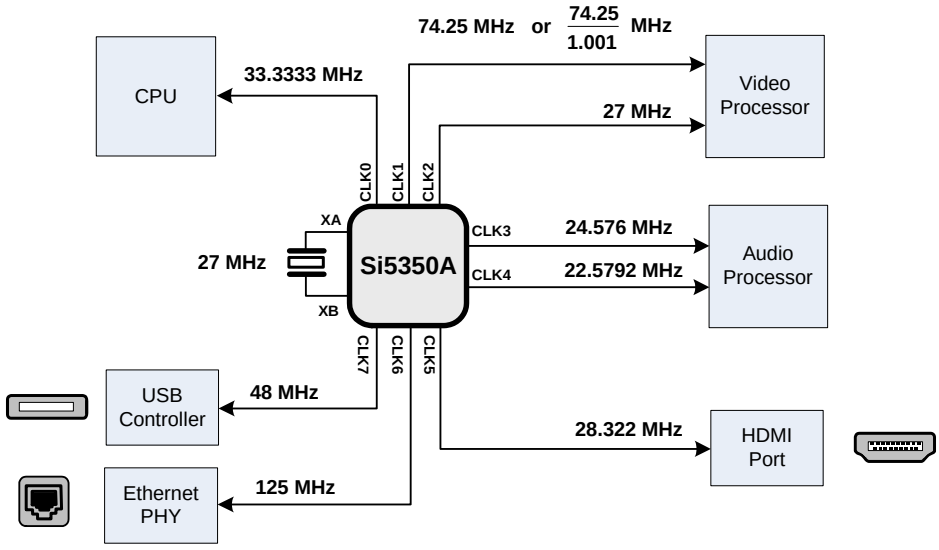


Figure 1. Example of an Si5350A in an Audio/Video Application

3. Functional Description

The Si5350A's synthesis architecture consists of two high-frequency PLLs in addition to one high-resolution fractional MultiSynth™ divider per output. A block diagram of both the 3-output and 8-output versions are shown in Figure 2. This unique architecture allows the Si5350A to generate up to eight independent, non-integer-related frequencies at any of its outputs. Each MultiSynth™ is configurable with two frequencies (F1_x, F2_x). This allows a pin controlled glitchless frequency change at each output (CLK0 to CLK5).

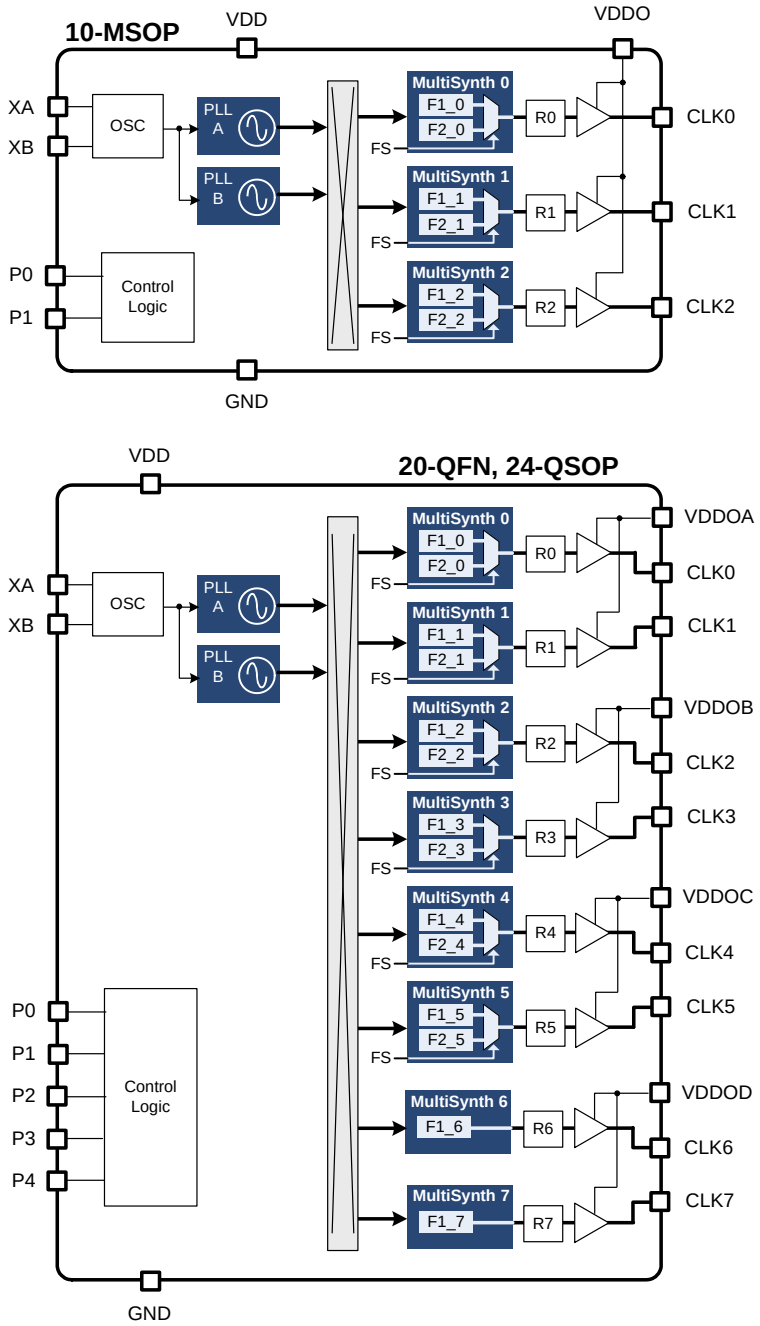


Figure 2. Block Diagrams of 3-Output and 8-Output Si5350A Devices

4. Configuring the Si5350A

The Si5350A is a factory-programmed custom clock generator that is user definable with a simple to use web-based utility (www.silabs.com/ClockBuilder). The ClockBuilder utility provides a simple graphical interface that allows the user to enter input and output frequencies along with other custom features as described in the following sections. All synthesis calculations are automatically performed by ClockBuilder to ensure an optimum configuration. A unique part number is assigned to each custom configuration.

4.1. Crystal Inputs (XA, XB)

The Si5350A uses a fixed-frequency standard AT-cut crystal as a reference to synthesize its output clocks.

4.1.1. Crystal Frequency

The Si5350A can operate using either a 27 MHz or a 25 MHz crystal.

4.1.2. Internal XTAL Load Capacitors

Internal load capacitors (C_L) are provided to eliminate the need for external components when connecting a XTAL to the Si5350A. Options for internal load capacitors are 6, 8, or 10 pF, or no internal load capacitors. XTALs with alternate load capacitance requirements are supported using external load capacitors as shown in Figure 3.

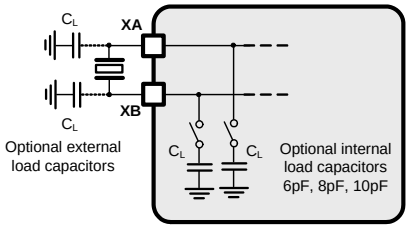


Figure 3. External XTAL with Optional Load Capacitors

4.2. Output Clocks (CLK0–CLK7)

The Si5350A is orderable as a 3-output (10-MSOP) or 8-output (24-QSOP, 20-QFN) clock generator. Output clocks CLK0 to CLK5 can be ordered with two clock frequencies (F1_x, F2_x) which are selectable with the optional frequency select pins (FS0/1). See “4.3.3. Frequency Select (FS_0, FS_1)” for more details on the operation of the frequency select pins.

4.2.1. Output Clock Frequency

Outputs can be configured at any frequency from 8 kHz up to 100 MHz. In addition, the device can generate any frequency up to 125 MHz on two of its outputs.

4.2.2. .Spread Spectrum

Spread spectrum can be enabled on any of the clock outputs for reducing electromagnetic interference (EMI). Enabling spread spectrum on an output clock modulates its frequency, which effectively reduces the overall amplitude of its radiated energy. Up to –15 dB reduction in EMI is possible.

The Si5350A supports several levels of spread spectrum allowing the designer to chose an ideal compromise between system performance and EMI compliance. The amount of spread is configurable within the following parameters:

- Down spread: –0.5 to –2.5% modulation amplitude

An optional spread spectrum enable pin (SSEN) is configurable to enable or disable the spread spectrum feature. See “4.3.1. Spread Spectrum Enable (SSEN)” for details.

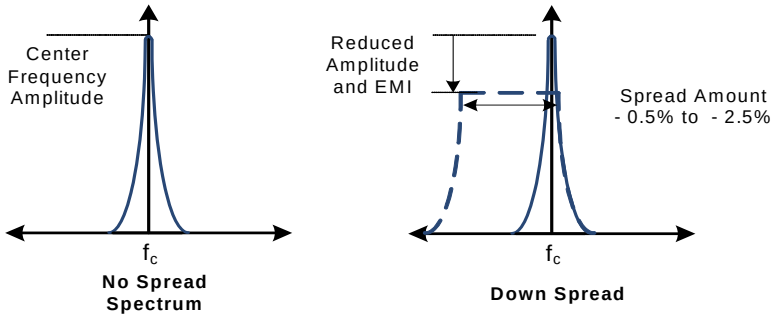


Figure 4. Available Spread Spectrum Profiles

4.2.3. Invert/Non-Invert

By default, each of the output clocks are generated in phase (non-inverted) with respect to each other. An option to invert any of the clock outputs is also available.

4.2.4. Output State When Disabled

There are up to three output enable pins configurable on the Si5350A as described in “4.3.4. Output Enable (OEB_0, OEB_1, OEB_2)” . The output state when disabled for each of the outputs is configurable as one of the following: disable low, disable high, or disable in high-impedance.

4.2.5. Powering Down Unused Outputs

Unused clock outputs can be completely powered down to conserve power.

4.3. Programmable Control Pins (P0–P4) Options

Up to five programmable control pins (P0-P4) are configurable allowing direct pin control of the following features:

4.3.1. Spread Spectrum Enable (SSEN)

An optional control pin allows disabling the spread spectrum feature for all outputs that were configured with spread spectrum enabled. Hold SSEN low to disable spread spectrum. The SSEN pin provides a convenient method of evaluating the effect of using spread spectrum clocks during EMI compliance testing.

4.3.2. Power Down (PDN)

An optional power down control pin allows a full shutdown of the Si5350A to minimize power consumption when its output clocks are not being used. The Si5350A is in normal operation when the PDN pin is held low and is in power down mode when held high. Power consumption when the device is in power down mode is indicated in Table 3 on page 4.

4.3.3. Frequency Select (FS_0, FS_1)

The Si5350A offers the option of configuring up to two frequencies per clock output on CLK0-CLK5. This is a useful feature for applications that need to support more than one clock rate on the same output. An example of this is shown in Figure 5 where the FS pins selects which frequency is generated from the clock output: F1_0 is generated when FS is set low, and F2_0 is generated when FS is set high.

FS0 Bit Level	Output Frequency Selected
0	F1_0: 74.25 MHz
1	F2_0: $\frac{74.25}{1.001}$ MHz

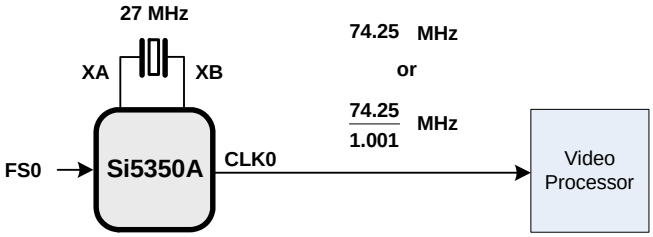


Figure 5. Example of Generating Two Clock Frequencies from the Same Clock Output

Up to two frequency select pins are available on the Si5350A. Each of the frequency select pins can be linked to any of the clock outputs as shown in Figure 6. For example, FS_0 can be linked to control clock frequency selection on CLK0, CLK3, and CLK5; FS_1 can be used to control clock frequency selection on CLK1, CLK2, and CLK4. Any other combination is also possible.

The Si5350A uses control circuitry to ensure that frequency changes are glitchless. This ensures that the clock always completes its last cycle before starting a new clock cycle of a different frequency.

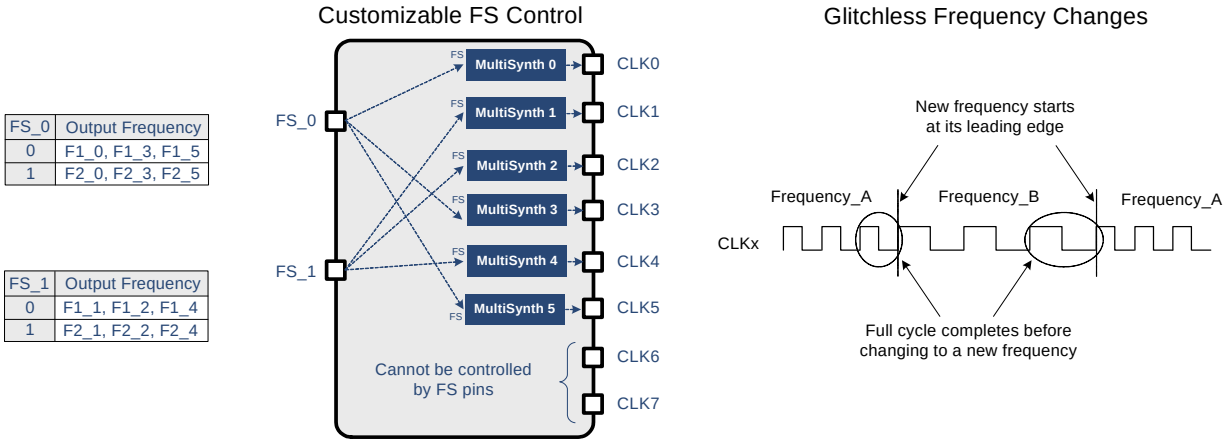


Figure 6. Example Configuration of a Pin-Controlled Frequency Select (FS)

4.3.4. Output Enable (OEB_0, OEB_1, OEB_2)

Up to three output enable pins (OEB_0/1/2) are available on the Si5350A. Similar to the FS pins, each OEB pin can be linked to any of the output clocks. In the example shown in Figure 7, OEB_0 is linked to control CLK0, CLK3, and CLK5; OEB_1 is linked to control CLK6 and CLK7, and OEB_2 is linked to control CLK1, CLK2, CLK4, and CLK5. Any other combination is also possible. If more than one OEB pin is linked to the same CLK output, the pin forcing a disable state will be dominant. Clock outputs are enabled when the OEB pin is held low.

The output enable control circuitry ensures glitchless operation by starting the output clock cycle on the first leading edge after OEB is asserted (OEB = low). When OEB is released (OEB = high), the clock is allowed to complete its full clock cycle before going into a disabled state. This is shown in Figure 7. When disabled, the output state is configurable as disabled high, disabled low, or disabled in high-impedance.

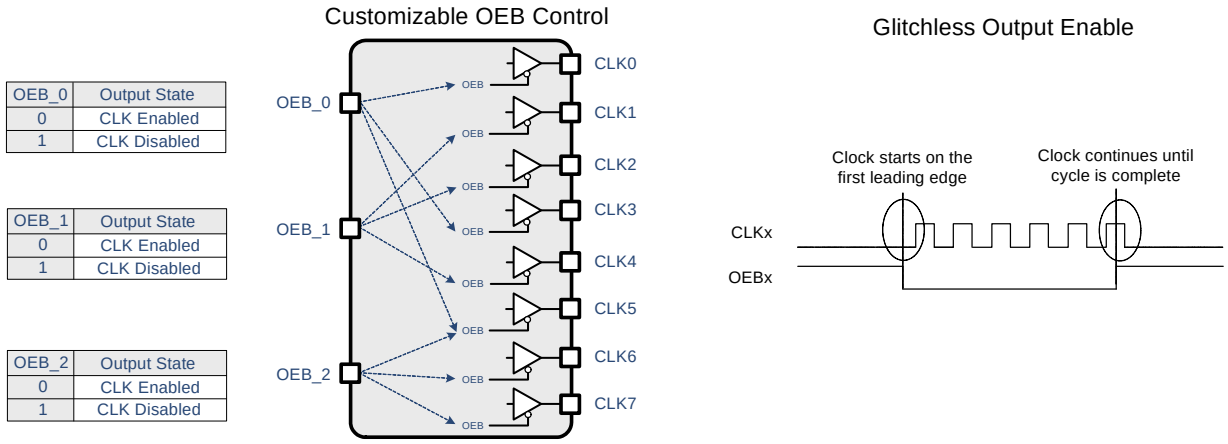


Figure 7. Example Configuration of a Pin-Controlled Output Enable

4.4. Design Considerations

The Si5350A is a self-contained clock generator that requires very few external components. The following general guidelines are recommended to ensure optimum performance.

4.4.1. Power Supply Decoupling/Filtering

The Si5350A has built-in power supply filtering circuitry to help keep the number of external components to a minimum. All that is recommended is one 0.1 µF decoupling capacitor per power supply pin. This capacitor should be mounted as close to the VDD and VDDO pins as possible without using vias.

4.4.2. Power Supply Sequencing

The VDD and VDDOx (i.e., VDDO0, VDDO1, VDDO2, VDDO3) power supply pins have been separated to allow flexibility in output signal levels. It is important that power is applied to all supply pins (VDD, VDDOx) at the same time. Unused VDDOx pins should be tied to VDD.

4.4.3. External Crystal

The external crystal should be mounted as close to the pins as possible using short PCB traces. The XA and XB traces should be kept away from other high-speed signal traces. See “AN551: Crystal Selection Guide” for more details.

4.4.4. External Crystal Load Capacitors

The Si5350A provides the option of using internal and external crystal load capacitors. If external load capacitors are used, they should be placed as close to the XA/XB pads as possible. See “AN551: Crystal Selection Guide” for more details.

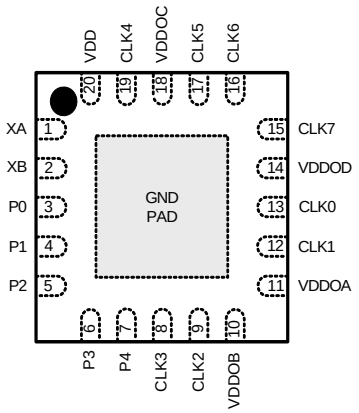
4.4.5. Unused Pins

Unused control pins (P0–P4) should be tied to GND.

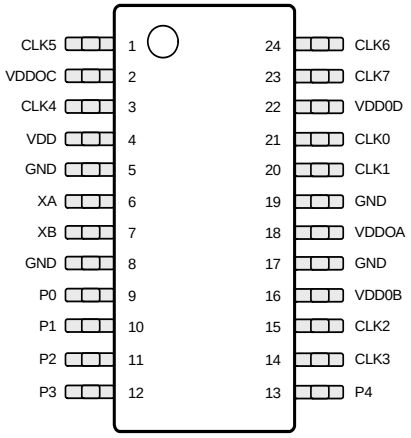
Unused output pins (CLK0–CLK7) should be left floating.

5. Pin Descriptions (20-Pin QFN, 24-Pin QSOP)

Si5350A 20-QFN
(Top View)



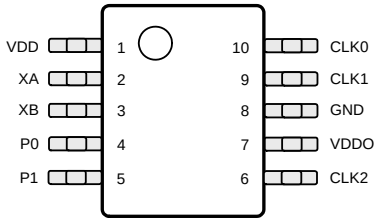
Si5350A 24-QSOP
(Top View)



Pin Name	Pin Number		Pin Type*	Function
	20-QFN	24-QSOP		
XA	1	6	I	Input pin for external XTAL
XB	2	7	I	Input pin for external XTAL
CLK0	13	21	O	Output clock 0
CLK1	12	20	O	Output clock 1
CLK2	9	15	O	Output clock 2
CLK3	8	14	O	Output clock 3
CLK4	19	3	O	Output clock 4
CLK5	17	1	O	Output clock 5
CLK6	16	24	O	Output clock 6
CLK7	15	23	O	Output clock 7
P0	3	9	I	User configurable input pin 0. See 4.4.5.
P1	4	10	I	User configurable input pin 1. See 4.4.5.
P2	5	11	I	User configurable input pin 2. See 4.4.5.
P3	6	12	I	User configurable input pin 3. See 4.4.5.
P4	7	13	I	User configurable input pin 4. See 4.4.5.
VDD	20	4	P	Core voltage supply pin. See 4.4.2
VDDOA	11	18	P	Output voltage supply pin for CLK0 and CLK1. See 4.4.2
VDDOB	10	16	P	Output voltage supply pin for CLK2 and CLK3. See 4.4.2
VDDOC	18	2	P	Output voltage supply pin for CLK4 and CLK5. See 4.4.2
VDDOD	14	22	P	Output voltage supply pin for CLK6 and CLK7. See 4.4.2
GND	Center Pad	5, 8, 17, 19	P	Ground
***Note:** I = Input, O = Output, P = Power				

6. Pin Descriptions (10-Pin MSOP)

Si5350A 10-MSOP
Top View



Pin Name	Pin Number	Pin Type*	Function
	10-MSOP		
XA	2	I	Input pin for external XTAL
XB	3	I	Input pin for external XTAL
CLK0	10	O	Output clock 0
CLK1	9	O	Output clock 1
CLK2	6	O	Output clock 2
P0	4	I	User configurable input pin 0
P1	5	I	User configurable input pin 1
VDD	1	P	Core voltage supply pin. See 4.4.2
VDDO	7	P	Output clock voltage supply pin for CLK0, CLK1, and CLK2. See 4.4.2
GND	8	P	Ground
***Note:** I = Input, O = Output, P = Power			

7. Package Outline (24-Pin QSOP)

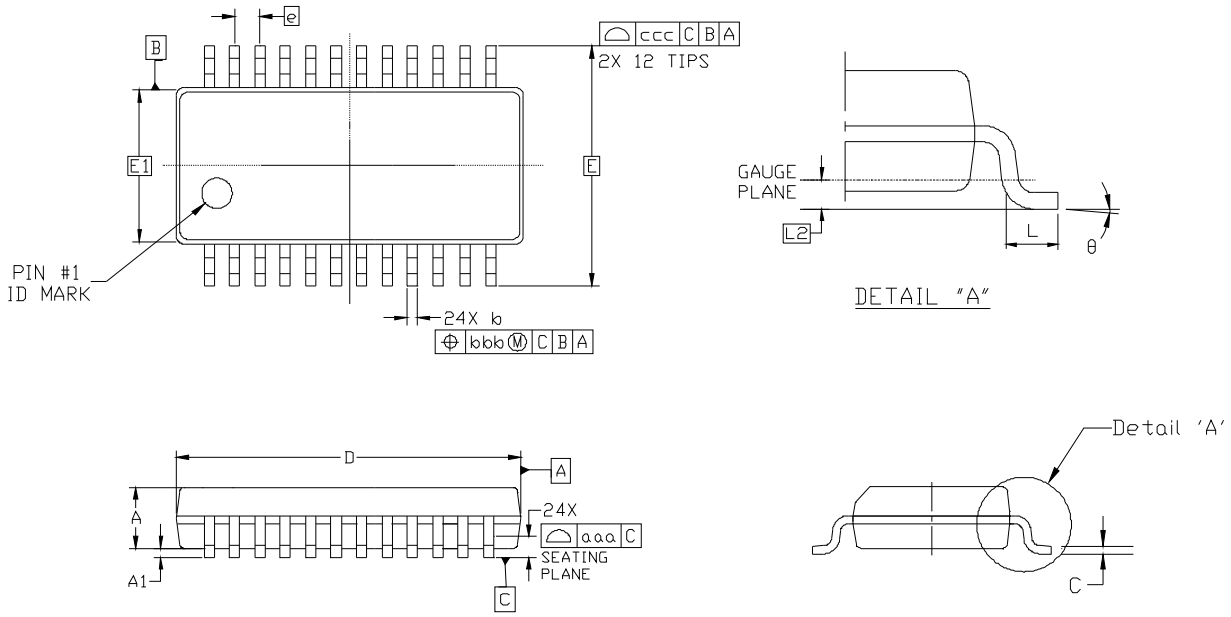


Table 10. 24-QSOP Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.19	—	0.30
c	0.15	—	0.25
D	8.55	8.65	8.75
E		6.00 BSC	
E1	3.81	3.90	3.99
e		0.635 BSC	
L	0.40	—	1.27
L2		0.25 BSC	
q	0	—	8
aaa		0.10	
bbb		0.17	
ccc		0.10	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation C
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8. Package Outline (20-Pin QFN)

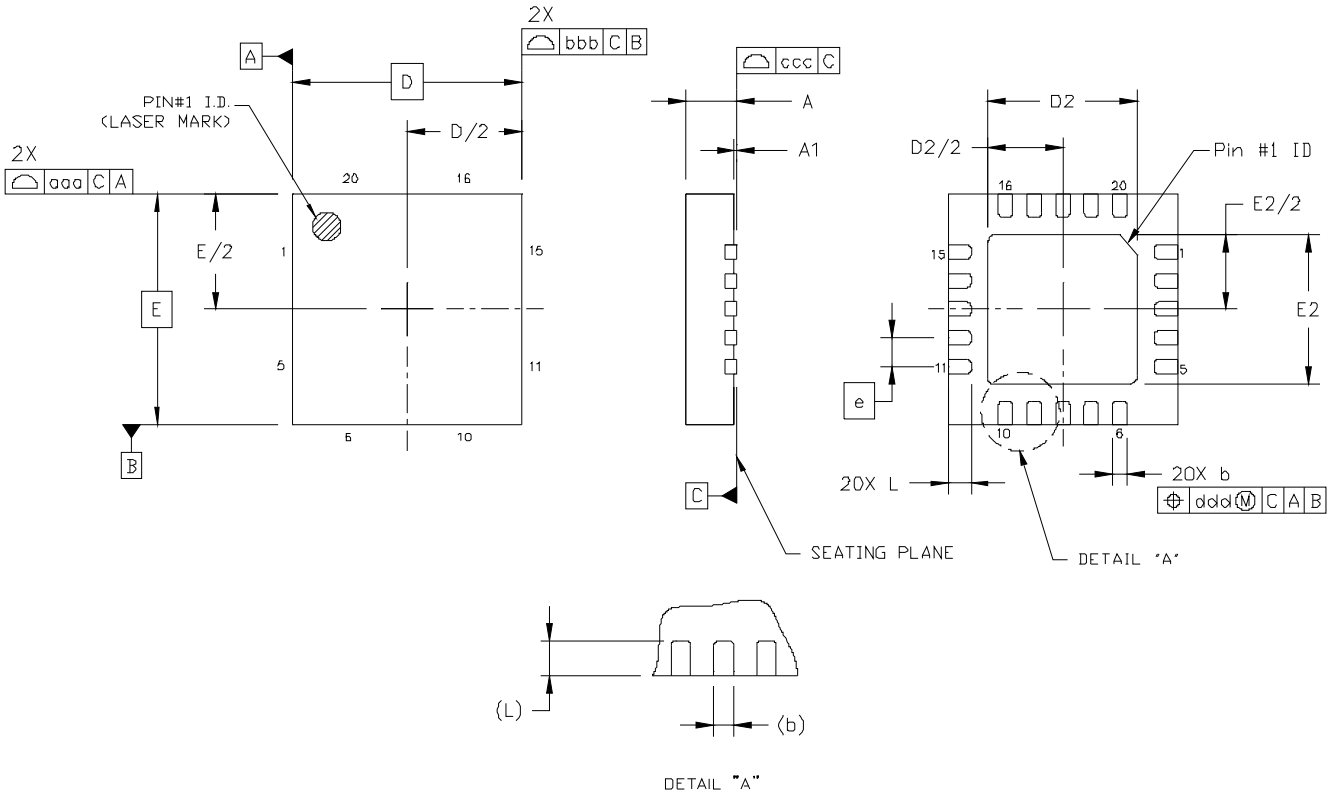


Table 11. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.65	2.70	2.75
e		0.50 BSC	
E		4.00 BSC	
E2	2.65	2.70	2.75
L	0.30	0.40	0.50
aaa			0.10
bbb			0.10
ccc			0.08
ddd			0.10
eee			0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9. Package Outline (10-Pin MSOP)

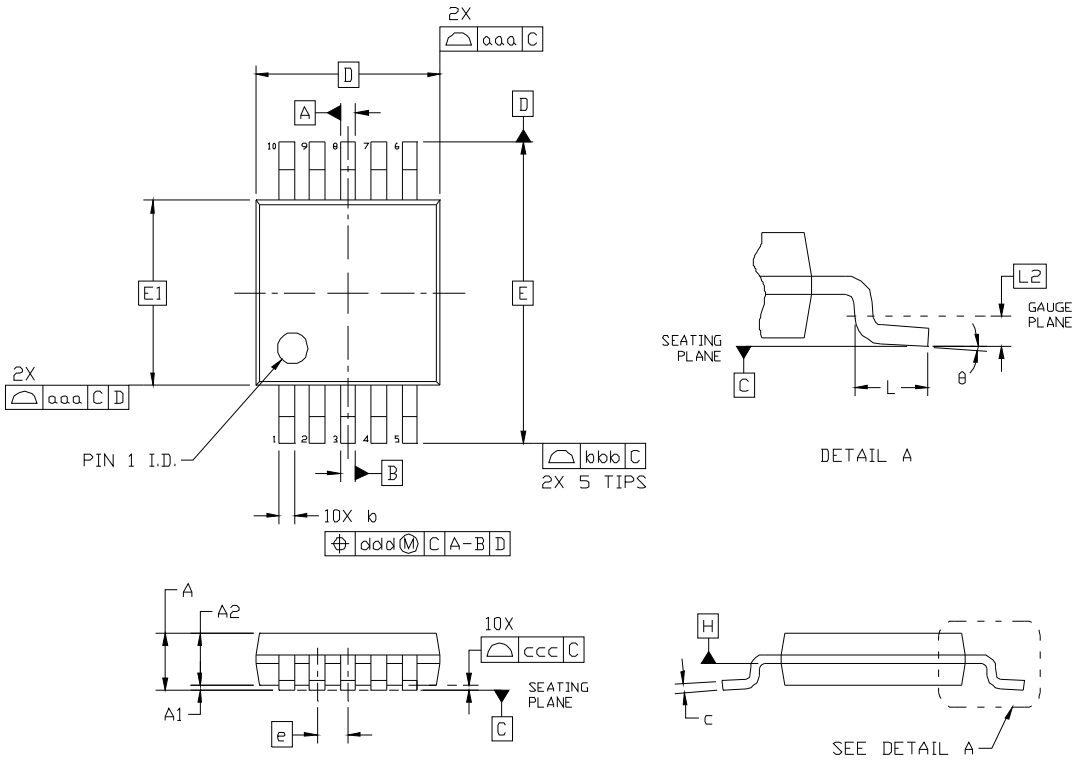


Table 12. 24-QSOP Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.10
A1	0.00	—	0.15
A2	0.75	0.85	0.95
b	0.17	—	0.33
c	0.08	—	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
e	0.50 BSC		
L	0.40	0.60	0.80
L2	0.25 BSC		
q	0	—	8
aaa	—	—	0.20
bbb	—	—	0.25
ccc	—	—	0.10
ddd	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation C
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10. Ordering Information

Factory programmed Si5350A devices can be requested using the ClockBuilder web-based utility available at: www.silabs.com/ClockBuilder. A unique part number is assigned to each custom configuration as indicated in Figure 8.

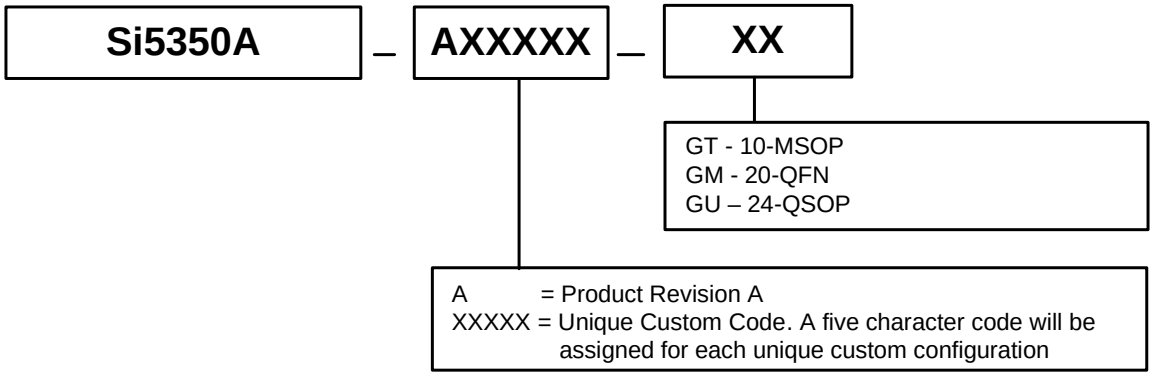


Figure 8. Custom Clock Part Numbers

A development kit containing ClockBuilder Desktop software and hardware allows easy customization of blank Si5350A devices with a user defined configuration. In addition to field programming, this development kit supports simplified device evaluation of any Si5350A device. The ordering part numbers for the development kits and blank Si5350A devices to be used for field programming are shown in Figure 9 and Figure 10, respectively.

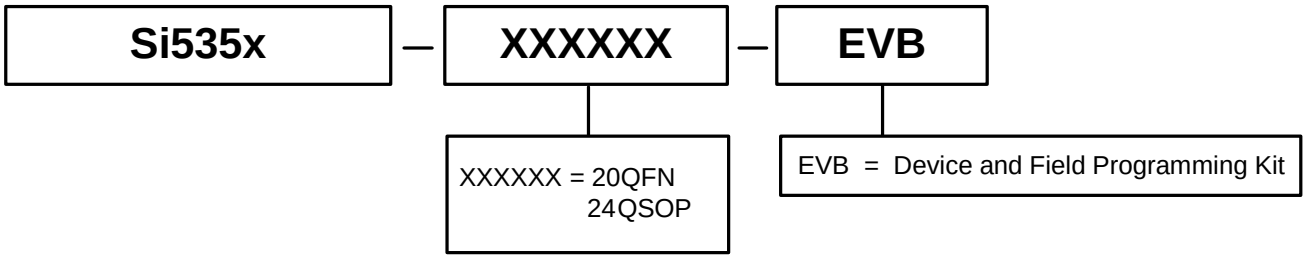


Figure 9. Development Kit Part Numbers

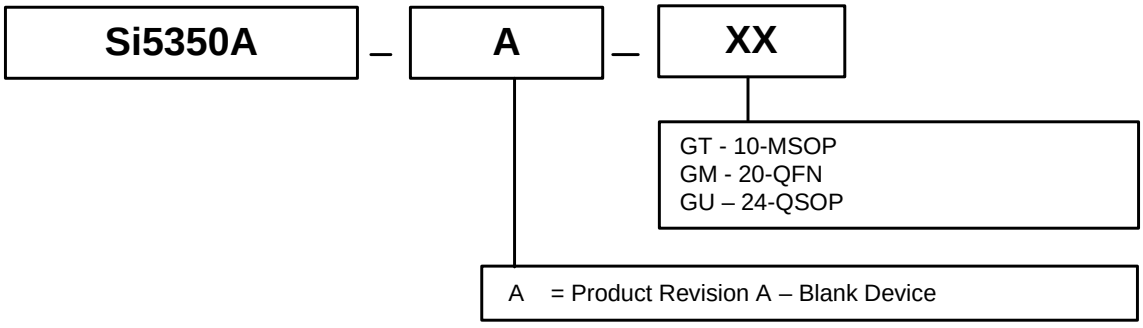


Figure 10. Blank Device Part Numbers

NOTES:

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