

P54/74PCT821A/B-P54/74PCT823A/B P54/74PCT825A/B BUS INTERFACE REGISTERS

PRELIMINARY

T-52-07

★ FEATURES

- Equivalent to Bipolar Am29821/23/25 Bipolar Registers
- Full CMOS Implementation
- Low Power Operation
- Fully TTL Compatible Input and Output Levels
- High Speed Parallel Registers with positive edge-triggered D-type Flip-Flops
- Buffered Common Clock Enable ($\overline{EN}$) and Asynchronous Clear Input ($\overline{CLR}$)
- $I_{OL} = 48\text{mA}$ (Commercial) and 32mA (Military)
- Clamp Diodes on all Inputs for Ringing Suppression
- Compact Pinout
 - 24-Pin 300 mil DIP, SOIC
 - 28-Pad 450 mil sq. LCC

★ DESCRIPTION

The P54/74PCT820 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The P54/74PCT821 is a buffered, 10 bit wide version of the popular '374 function. The P54/74PCT823 is a 9-bit wide buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$)—Ideal for parity bus interfacing in high-performance microprogrammed systems. The P54/74PCT825 is a 8-bit buffered register with all the 'PCT823 controls plus multiple enables ($\overline{OE}_1, \overline{OE}_2, \overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/WR. They are ideal for use as an output port requiring high I_{OL}/I_{OH} .

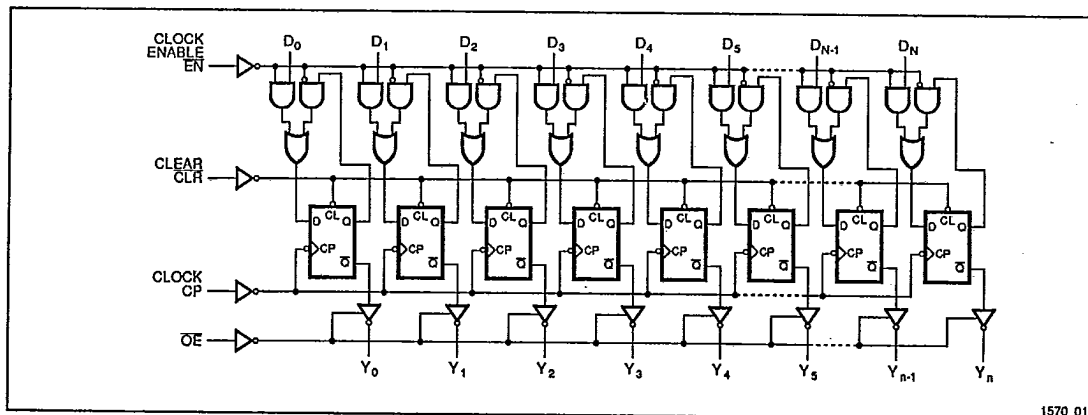
The P54/74PCT800 family of devices are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs.

All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

The P54/74PCT820 interface family is manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths giving 500 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

* For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V supply. For a fan-in/fan-out of 1, the internal gate delay is 200 picosecond at room temperature and 5.0V.

★ FUNCTIONAL BLOCK DIAGRAM



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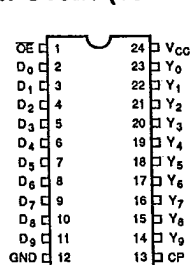
PRODUCT SELECTOR GUIDE

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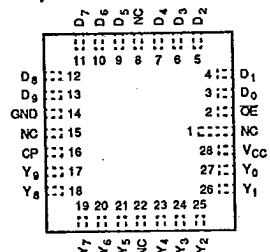
Non-Inverting	Device		
	10-Bit	9-Bit	8-Bit
	54/74PCT821A/B	54/74PCT823A/B	54/74PCT825A/B

PIN CONFIGURATIONS

P54/74PCT821 (10-Bit Register)

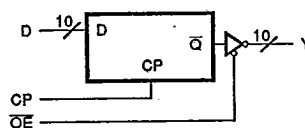


DIP (D4,P4) SOIC (S4)



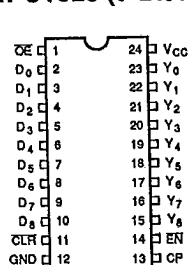
LCC (L5-1)

LOGIC SYMBOLS

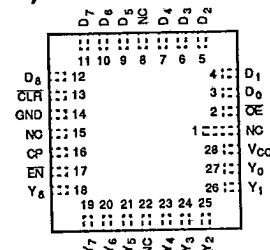


1570 02

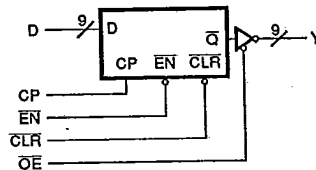
P54/74PCT823 (9-Bit Register)



DIP (D4,P4) SOIC (S4)

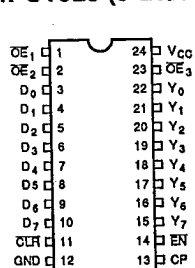


LCC (L5-1)

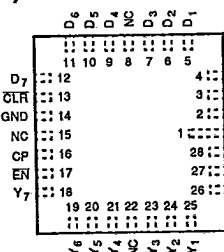


1570 03

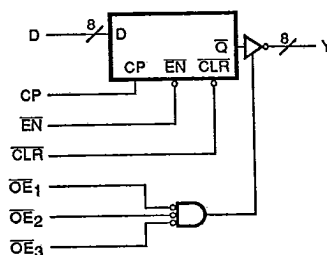
P54/74PCT825 (8-Bit Register)



DIP (D4,P4) SOIC (S4)



LCC (L5-1)



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P54/74PCT821A/B-P54/74PCT823A/B-P54/74PCT825A/B

ABSOLUTE MAXIMUM RATINGS^{1,2}

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	°C
T_A	Ambient Temperature Under Bias	-55 to +125	°C
V_{CC}	V_{CC} Potential to Ground	-0.5 to +7.0	V
I_{IN}	Input Current	-30 to +5.0	mA

Notes: 1570 Tbl 01
1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	100	mA
V_{IN}	Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	Voltage Applied to Output	-0.5 to $V_{CC} + 0.5$	V

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2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	-55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter	Min	Typ ¹	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0		$V_{CC} + 0.5$	V		
V_{IL}	Input LOW Voltage	-0.5		0.8	V		
V_H	Hysteresis		.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage			-1.2	V	MIN	$I_{IN} = -18mA$
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = 0.2V, \text{ or } V_{CC} - 0.2V$		$V_{CC} - 0.2$	V		$I_{OH} = -32\mu A$
		Military/Commercial (CMOS)		$V_{CC} - 0.2$	V	MIN	$I_{OH} = -300\mu A$
		Military (TTL)		2.4	V	MIN	$I_{OH} = -15mA$
		Commercial (TTL)		2.7	V	MIN	$I_{OH} = -24mA$
V_{OL}	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = 0.2V, \text{ or } V_{CC} - 0.2V$		0.2	V		$I_{OL} = 300\mu A$
		Military/Commercial (CMOS)		0.2	V	MIN	$I_{OL} = 300\mu A$
		Military (TTL)		0.5	V	MIN	$I_{OL} = 32mA$
		Commercial (TTL)		0.5	V	MIN	$I_{OL} = 48mA$
I_{IH}	Input HIGH Current			5	μA	MAX	$V_{IN} = V_{CC}$
I_{IL}	Input LOW Current			-5	μA	MAX	$V_{IN} = GND$
I_{IH}	Input HIGH Current ³			5	μA	MAX	$V_{IN} = 2.7V$
I_{IL}	Input LOW Current ³			-5	μA	MAX	$V_{IN} = 0.5V$
I_{OZH}	Off State I_{OUT} HIGH-Level Voltage Applied			10	μA	MAX	$V_{OUT} = V_{CC}$
I_{OZL}	Off State I_{OUT} LOW-Level Voltage Applied			-10	μA	MAX	$V_{OUT} = GND$
I_{OZH}	Off State I_{OUT} HIGH-Level Voltage Applied ³			10	μA	MAX	$V_{OUT} = 2.7V$
I_{OZL}	Off State I_{OUT} LOW-Level Voltage Applied ³			-10	μA	MAX	$V_{OUT} = 0.5V$
I_{OS}	Output Short Circuit Current ²	-75			mA	MAX	$V_{OUT} = 0.0V$
C_{IN}	Input Capacitance ³		5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance ³		9	12	pF	MAX	All outputs

Notes:
1. Typical limits are at $V_{CC} = 5.0V, T_A = +25^\circ C$ ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

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DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ ¹	Max	Units	Conditions
I_{CCOC}	Quiescent Power Supply Current (CMOS inputs) Com'l. Mil.	.003 .003	0.3 0.5	mA mA	$V_{CC} = \text{MAX}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, $f = 0$, Outputs Open
I_{CCOT}	Quiescent Power Supply Current (TTL inputs)		2.0	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 3.4V^2$, $f = 0$, Outputs Open
I_{CCD}	Dynamic Power Supply Current ³		0.25	mA/ mHz	$V_{CC} = \text{MAX}$, One Bit Toggling, 50% Duty Cycle, $\overline{OE} = \text{GND}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, Outputs Open
I_{CC}	Total Power Supply Current ⁵		4.0	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_i = 5\text{MHz}$, $\overline{OE} = \text{GND}$ and $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			6.0	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_i = 5\text{MHz}$, $\overline{OE} = \text{GND}$ and $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$
			7.8 ⁴	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_i = 2.5\text{MHz}$, $\overline{OE} = \text{GND}$ and $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			16.8 ⁴	mA	$V_{CC} = \text{MAX}$, $f_0 = 10\text{MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_i = 2.5\text{MHz}$, $\overline{OE} = \text{GND}$ and $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$

Notes:

- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient and maximum loading.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_{CC} = I_{CCOC} + I_{CCOT} D_H N_I + I_{CCD} (f_0/2 + f_i N_i)$
 I_{CCOC} = Quiescent Current with CMOS input levels

 I_{CCOT} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

 D_H = Duty Cycle for TTL Inputs High

 N_I = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

 f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)

 f_i = Input Frequency

 N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

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AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	P54/74PCT821A/823A/825A				P54/74PCT821B/823B/825B				Units	Fig. No.
			MIL		COM'L		MIL		COM'L			
			Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Y_1 ($\overline{OE} = \text{LOW}$)	$C_L = 50\text{pF}$ $R_L = 500\Omega$	—	12.0	—	12.0	—	8.5	—	7.5	ns	1, 5
			—	12.0	—	12.0	—	8.5	—	7.5	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to Y_1 ($\overline{OE} = \text{LOW}$)	$C_L = 300\text{pF}^2$ $R_L = 500\Omega$	—	20.0	—	20.0	—	16.0	—	15.0	ns	1, 5
			—	20.0	—	20.0	—	16.0	—	15.0	ns	
t_{PLH}	Propagation Delay Clear to Y_1	$C_L = 50\text{pF}$ $R_L = 500\Omega$	—	20.0	—	20.0	—	9.5	—	9.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to $Y_1 \uparrow$	$C_L = 50\text{pF}$ $R_L = 500\Omega$	—	15.0	—	14.0	—	9.0	—	8.0	ns	1, 7, 8
			—	15.0	—	14.0	—	9.0	—	8.0	ns	
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to $Y_1 \uparrow$	$C_L = 300\text{pF}^2$ $R_L = 500\Omega$	—	25.0	—	23.0	—	16.0	—	15.0	ns	1, 7, 8
			—	25.0	—	23.0	—	16.0	—	15.0	ns	
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to $Y_1 \uparrow$	$C_L = 5\text{pF}^2$ $R_L = 500\Omega$	—	10.0	—	9.0	—	7.0	—	6.5	ns	1, 7, 8
			—	10.0	—	9.0	—	7.0	—	6.5	ns	
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to $Y_1 \uparrow$	$C_L = 50\text{pF}$ $R_L = 500\Omega$	—	18.0	—	16.0	—	8.0	—	7.5	ns	1, 7, 8
			—	18.0	—	16.0	—	8.0	—	7.5	ns	

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AC OPERATING REQUIREMENTS

Symbol	Parameter	Test Conditions	P54/74PCT821A/823A/825A				P54/74PCT821B/823B/825B				Units	Fig. No.
			MIL		COM'L		MIL		COM'L			
			Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.	Min. ¹	Max.		
t _{su}	Data to CP Set-up Time	C _L = 50pF R _L = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	ns	4
t _h	Data CP Hold Time		2.0	—	2.0	—	1.5	—	1.5	—	ns	4
t _{su}	Enable (EN ↑) to CP Set-up Time		4.0	—	4.0	—	3.0	—	3.0	—	ns	9
t _h	Enable EN Hold Time		2.0	—	2.0	—	0.0	—	0.0	—	ns	9
t _{rec}	Clear Recovery (CLR ↑) Time		7.0	—	7.0	—	6.0	—	6.0	—	ns	6
t _w (H) t _w (L)	Clock Pulse Width HIGH or LOW		7.0 7.0	— —	7.0 7.0	— —	6.0 6.0	— —	6.0 6.0	— —	ns ns	5
t _w (L)	Clear (CLR = LOW) Pulse Width		7.0	—	7.0	—	6.0	—	6.0	—	ns	5

Notes:

1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. These parameters are guaranteed but not tested.

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★ PIN DESCRIPTION

Name	I/O	Description
D ₁	I	The D flip-flop data inputs.
CLR	I	For both inverting and non-inverting registers, when the clear input is LOW and OE is LOW, the Q ₁ outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	O	Clock Pulse for the register; enters data into the register on the LOW-to-HIGH transition.
Y ₁ , Y ₂	O	The register three-state outputs.
EN	I	Clock Enable. When the clock enable is LOW, data on the D ₁ input is transferred to the Q ₁ output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q ₁ outputs do not change state, regardless of the data or clock input transitions.
OE	I	Output Control. When the OE input is HIGH, the Y ₁ outputs are in the high impedance state. When the OE input is LOW, the TRUE register data is present at the Y ₁ outputs.

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FUNCTION TABLES P54/74PCT821/23/25

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Inputs					Internal Outputs		Function
OE	CLR	EN	D ₁	CP	Q ₁	Y ₁	
H	X	L	L	↑	L	Z	High Z
H	X	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

H = HIGH, L = LOW, X = Don't Care, NC = No Change, 1570 Tbl 10
↑ = LOW-to-HIGH Transition, Z = HIGH Impedance

ORDERING INFORMATION

PxxPCT	xxxx	x	x	x	
Temp. Class	Device type	Package	Temperature	Processing	
				B	MIL-STD-883, Class B
				C	0°C to +70°C
				M	-55°C to +125°C
				P	Plastic DIP
				D	CERDIP
				S	Small Outline IC
				L	Leadless Chip Carrier
				821A	10-Bit Non-Inverting Register
				821B	Fast 10-Bit Non-Inverting Register
				823A	9-Bit Non-Inverting Register
				823B	Fast 9-Bit Non-Inverting Register
				825A	8-Bit Non-Inverting Register
				825B	Fast 8-Bit Non-Inverting Register
				74	Commercial
				54	Military

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TECHDOC 1570