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FAST Products	

FAST 74F1764/1765 74F1764-1/1765-1 1 Megabit DRAM Dual-Ported Controllers

FEATURES

- Allows two microprocessors to access the same bank of dynamic RAM
- Performs arbitration, signal timing, address multiplexing and refresh
- 10 address output pins allow direct control of up to 1Mbit dynamic RAMs
- External address multiplexing enables control of 4Mbit (or greater) dynamic RAMs
- Separate refresh clock allows adjustable refresh timing
- 74F1764/F1764-1 have on-chip 20-bit address input latch
- Allows control of dynamic RAMs with row access times down to 40ns
- 74F1764/F1765 output drivers designed for incident wave switching
- 74F1764-1/F1765-1 output drivers designed for first reflected wave switching

DESCRIPTION

The 74F1764/1765 DRAM Dual-ported Controller is a high speed synchronous dual-port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing device to share the same block of DRAM. The device performs arbitration, signal timing, address multiplexing, and refresh address generation, replacing up to 25 discrete devices.

74F1764 vs 74F1765

The 74F1764 though functionally and pin to pin compatible with the 74F1765 differs from the later in that it has an on-chip address input latch. This is useful in systems that have unlatched or multiplexed address and data bus.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1764/1765	150MHz	150mA
74F1764-1/1765-1	150MHz	125mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
48-Pin Plastic DIP	N74F1764N, N74F1765N, N74F1764-1N, N74F1765-1N
44-Pin PLCC	N74F1764A, N74F1765A, N74F1764-1A, N74F1765-1A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$RA_0 - RA_9$	Row address inputs	1.0/1.0	20 μ A/0.6mA
$CA_0 - CA_9$	Column address inputs	1.0/1.0	20 μ A/0.6mA
$\overline{REQ}_1, \overline{REQ}_2$	Memory access request inputs	1.0/1.0	20 μ A/0.6mA
CP	Clock input	1.0/1.0	20 μ A/0.6mA
RCP	Refresh clock input	1.0/1.0	20 μ A/0.6mA
$\overline{SEL}_1, \overline{SEL}_2$	Select outputs	'F1764/1765 750/40	15.0mA/24mA
		'F1764-1/1765-1 1000/13.3	20.0mA/8mA
$MA_0 - MA_9$	Memory address outputs	'F1764/1765 750/40	15.0mA/24mA
		'F1764-1/1765-1 1000/13.3	20.0mA/8mA
GNT	Grant output	'F1764/1765 750/40	15.0mA/24mA
		'F1764-1/1765-1 1000/13.3	20.0mA/8mA
$\overline{RAS}$	Row address strobe output	'F1764/1765 750/40	15.0mA/24mA
		'F1764-1/1765-1 1000/13.3	20.0mA/8mA
WG	Write gate output	'F1764/1765 750/40	15.0mA/24mA
		'F1764-1/1765-1 1000/13.3	20.0mA/8mA
$\overline{CASEN}$	Column address strobe enable output	'F1764/1765 750/40	15.0mA/24mA
		'F1764-1/1765-1 1000/13.3	20.0mA/8mA
DTACK	Data transfer acknowledge output	'F1764/1765 750/40	15.0mA/24mA
		'F1764-1/1765-1 1000/13.3	20.0mA/8mA

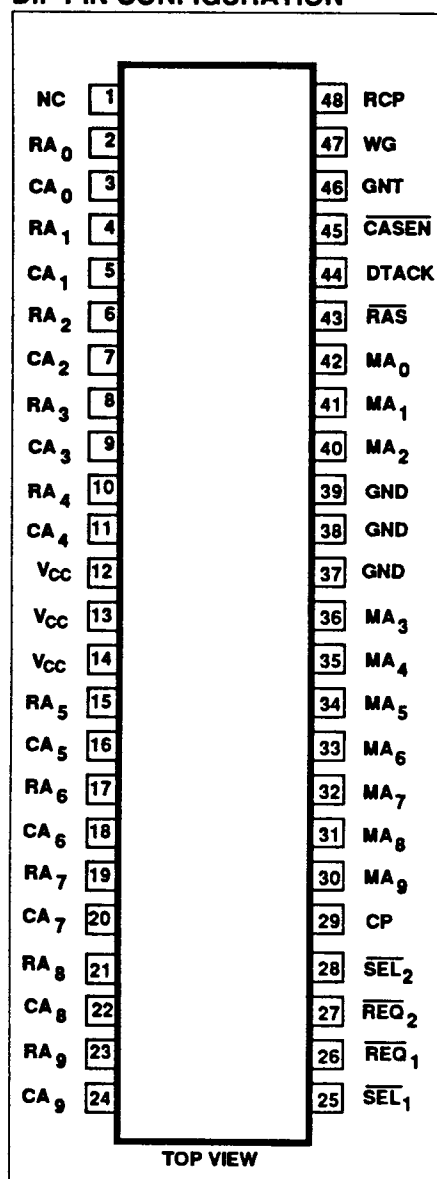
NOTE:

1.One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state

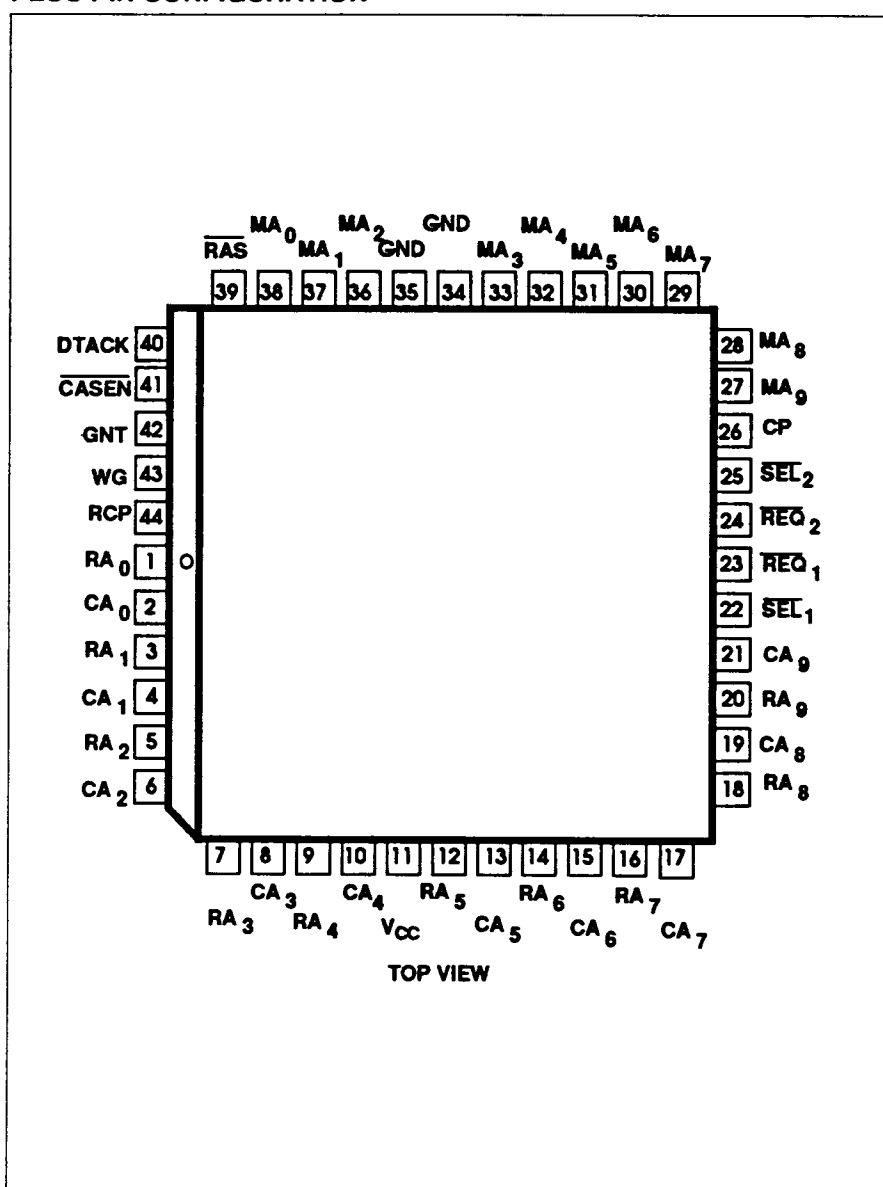
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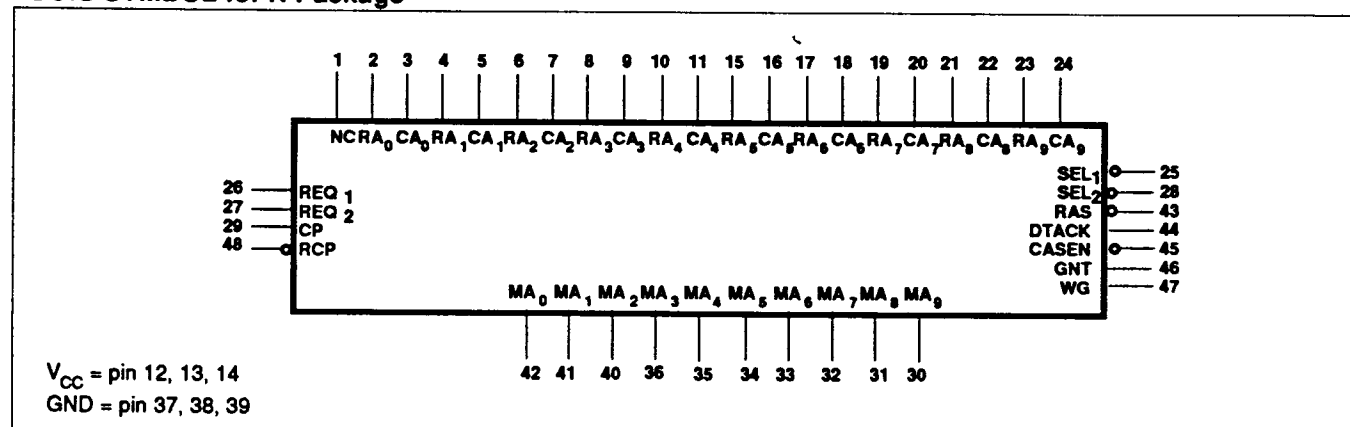
DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION



LOGIC SYMBOL for N Package



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PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
RA ₀	2	1	Inputs	Address inputs used to generate memory row address
RA ₁	4	3		
RA ₂	6	5		
RA ₃	8	7		
RA ₄	10	9		
RA ₅	15	12		
RA ₆	17	14		
RA ₇	19	16		
RA ₈	21	18		
RA ₉	23	20		
CA ₀	3	2	Inputs	Address inputs used to generate memory column address
CA ₁	5	4		
CA ₂	7	6		
CA ₃	9	8		
CA ₄	11	10		
CA ₅	16	13		
CA ₆	18	15		
CA ₇	20	17		
CA ₈	22	19		
CA ₉	24	21		
REQ ₁	26	23	Input	Memory access request from Microprocessor 1
REQ ₂	27	24	Input	Memory access request from Microprocessor 2
CP	29	26	Input	Clock input which determines the master timing
RCP	48	44	Input	Refresh clock determines the period of refresh for each row after it is internally divided by 64
SEL ₁	25	22	output	Select signal is activated in response to active REQ ₁ input indicating selection of Microprocessor 1
SEL ₂	28	25	output	Select signal is activated in response to active REQ ₂ input indicating selection of Microprocessor 2
MA ₀	42	38	Outputs	Memory address outputs designed to drive address lines of the DRAM
MA ₁	41	37		
MA ₂	40	36		
MA ₃	36	33		
MA ₄	35	32		
MA ₅	34	31		
MA ₆	33	30		
MA ₇	32	29		
MA ₈	31	28		
MA ₉	30	27		
GNT	46	42	Output	Grant output, activated upon start of a memory access cycle
RAS	43	39	Output	Row address strobe, used to latch the row address into the bank of DRAM (to be connected directly to the RAS inputs of the DRAMs)
WG	47	43	Output	Write Gate may be gated with the microprocessor's write strobe to perform an early write cycle
CASEN	45	41	Output	Column address Strobe Address Enable is used to latch the column address into the bank of DRAMs
DTACK	44	40	Output	Data Transfer Acknowledge indicates that the data on the DRAM output lines is valid or the proper access time has been met

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ARCHITECTURE

The 74F1764/1765 1 Megabit DRAM dual-ported controller is a synchronous device, with all signal generation being a function of the input clock (CP).

The 'F1764/1765 arbitration logic is divided into two stages. The first stage controls which one of the two REQ inputs will be serviced by activating the corresponding SEL output. This arbitration takes place irrespective of whether or not a refresh cycle is in progress. The arbitration is accomplished by sampling the REQ₁ and REQ₂ inputs on different edges of the CP clock. REQ₁ is sampled on the rising edge and REQ₂ on the falling edge (refer to Figure 1 and 2).

Therefore, if access to the DRAM is requested by both processors at the same time, the contention is automatically resolved. The internal flip-flops of the device used in the arbitration process have been chosen for their immunity to metastable conditions.

The second stage of arbitration selects between the selected processor and any internal refresh request. Refresh always has priority and is serviced immediately after the current cycle is completed (if needed). This arbitration stage also indicates the start of an access cycle by asserting the GNT output.

The Refresh Clock (RCP) input determines the period for each row. This clock may be held in the High state for external or no refresh applications. When used, a refresh request is internally generated

every 64 RCP cycles. The refresh counter is incremented at the end of every refresh cycle, and provides the refresh address.

Since SEL outputs indicate which one of the two memory accessing devices has been selected to be serviced, these provide an indication of which processor's address bus should be asserted at the controller address inputs. A Data Transfer Acknowledge (DTACK) signal is generated by the timing logic and either this signal or GNT may be used with the SEL outputs to indicate the end or beginning of an access cycle for each processor.

FUNCTIONAL DESCRIPTION

As described earlier, the timing, arbitration, refresh and multiplexing functions provided by the controller are all derived from the CP input. The period of this clock should be set equal to:

$(t_{ras} \text{ (of the DRAM)} + 16.5) / 4$ plus any system guard-band required.

For the 74F1764-1/1765-1 the CP clock input period should be equal to:

$(T_{ras} \text{ (of the DRAM)} + 22.10) / 4$ plus any system guard-band required.

A microprocessor requests access to the DRAM by activating the appropriate REQ input. If a refresh cycle is not in process and the other request input is not active, the SEL output corresponding to the active REQ input will be asserted to indicate the selected processor. The GNT output then goes High to indicate the start of a memory access cycle. If however, a re-

fresh cycle is in process, and there is only one active REQ input, the SEL output corresponding to the active input REQ will be asserted but the GNT output will not go High until the completion of the refresh cycle (see Figures 8 and 9).

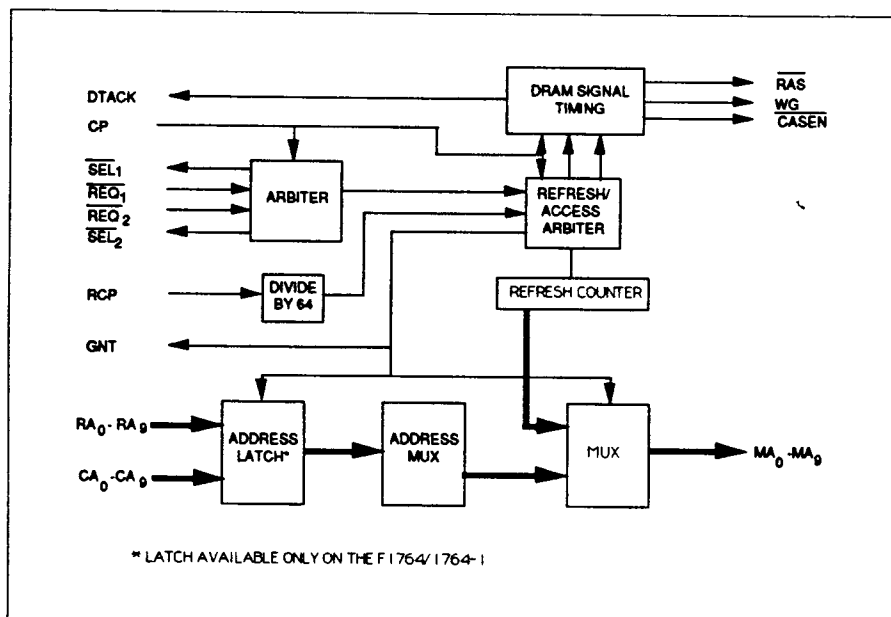
When the device is servicing a memory access cycle and a memory access is also requested by the other processor before the current cycle is completed, the SEL output for the other processor will not be issued, though GNT is asserted at that time, because the other processor is performing an access cycle. This will insure that there is no contention on the address bus, i.e., the address bus is not driven by both processors at the same time.

Following the completion of the current memory access cycle, the SEL output corresponding to the awaiting REQ input will be asserted, followed by the GNT output. If, however, there are any pending refresh requests, assertion of the GNT output will be held OFF until the refresh has been serviced.

When GNT goes High, the RA₀-RA₉ and CA₀-CA₉ address input to the 'F1764/'F1764-1 are latched internally and the RA₀-RA₉ signals are propagated to the MA₀-MA₉ outputs. The address inputs are not latched by the 74F1765/'F1765-1 and therefore, RA₀-RA₉ inputs propagate directly to the MA₀-MA₉ outputs.

A half-clock cycle is allowed for the address signals to propagate through to the outputs, after which the RAS output is asserted.

BLOCK DIAGRAM



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74F1764-1, 74F1765-1

One clock cycle later, the CA_0 - CA_9 latch outputs on the 'F1764 and 'F1764-1 or CA_0 - CA_9 inputs to the 'F1765 and 'F1765-1 are selected and propagated to the MA_0 - MA_9 outputs. The Write Gate (WG) output becomes valid at this time to indicate the proper time to gate the Write signal from the selected processor to the DRAM to perform an Early Write cycle.

A half-clock cycle is again allowed for the CA_0 - CA_9 signals to propagate and stabilize. $\overline{CASEN}$ then becomes valid. $\overline{CASEN}$ can be used as $\overline{CAS}$ output or decoded with higher order address signals to produce multiple $\overline{CAS}$ signals. After $\overline{CASEN}$

is valid, the controller will wait for 2 and one-half clock cycles before negating $\overline{RAS}$, making a total $\overline{RAS}$ pulse width of approximately 4 clock cycles. Since this width matches the standard DRAM access time, the controller next asserts DTACK output, indicating that valid data is on the DRAM data lines or that a memory access cycle is complete. DTACK may be used to assert valid data transfer acknowledge for processors requiring this signal (i.e., the 68000 family of processors).

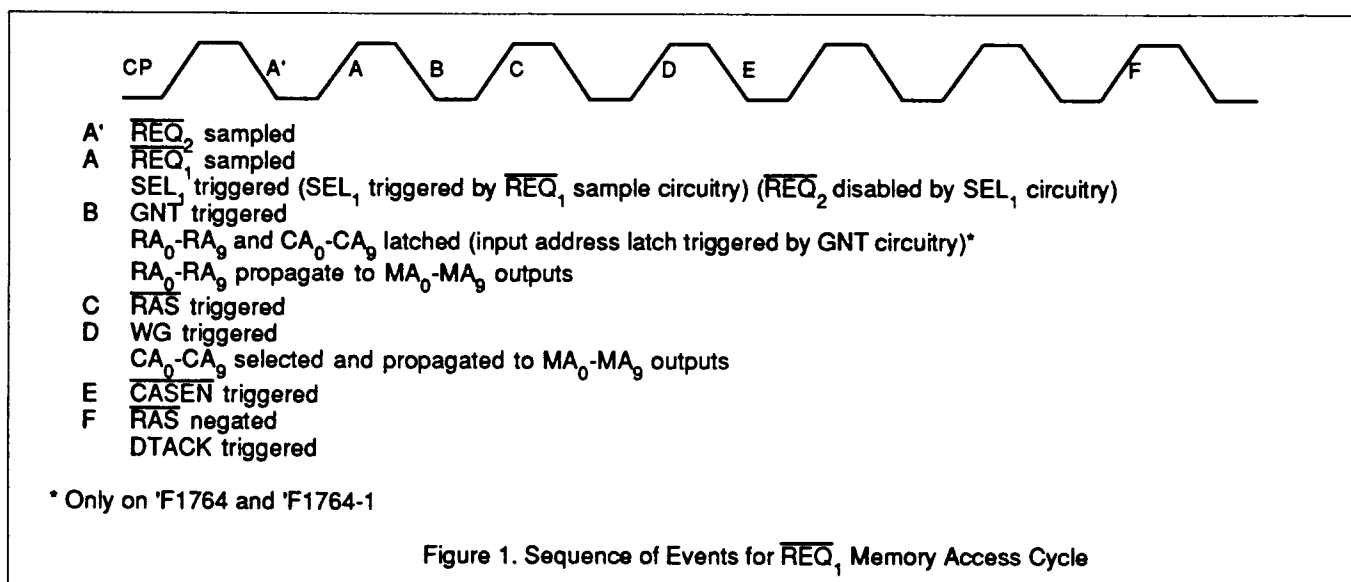
All controller output signals are held in this final state until the selected processor

withdraws its request by driving its $\overline{REQ}$ input High.

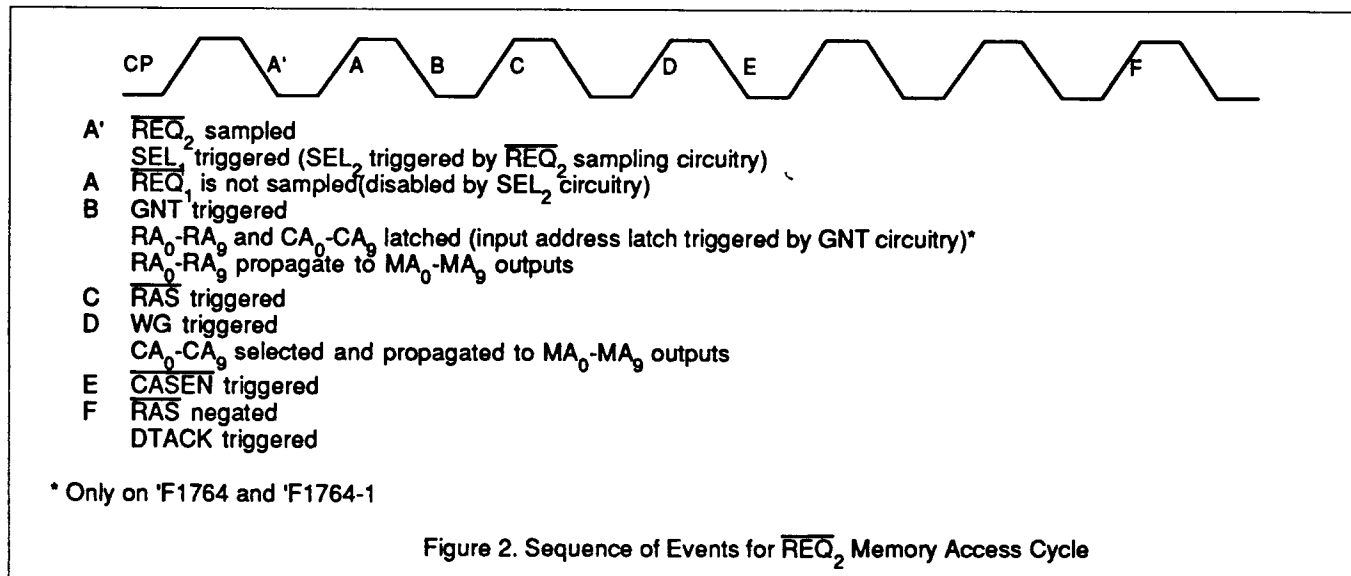
When the request is withdrawn, internal synchronization takes place, the controller output signals become inactive, and any pending memory access or refresh cycles are serviced.

A refresh cycle is serviced by propagating the 10 refresh counter address signals to the MA_0 - MA_9 outputs. After a half-clock cycle the $\overline{RAS}$ output is asserted for four cycles and then negated for three clock cycles to meet the $\overline{RAS}$ precharge requirements of the DRAMS (see Figures 3 and 4).

TIMING SEQUENCE



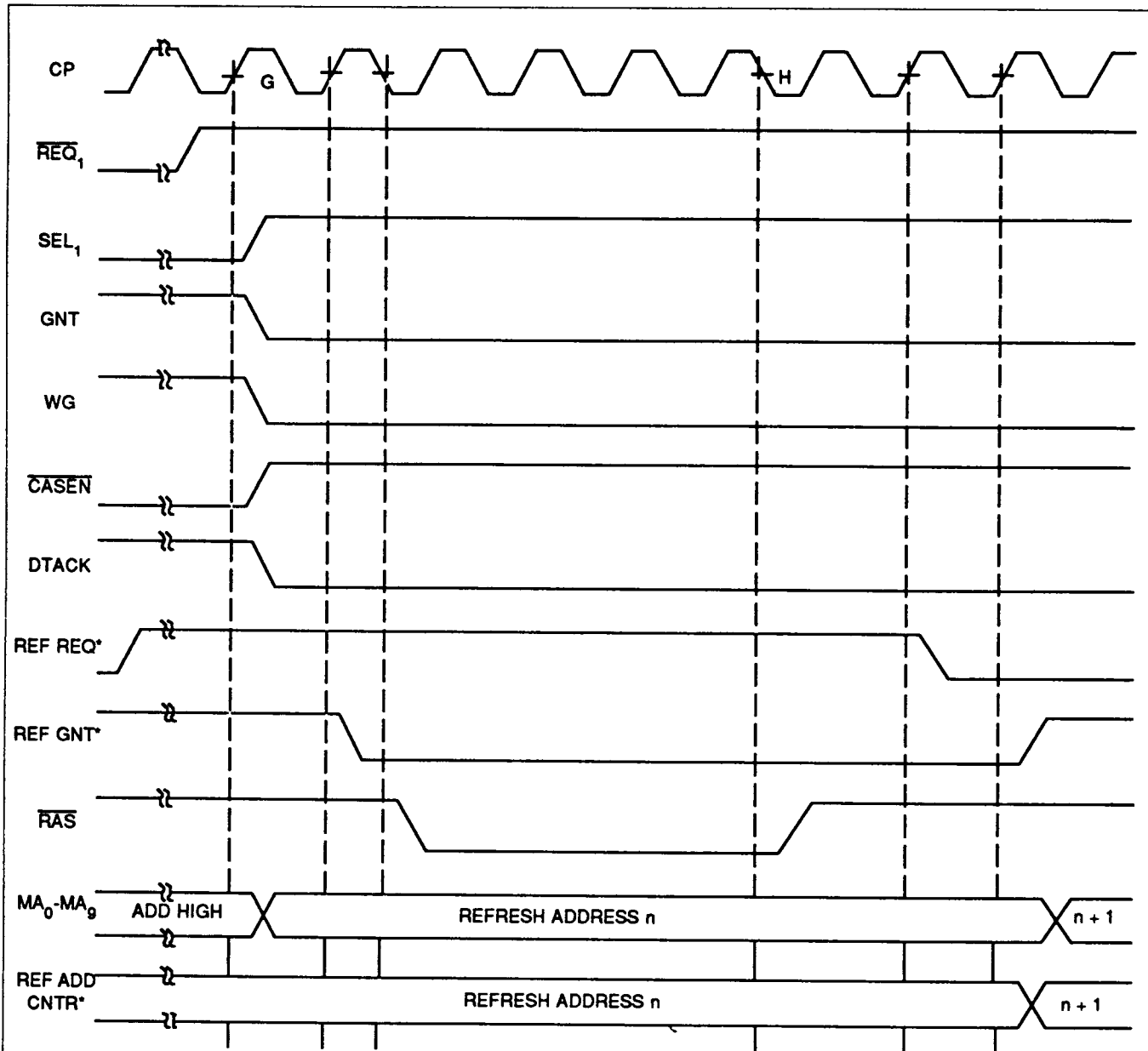
TIMING SEQUENCE



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TIMING DIAGRAM



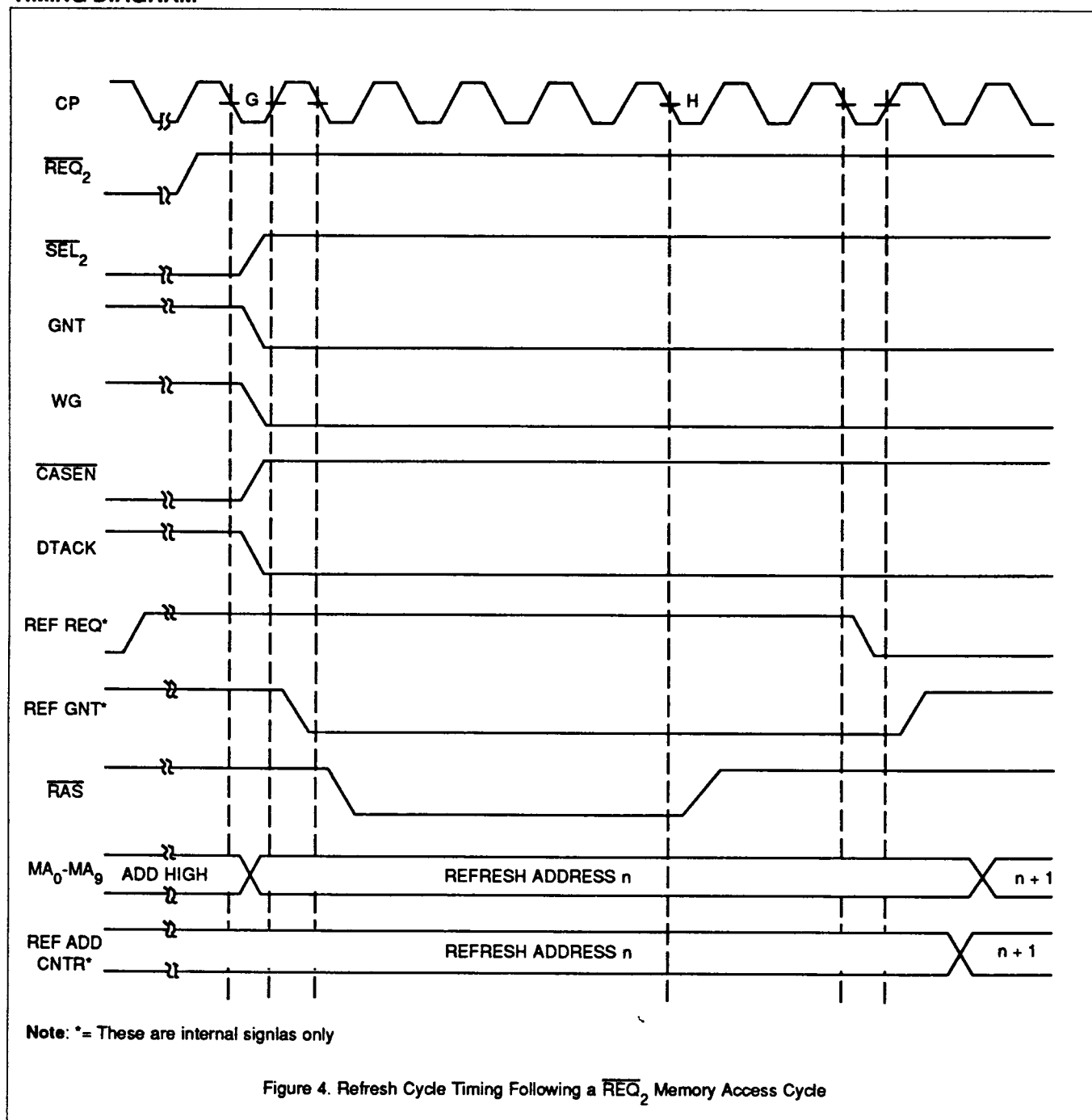
Note: * = These are internal signals only

Figure 3. Refresh Cycle Timing Following a $\overline{REQ}_1$ Memory Access Cycle

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74F1764-1, 74F1765-1

TIMING DIAGRAM



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Using 74F1764/1765 AND 74F1764-1/1765-1 TO ADDRESS 4MBIT DRAMS

The addressing capabilities of the 1 Megabit DRAM dual-ported controllers can be extended to address 4Mbit (or greater) DRAMs by using an external multiplexer to multiplex additional address bits.

Figure 5 shows an application, using an external 2-to-1 multiplexer to address

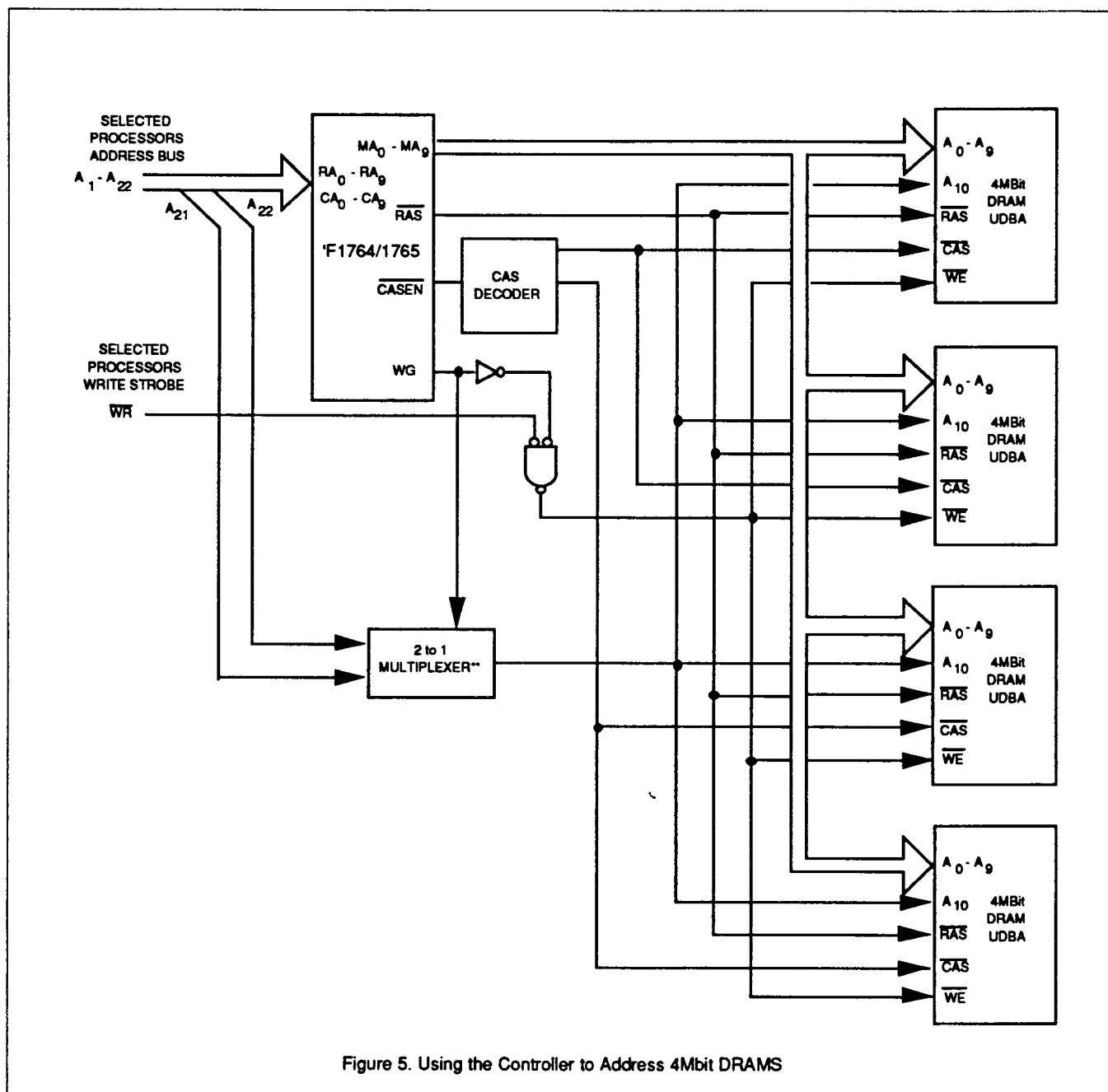
4Mbit dynamic RAMs. The 10-bit internal refresh counter of the controller provides 1024 row addresses which more than meet the refreshing needs for most industry standard 4Mbit DRAMs. Therefore, it is unnecessary to provide for any additional refresh address bits for DRAMs with up to 1024 rows.

Additional address bits (for larger DRAMs) may also be multiplexed

externally as long as the DRAM refreshing requirements do not exceed 1024 row addresses.

The WG output of the controller should be used to multiplex between the external row and column addresses. However, it is important that the propagation delay through the external multiplexer does not cause column address setup violations on the dynamic RAM.

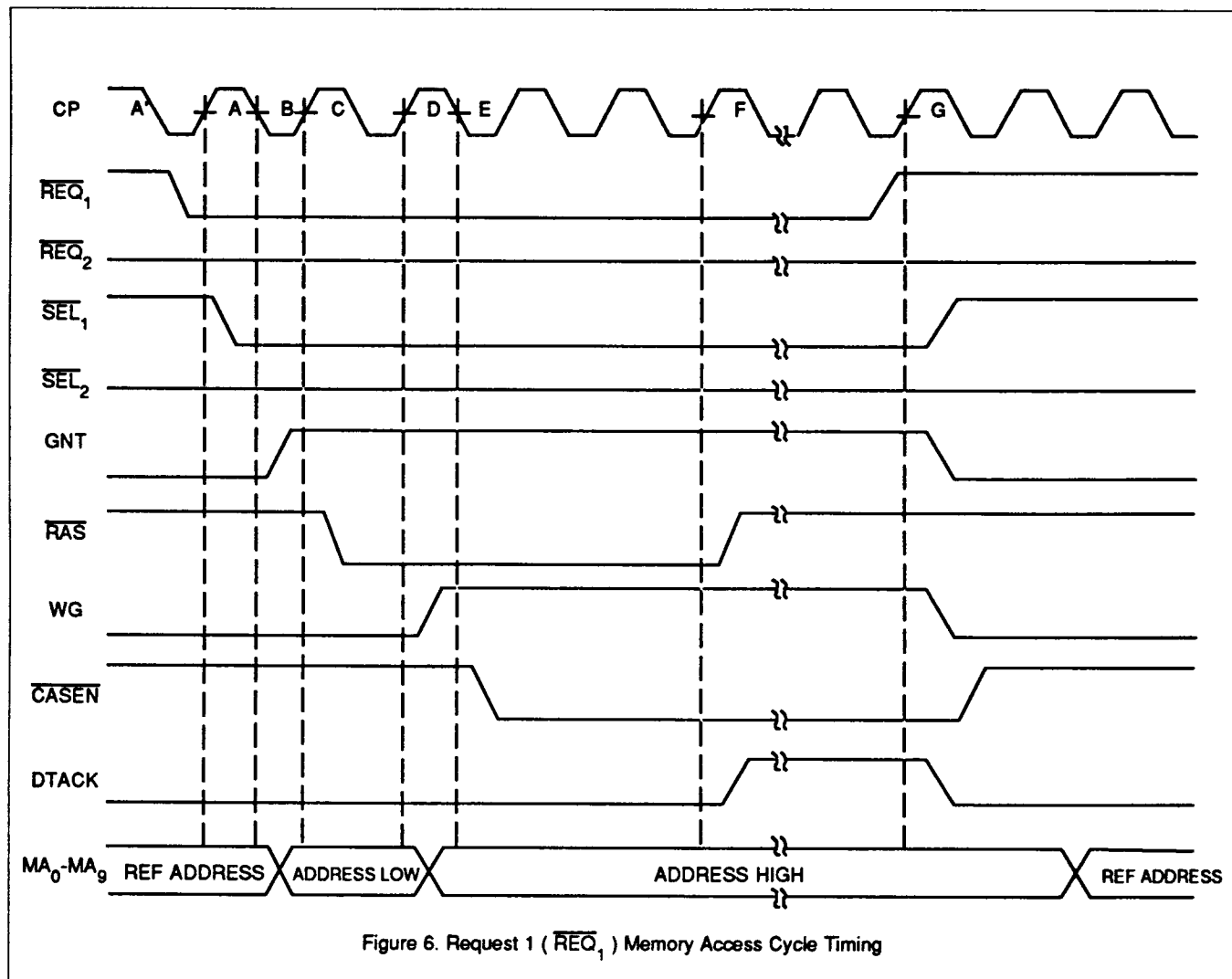
APPLICATION



1 Megabit DRAM Dual-Ported Controllers

FAST 74F1764, 74F1765,
74F1764-1, 74F1765-1

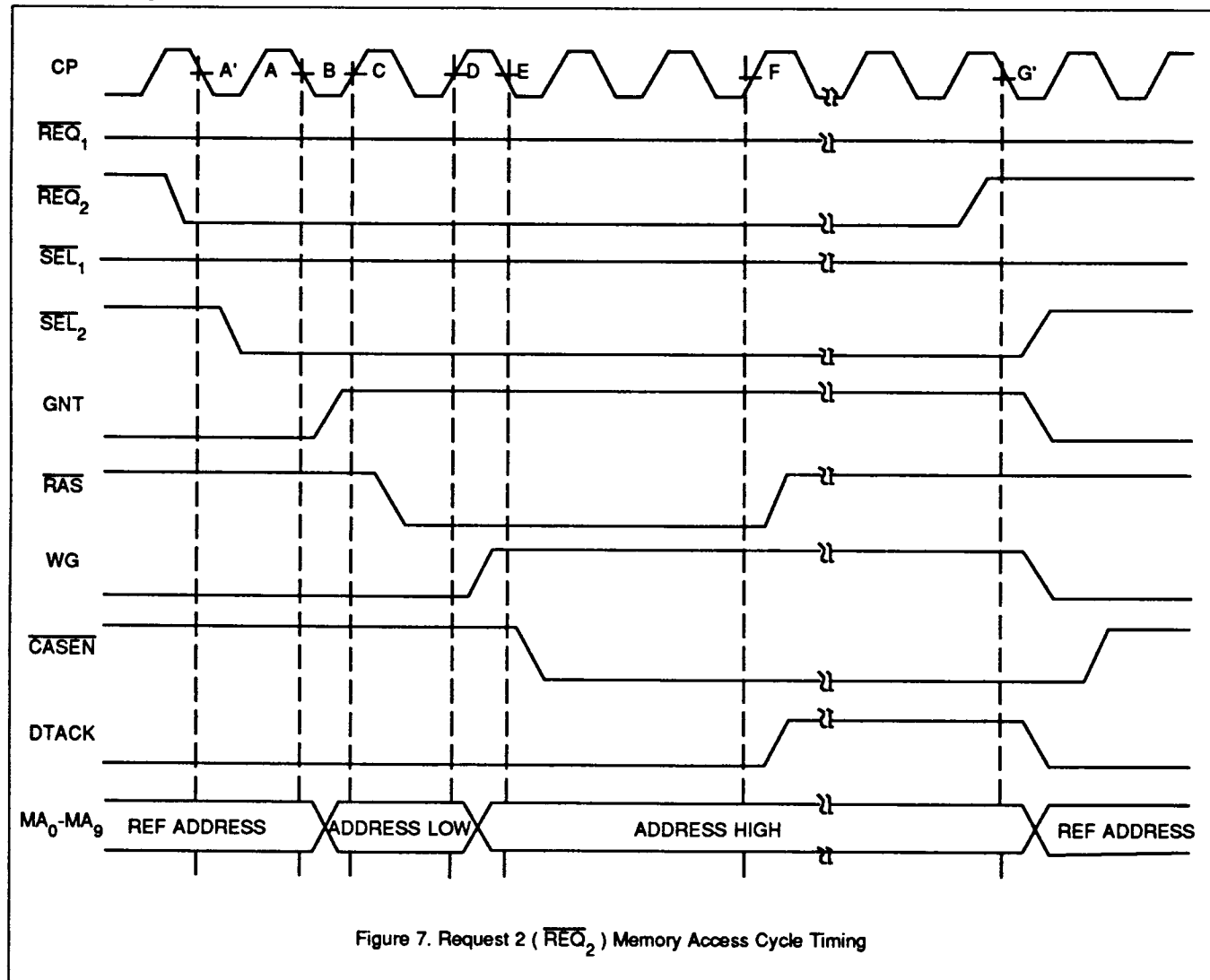
TIMING DIAGRAM



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74F1764-1, 74F1765-1

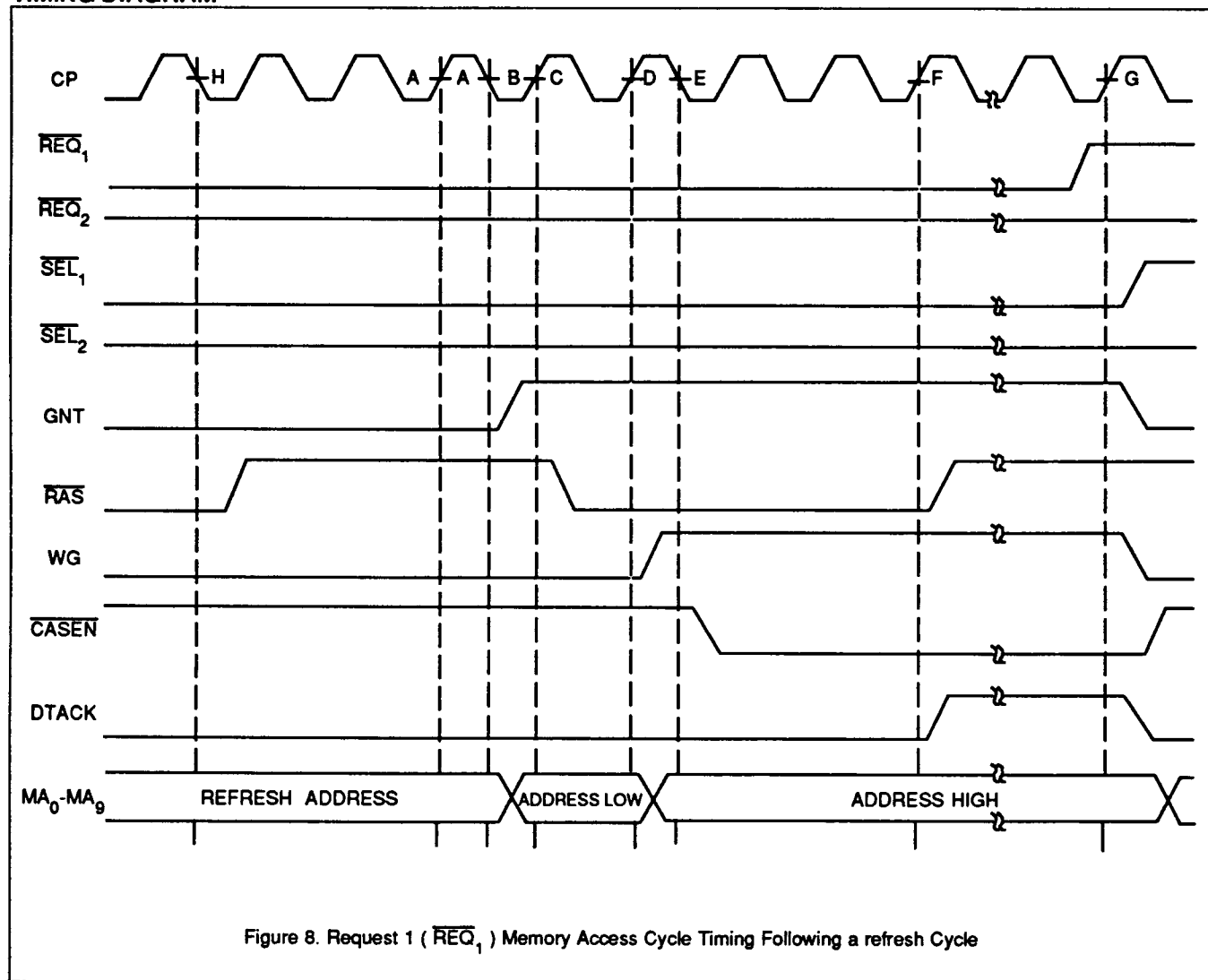
TIMING DIAGRAM



1 Megabit DRAM Dual-Ported Controllers

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74F1764-1, 74F1765-1

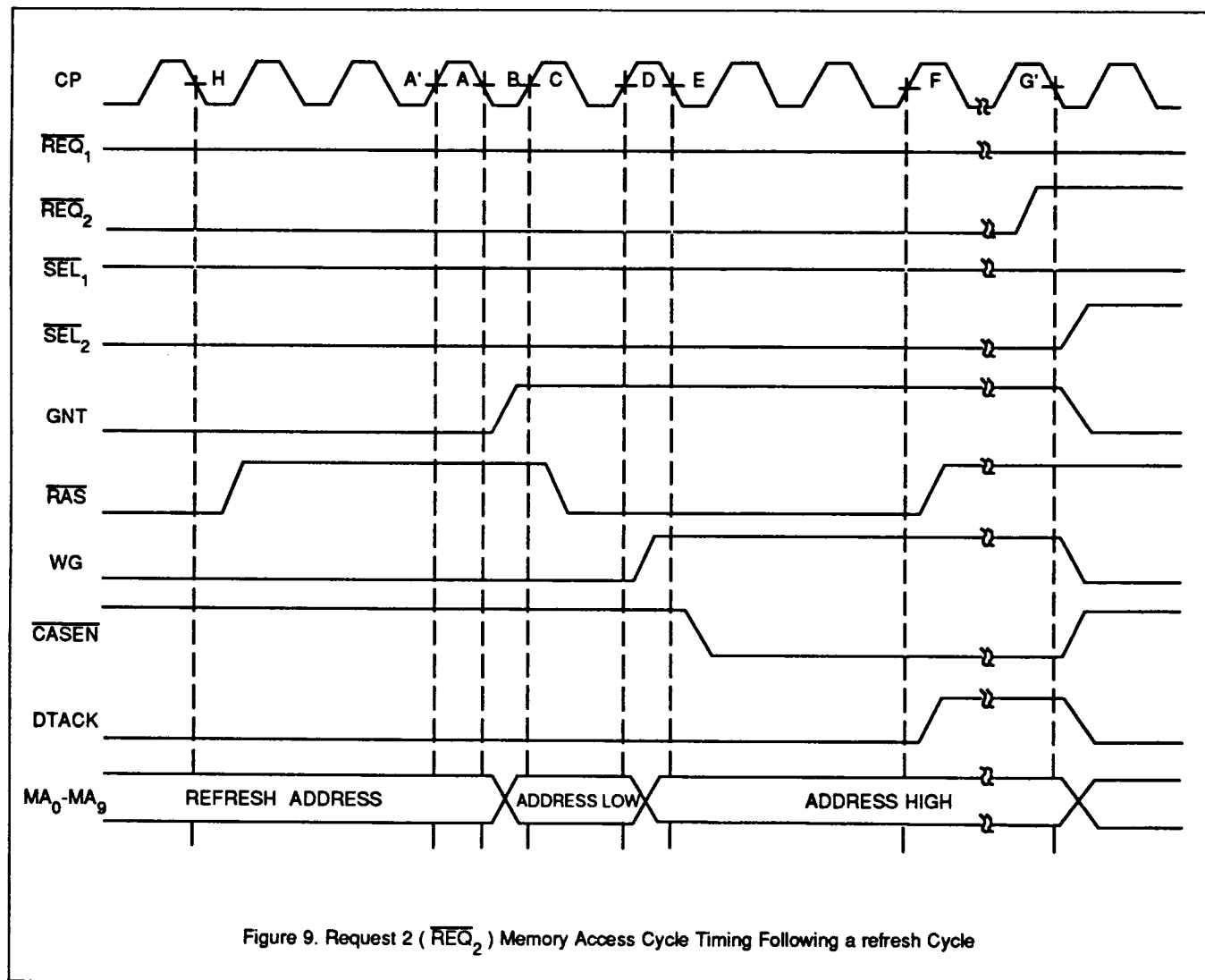
TIMING DIAGRAM



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TIMING DIAGRAM



1 Megabit DRAM Dual-Ported Controllers

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74F1764-1, 74F1765-1

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_H	High-level input voltage		2.0			V
V_L	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current ¹	74F1764/74F1765			-15	mA
		74F1764-1/74F1765-1			-20	mA
I_{OL}	Low-level output current ¹	74F1764/74F1765			24	mA
		74F1764-1/74F1765-1			8	mA
T_A	Operating free-air temperature range		0		70	°C

NOTES:

1. Transient currents will exceed these values in actual operation. Please refer to Appendix A for a detailed discussion.

1 Megabit DRAM Dual-Ported Controllers

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74F1764-1, 74F1765-1**DC ELECTRICAL CHARACTERISTICS** (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹			LIMITS			UNIT
						Min	Typ ²	Max	
V _{OH}	High-level output voltage	74F1764 74F1765	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -15mA	±10%V _{CC}	2.5			V
V _{OH2} ³					±5%V _{CC}	2.7			V
V _{OH}		74F1764-1 74F1765-1	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -20mA	±10%V _{CC}	2.4	2.7		V
					±5%V _{CC}	2.6	3.0		V
V _{OL}	Low-level output voltage	74F1764 74F1765	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = 24mA	±10%V _{CC}		0.35	0.50	V
					±5%V _{CC}		0.35	0.50	V
		74F1764-1 74F1765-1	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL2} ⁴ = 60mA	±5%V _{CC}		0.45	0.80	V
					I _{OL} = 8mA	±10%V _{CC}		0.30	0.50
V _{OH2} ³					±5%V _{CC}		0.30	0.50	V
				I _{OL2} ³ = 75mA	±5%V _{CC}		2.1	2.5	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}				-0.73	-1.2	V
I _I	Input current at maximum input voltage		V _{CC} = 0.0V, V _I = 7.0V					100	μA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7V					20	μA
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.5V					-0.6	mA
I _{OS}	Short-circuit output current ⁵		74F1764 74F1765	V _{CC} = MAX		-100		-225	mA
			74F1764-1 74F1765-1	V _{CC} = MAX		-60	100	-150	mA
I _{CC}	Supply current (total)	I _{CCH}	74F1764 74F1765	V _{CC} = MAX			150	200	mA
		I _{CCL}				165	210	mA	
		I _{CCH}	74F1764-1 74F1765-1				120	165	mA
		I _{CCL}				125	170	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- Refer to Appendix A.
- Refer to Appendix A.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS for 74F1764/74F1765

SYMBOL	PARAMETER	TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
			$T_A = +25^{\circ}\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 300\text{pF}$ $R_L = 70\Omega$			$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 300\text{pF}$ $R_L = 70\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		100	150		100		MHz
t_{PLH}	Propagation delay, CP(G) to SEL_1		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(A) to SEL_1		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(G') to SEL_2		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(A') to SEL_2		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(B) to GNT		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to GNT		5.0	10.0	15.0	5.0	16.0	ns
t_{PLH}	Propagation delay		5.0	12.0	17.0	5.0	18.0	ns
t_{PHL}	CP(B) to MA (row address)		5.0	11.0	15.0	5.0	16.0	
t_{PLH}	Propagation delay, CP(F or H) to $\overline{\text{RAS}}$		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(C) to $\overline{\text{RAS}}$		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(D) to WG		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to WG		8.0	13.0	17.0	8.0	18.0	ns
t_{PLH}	Propagation delay		5.0	12.0	17.0	5.0	18.0	ns
t_{PHL}	CP(D) to MA (column address)		5.0	10.0	15.0	5.0	16.0	
t_{PLH}	Propagation delay, CP(G or G') to $\overline{\text{CAsEN}}$		7.0	17.0	23.0	7.0	25.0	ns
t_{PHL}	Propagation delay, CP(E) to $\overline{\text{CAsEN}}$		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(F) to DTACK		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to DTACK		6.0	13.0	17.0	5.0	18.0	ns
t_{PLH}	Propagation delay		4.0	7.0	12.0	4.0	13.0	ns
t_{PHL}	$\text{RA}_0\text{-RA}_9, \text{CA}_0\text{-CA}_9$ to $\text{MA}_0\text{-MA}_9$	74F1765 only	2.0	5.0	8.0	4.0	9.0	

AC SETUP REQUIREMENTS for 74F1764/74F1765

SYMBOL	PARAMETER		TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
				$T_A = +25^{\circ}\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 300\text{pF}$ $R_L = 70\Omega$			$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 300\text{pF}$ $R_L = 70\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low REQ ₁ , REQ ₂ to CP			2.0 2.0			2.0 2.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low REQ ₁ , REQ ₂ to CP			2.0 2.0			3.0 3.0		ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low RA ₀ -RA ₉ , CA ₀ -CA ₉ to CP	74F1764 only		-4.0 ¹ -4.0			-5.0 -5.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low RA ₀ -RA ₉ , CA ₀ -CA ₉ to CP			5.0 5.0			5.0 5.0		ns
$t_w(\text{H})$ $t_w(\text{L})$	CP Pulse width, High or Low			5.0 5.0			5.0 5.0		ns
$t_w(\text{H})$ $t_w(\text{L})$	RCP Pulse width, High or Low			10.0 10.0			10.0 10.0		ns

NOTES:

1. These numbers indicate that the address inputs have a negative setup time and could not be valid 4ns after the falling edge of the CP clock. It is suggested that SEL_2 be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of SEL_1 to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.

1 Megabit DRAM Dual-Ported Controllers

FAST 74F1764, 74F1765,
74F1764-1, 74F1765-1

AC ELECTRICAL CHARACTERISTICS for 74F1764-1/74F1765-1

SYMBOL	PARAMETER		TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
				$T_A = +25^{\circ}\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 300\text{pF}$ $R_L = 70\Omega$			$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 300\text{pF}$ $R_L = 70\Omega$		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency			150	175		100		MHz
t_{PLH}	Propagation delay, CP(G) to SEL_1			9.0	12.0	15.0	8.0	17.0	ns
t_{PHL}	Propagation delay, CP(A) to SEL_1			13.0	16.0	20.0	12.0	22.0	ns
t_{PLH}	Propagation delay, CP(G') to SEL_2			9.0	12.0	15.0	8.0	17.0	ns
t_{PHL}	Propagation delay, CP(A') to SEL_2			13.0	16.0	20.0	12.0	22.0	ns
t_{PLH}	Propagation delay, CP(B) to GNT			9.0	12.0	14.0	8.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to GNT			20.0	23.0	26.0	17.0	28.0	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA (row address)			11.0 14.0	14.0 18.0	17.0 22.0	10.0 13.0	19.0 24.0	ns
t_{PLH}	Propagation delay, CP(F or H) to $\overline{\text{RAS}}$			11.0	14.0	16.0	10.0	18.0	ns
t_{PHL}	Propagation delay, CP(C) to $\overline{\text{RAS}}$			13.0	17.0	20.0	12.0	22.0	ns
t_{PLH}	Propagation delay, CP(D) to WG			9.0	11.0	14.0	8.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to WG			20.0	23.0	26.0	19.0	26.0	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA (column address)			12.0 14.0	14.0 18.0	17.0 21.0	11.0 13.0	19.0 23.0	ns
t_{PLH}	Propagation delay, CP(G or G') to $\overline{\text{CAsEN}}$			14.0	17.0	20.0	12.0	22.0	ns
t_{PHL}	Propagation delay, CP(E) to $\overline{\text{CAsEN}}$			14.0	16.0	19.0	13.0	21.0	ns
t_{PLH}	Propagation delay, CP(F) to DTACK			10.0	12.0	15.0	9.0	17.0	ns
t_{PHL}	Propagation delay, CP(G or G') to DTACK			20.0	23.0	26.0	19.0	28.0	ns
t_{PLH} t_{PHL}	Propagation delay $\text{RA}_0\text{-RA}_9, \text{CA}_0\text{-CA}_9$ to $\text{MA}_0\text{-MA}_9$	'F1765-1 only		9.0 9.0	11.0 12.0	14.0 15.0	8.0 8.0	16.0 17.0	ns

AC SETUP REQUIREMENTS for 74F1764-1/74F1765-1

SYMBOL	PARAMETER		TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
				$T_A = +25^{\circ}\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 300\text{pF}$ $R_L = 70\Omega$			$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 300\text{pF}$ $R_L = 70\Omega$		
				Min	Typ	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low $\overline{\text{REQ}}_1, \overline{\text{REQ}}_2$ to CP			3.0 3.0	1.0 1.0		4.0 4.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low $\overline{\text{REQ}}_1, \overline{\text{REQ}}_2$ to CP			2.0 2.0	0 0		3.0 3.0		ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low $\text{RA}_0\text{-RA}_9, \text{CA}_0\text{-CA}_9$ to CP	74F1764-1 only		0 0	-1.0 ¹ -1.0 ¹		1.0 1.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low $\text{RA}_0\text{-RA}_9, \text{CA}_0\text{-CA}_9$ to CP			5.0 5.0	3.0 3.0		6.0 6.0		ns
$t_w(\text{H})$ $t_w(\text{L})$	CP Pulse width, High or Low			5.0 5.0	3.0 3.0		5.0 5.0		ns
$t_w(\text{H})$ $t_w(\text{L})$	RCP Pulse width, High or Low			5.0 5.0			5.0 5.0		ns

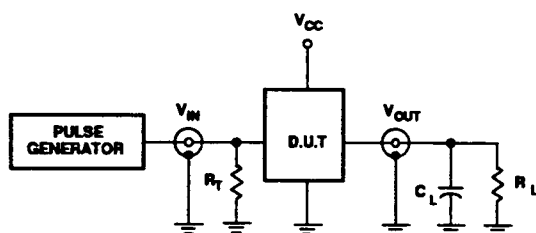
NOTES:

1. These numbers indicate that the address inputs have a negative setup time and could not be valid 4ns after the falling edge of the CP clock. It is suggested that SEL_2 be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of SEL_1 to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.

1 Megabit DRAM Dual-Ported Controllers

 FAST 74F1764, 74F1765,
74F1764-1, 74F1765-1

TEST CIRCUIT AND WAVEFORMS

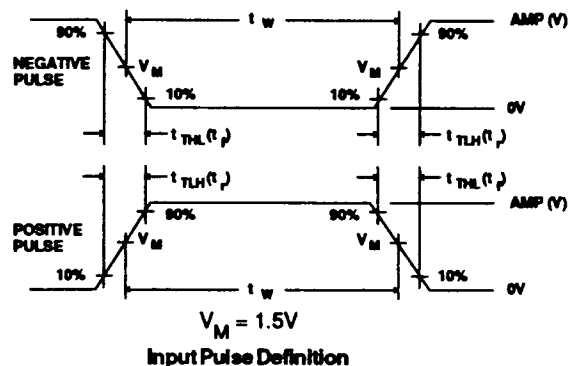


Test Circuit For Totem-Pole Outputs

DEFINITIONS

 R_L = Load resistor; see AC CHARACTERISTICS for value.

 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.


Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

APPLICATIONS

The 1 Megabit DRAM dual-ported controller can be designed into a wide range of single and dual-port interface configurations. The processors could be general or special-purpose (microcontrollers) and the data bus may differ in size.

Figure 10 shows two 68000 processors sharing a 4Meg X 8 (two banks each consisting of sixteen 1 Meg devices) memory. Since the 68000 does not have a multiplexed address and data bus, the 'F 1765/F1765-1 is appropriate.

Address bit (A21) from either the two 68000 processors distinguishes between Memory Banks A and B. Where Bank A consists of Upper Data Byte A (UDBA) and Lower Data Byte A (LDBA) and Bank B consists of Upper Data Byte B (UDBB) and Lower Data Byte B (LDBB).

Upper and Lower Data Strobes (UDS and LDS) from either of the two 68000 determine whether a byte or word transfer will take place. The additional circuitry is to ensure that DTACK to the 68000 is as-

serted only when it is selected.

Figure 11 shows two 8086 processors sharing 1 Mbyte (two banks each consisting of sixteen 256K X 1 devices) of dynamic RAM. Using 'F1764/1764-1 in this application may eliminate the need for an external address latch.

Similarly Figure 12 shows two 6020 processors sharing 4Mbyte of memory.

1 Megabit DRAM Dual-Ported Controllers

FAST 74F1764, 74F1765,
74F1764-1, 74F1765-1

APPLICATION

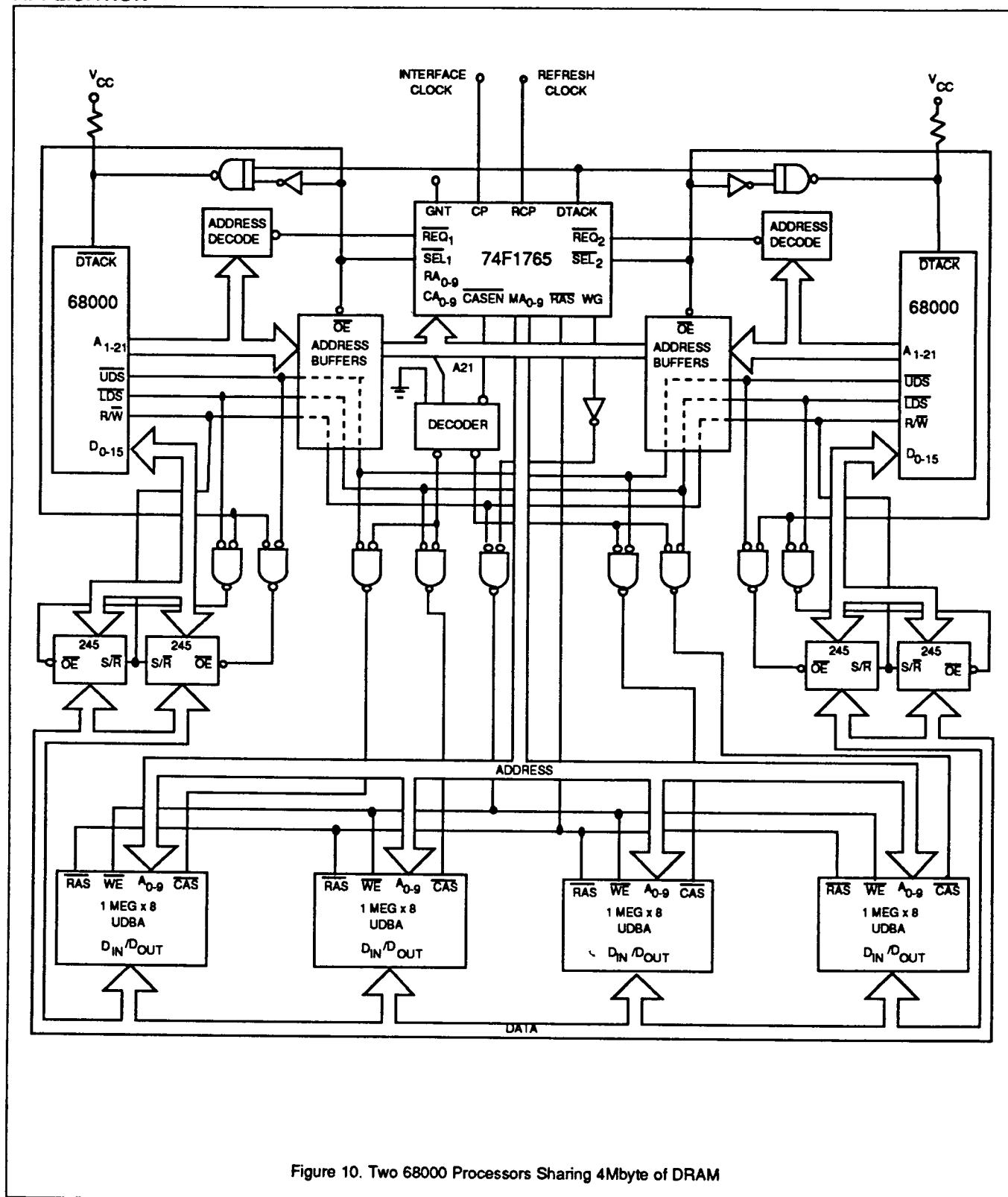
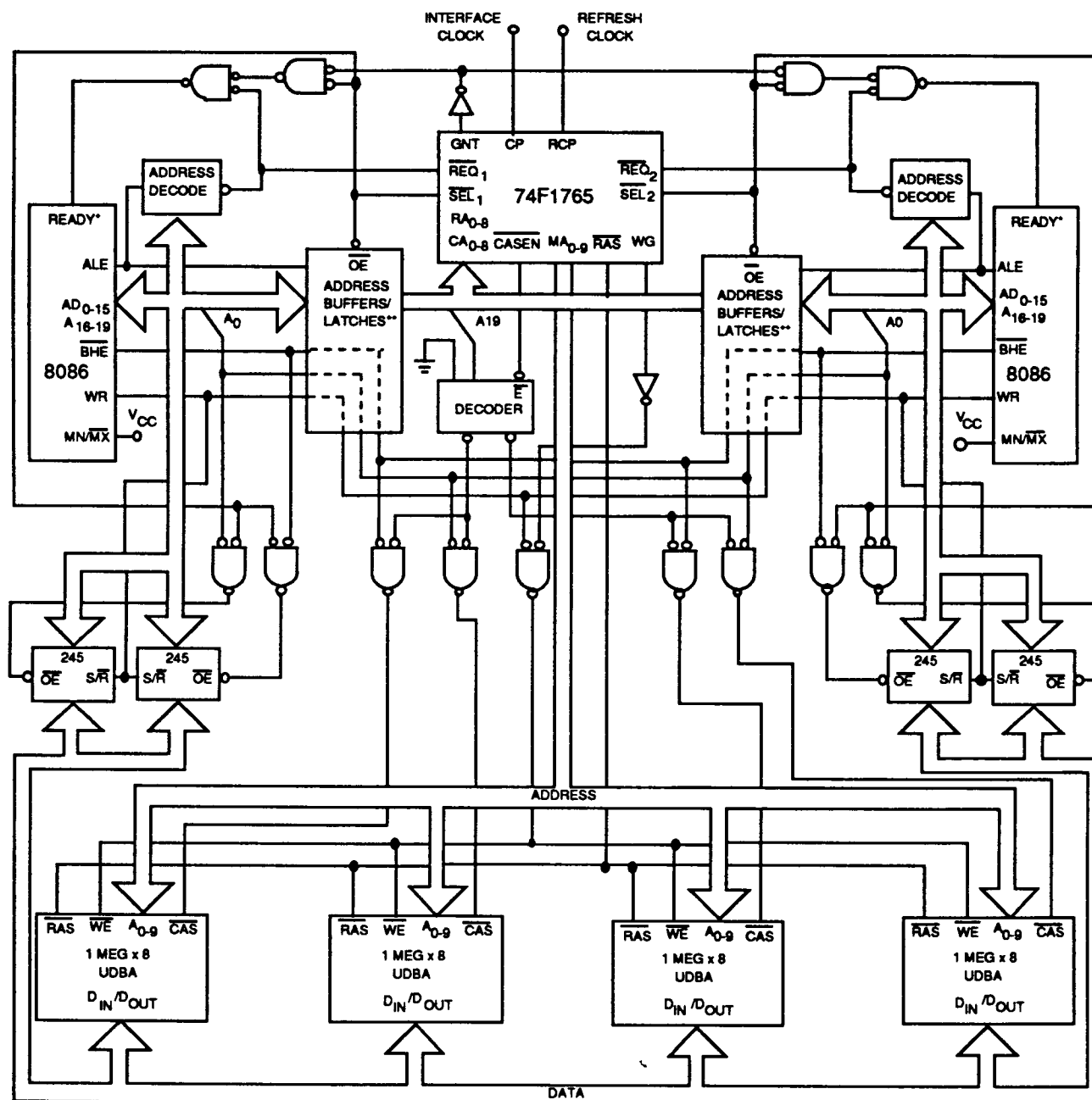


Figure 10. Two 68000 Processors Sharing 4Mbyte of DRAM

1 Megabit DRAM Dual-Ported Controllers

FAST 74F1764, 74F1765,
74F1764-1, 74F1765-1

APPLICATION



Notes:

*= It might be necessary to synchronize READY by the 8284A. Please refer to the 8086 data sheet.

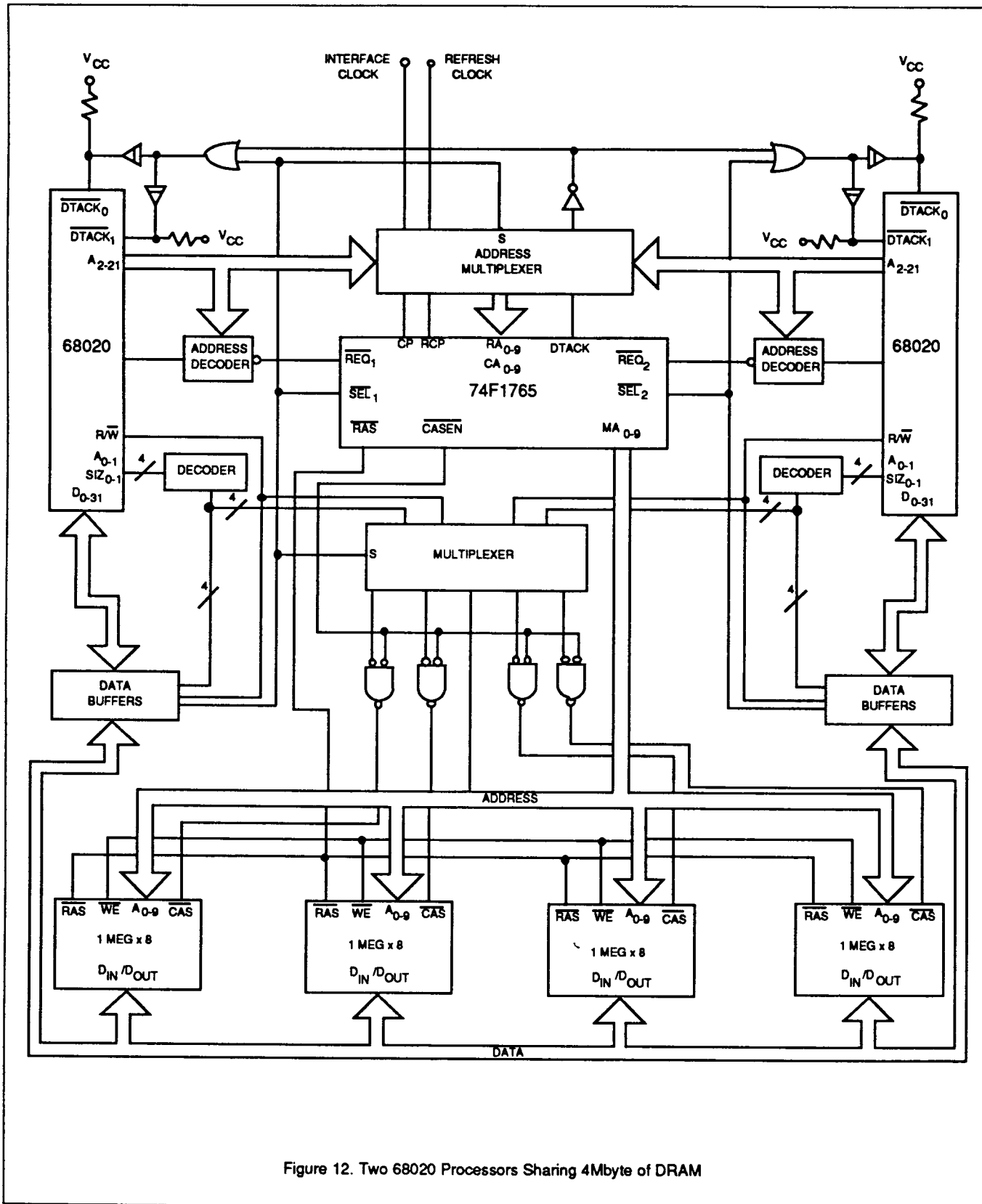
**= Whether or not the 8086 address needs to be latched externally, should be determined by the relative speeds of the 8086 and the controller

Figure 11. Two 8086 Processors Sharing 1Mbyte of DRAM

1 Megabit DRAM Dual-Ported Controllers

FAST 74F1764, 74F1765,
74F1764-1, 74F1765-1

APPLICATION



1 Megabit DRAM Dual-Ported Controllers

FAST 74F1764, 74F1765,
74F1764-1, 74F1765-1

APPENDIX A

74F1764 FAMILY LINE DRIVING CHARACTERISTICS

The 74F1764/1765 are designed to provide wave switching in dual-in package (DIP) or zig-zag in-line package (ZIP) housed memory arrays and first reflected wave switching in single in-line package (SIP) or single in-line module (SIM) housed arrays. The 74F1764-1/1765-1, on the other hand, are designed to provide first reflected wave switching with as wide a range of characteristics impedances as possible.

The I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} parameters are included in the product specifications to assist engineers in designing systems which will switch memory array signal lines in the above mentioned manner. For example, the characteristic impedance of signal lines in DIP housed memory arrays is usually around 70Ω. If a signal line has settled out in a High state at 4V and must be pulled down to 0.8V or less on the

incident wave, the DRAM controller output must sink (4-0.8)/70A or 46mA at 0.8V. The I_{OL2}/V_{OL2} parameter indicates that the signal line in question will always be switched on the incident wave over the full commercial operating range.

It should be noted here that I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} are intended for transient use only and that steady state operation at I_{OH2} or I_{OL2} is not recommended (long term, steady-state operation at these currents may result in electromigration).

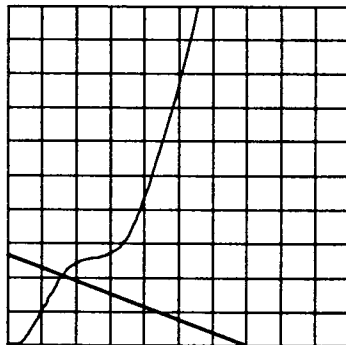
Figures 1-4 show the output I/V characteristics of the DRAM Controller family of devices. These figures also demonstrate graphical method for determining the incident wave (and first reflected wave) characteristics of the devices.

The suggested line termination for the

74F1764/1765 driving a dual in-line packaged or zig-zag packaged DRAMs is shown in Figure 8a. When driving single in-line modules using the 74F1764/1765 or when driving any type of memory arrays with the 74F1764-1/1765-1, The Schottky diode termination shown in Figure 8b can be used (most of these will need no termination at all).

Figures 5-7 are double exposures showing the High to Low to High transitions while driving four banks of eight dual in-line packaged DRAMs. The signal line is unterminated in Figures 5 and 6, allowing the 74F1764/1765 to ring two volts below ground while the 74F1764-1/1765-1 make nice clean transitions. In Figure 7 the 74F1764/1765 is driving the same signal line but with one of its four branches terminated in series with 300 pF to ground (the worst of the four branches is shown).

Output
Current-I
(50mA per
division)

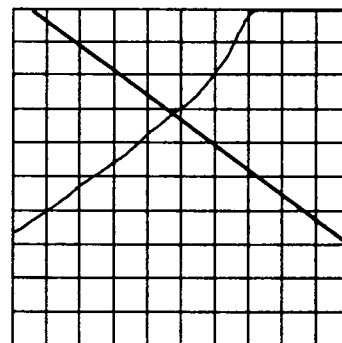


Output Voltage-V
(500mV per division)

Figure 1.

I-V Output Characteristics of the 74F1764/1765 in the Low state. Light line is the I-V Curve of a 25Ω transmission line settled to 3.5V (typical for recommended termination). The High to Low incident wave on this line will typically be to 0.8V.

Output
Current-I
(50mA per
division)



Output Voltage-V
(500mV per division)

Figure 2.

I-V Output Characteristics of the 74F1764/1765 in the High state. Light line is the I-V Curve of a 35Ω transmission line settled to 0.25V. The incident wave on the Low to High transition will typically be to 2.4V on this line. Any line over 35Ω will typically be switched on the incident wave.

1 Megabit DRAM Dual-Ported Controllers

FAST 74F1764, 74F1765,
74F1764-1, 74F1765-1

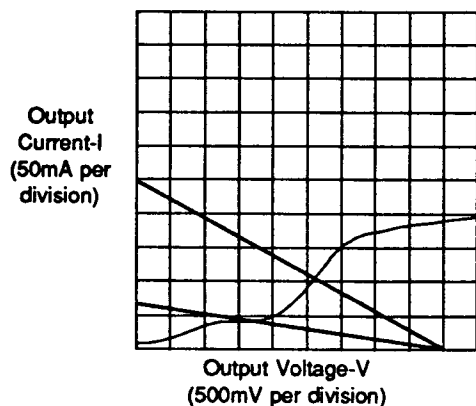


Figure 3.

I-V Output Characteristics of the 74F1764-1/1765-1 in the Low state. Any unterminated line impedance between 18Ω and 70Ω (both shown) will typically switch on the first reflected wave without violating the -1V minimum input voltage specification typical of DRAMs

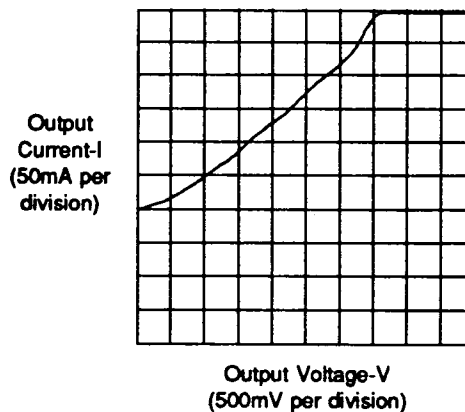


Figure 4.

I-V Output Characteristics of the 74F1764-1/1765-1 in the High state.

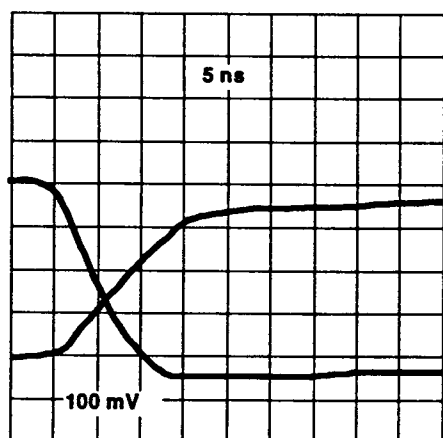


Figure 5.

74F1764-1/1765-1 Driving 32 DRAMS (Unterminated)

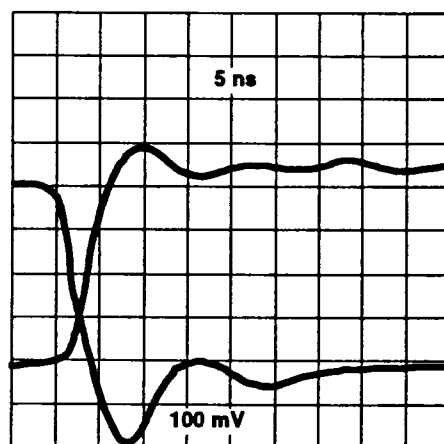


Figure 6.

74F1764/1765 Driving 32 DRAMS (Unterminated)

1 Megabit DRAM Dual-Ported Controllers

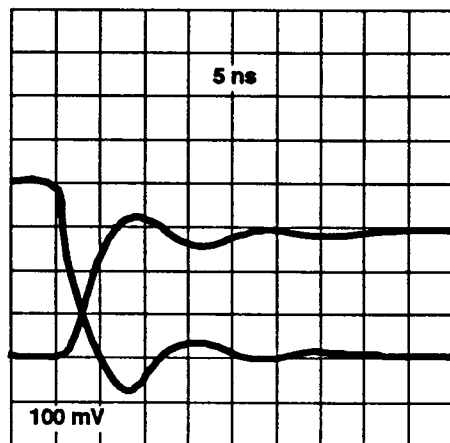
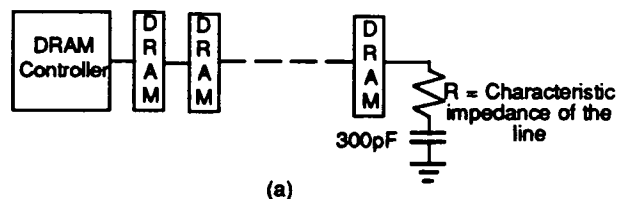
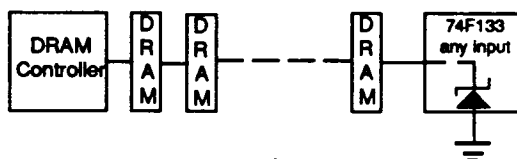
 FAST 74F1764, 74F1765,
74F1764-1, 74F1765-1


Figure 7.
74F1764/1765 Driving 32 DRAMS (Terminated as in Figure 8a)



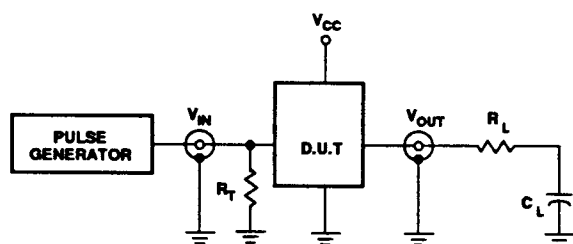
(a)



(b)

Figure 8.
74F1764/1765 Driving 32 DRAMS (Unterminated)

TEST CIRCUIT AND WAVEFORMS



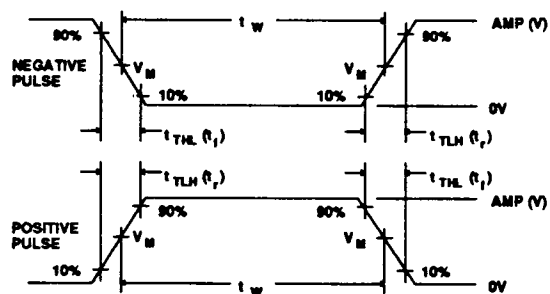
Test Circuit Simulating RAM Boards

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$$V_M = 1.5V$$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns