L64780
DVB-T COFDM Demodulator

Technical Manual

February 2000

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This document describes LSI Logic Corporation's L64780 DVB-T COFDM Demodulator and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

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Preface

This book is the primary reference and technical manual for the L64780 DVB-T COFDM Demodulator. It contains a complete functional description as well as complete physical and electrical specifications for the LSI Logic L64780.

Audience

This document assumes you are familiar with digital video broadcasting, terrestrial television transmission and reception, modulation/demodulation, error control coding, digital signal processing, microprocessors, and related support devices. The people who benefit from this book are:

- engineers and managers evaluating the L64780 for use in a receiver for digital TV or cable data transmissions.
- engineers designing the L64780 into a system.

Organization

This document has the following chapters and appendixes:

- Chapter 1, **Introduction**, provides a brief overview of the L64780 and lists its features and benefits.
- Chapter 2, **Architectural Overview**, describes the architecture of the L64780 and gives a functional description of its main components.
- Chapter 3, **Interfaces**, describes the interfaces of the L64780 and gives a functional description of each.
- Chapter 4, **Register Descriptions**, provides a description of the registers that determine the functionality of the L64780.

- Chapter 5, **Signal Descriptions**, provides a description of the signals used and generated by the L64780.
- Chapter 6, **Specifications**, describes the specifications for the L64780 electrical and mechanical characteristics.
- Appendix A, **Programming the L64780 Using The Serial Bus Interface**, describes how to program the L64780 using the Serial Bus.

Related Publications

ETSI Specification ETS 300 744. 1997. “Digital broadcasting systems for television, sound and data services; Framing structure, channel coding and modulation for digital terrestrial television.”

Stott, J.H., 1996. *The DVB Terrestrial (DVB-T) Specification and its Implementation In a Practical Modem*. International Broadcasting Convention 1996.

Conventions Used in This Manual

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive.

Hexadecimal numbers are indicated by the prefix “0x” (for example, 0x32CF). Binary numbers are indicated by the prefix “0b” (for example, 0b0011.0010.1100.1111).

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Chapter 1
Introduction

This chapter provides an overview of the LSI Logic L64780 DVB-T COFDM Demodulator. It also lists this chip's features and benefits, and provides an illustrated description of its typical performance. This chapter contains the following sections:

1.1 Overview

The L64780 is part of a digital terrestrial television receiver for signals transmitted in accordance with the Digital Video Broadcasting-Terrestrial/European Telecommunications Standards Institute (DVB-T/ETSI) specification. These signals convey digital information using Coded Orthogonal Frequency Division Multiplexing (COFDM), as well as concatenated Reed-Solomon and convolutional forward error correction (FEC) techniques. This information payload takes the form of an MPEG-2 transport stream that conveys picture, sound, and data information. This MPEG-2 transport stream format is used also in related specifications for the transmission of digital television signals by satellite or cable.

The concatenated coding used in the DVB-T/ETSI specification is identical to that in the DVB-S specification for satellite transmissions. The FEC decoder can take the same form in receivers for satellite as well as terrestrial transmissions. Thus, the L64780 chip provides all the necessary demodulation functions *except* for FEC decoding, which is done by a separate chip, such as the L64724 or the L64705. The L64780 I/O format and pinouts simplify its connection to the L64724/L64705.

The DVB-T/ETSI specification incorporates many modes, providing a wide range of capacity/performance trade-off options. The L64780 demodulates all these modes.

Terrestrial transmission paths are prone to multipath, which can result in “ghosting” on analog television pictures. With conventional methods of digital transmission, multipath causes inter-symbol interference. This becomes increasingly problematic as the bit rate increases.

The DVB-T/ETSI specification uses a special form of modulation that uses Coded Orthogonal Frequency Division Multiplexing, which is well-suited to channels with significant multipath. It can tolerate signals with long delay and high relative amplitude. Consequently, the L64780 can accommodate natural multipath (from terrain, buildings, etc.) and it can be used in a Single Frequency Network (SFN). In an SFN, many transmitters operate on the same frequency with the same modulation (used in Digital Audio Broadcasting, which also uses COFDM).

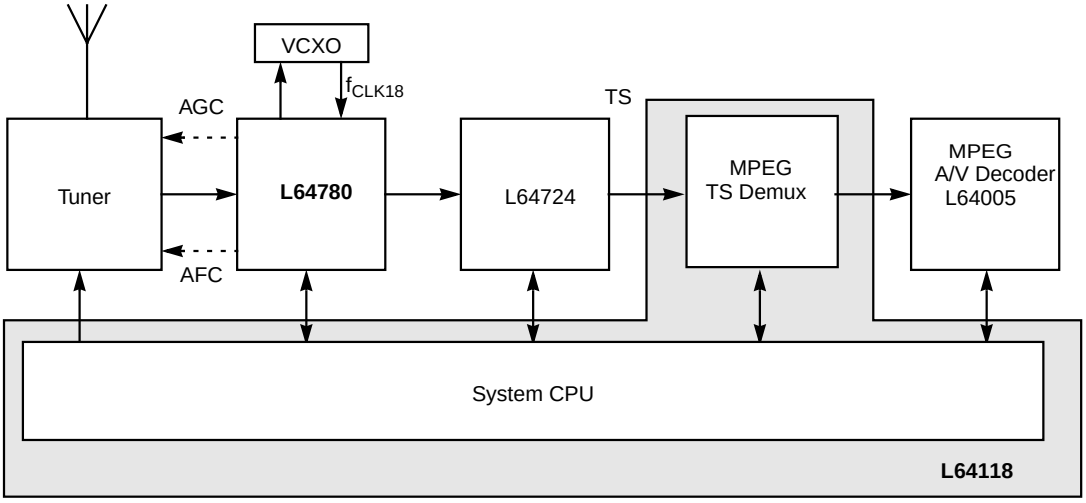
In the frequency domain, multipath can be seen as channel frequency selectivity. COFDM applies concatenated FEC coding, then distributes the coded data over many carriers (1705 or 6817 in this case, depending on the mode). At the receiver, the frequency selectivity of the channel causes some carriers to be degraded or suppressed. However, the receiver can determine how much each carrier is affected by noise, then pass this information to the inner-code Viterbi decoder by means of soft-decision bits. This allows the Viterbi decoder to decode the data more efficiently. A second decoder, for the Reed-Solomon FEC, completes the process.

1.2 Using the L64780 in a Receiver

The L64780 provides those parts of a receiver for DVB-T signals that are exclusive to the terrestrial specification for COFDM demodulation and inner interleaving. This includes synchronization, channel-equalization, and derivation of channel-state information.

The combination of the LSI Logic L64780 and L64724 (or L64705) chips forms the core of a receiver design for DVB-T, supporting two possible approaches: exclusively DVB-T reception, and dual DVB-T/DVB-S reception (see Figure 1.1).

Figure 1.1 Typical Terrestrial-Only Receiver



AGC (automatic gain control)
AFC (automatic frequency control)

Figure 1.1 shows the basic structure for a terrestrial-only receiver. The UHF (or, possibly, VHF) signal from the antenna passes through a Tuner module that delivers a low intermediate frequency (IF) signal to the L64780 chip by means of an analog-to-digital converter (ADC). The L64780 chip performs all the essential functions for COFDM demodulation, excluding the final steps of error correction. It requires a sampling-frequency clock oscillator (at f_{CLK18} MHz), for which it provides the control voltage to lock its frequency to the desired value. The L64780 chip delivers soft-decision information to the L64705 or L64724 chip,

which then completes the error correction, delivering an MPEG-2 Transport Stream. Other MPEG-standard LSI Logic chips (for example, L64118 and L64005) can then be used to demultiplex the MPEG-2 Transport Stream into its coded audio, coded video, and data components, handle Conditional Access, and decode the audio and video signals for presentation to the display and loudspeakers. In Figure 1.1, the microprocessor is embedded in the L64118. It controls RF-channel selection, mode selection for the L64780 chip, and program selection for the MPEG demultiplexer.

1.3 RF Tuner Block Functions

Figure 1.2 indicates the functions performed within the RF Tuner block. The example uses a double-conversion approach, in which the RF Tuner converts the UHF signal to a first IF (IF1, where filtering, amplification, and gain control are done) followed by another conversion to the second low IF, (IF2), required at the input of the L64780.

Figure 1.2 UHF Tuner Example

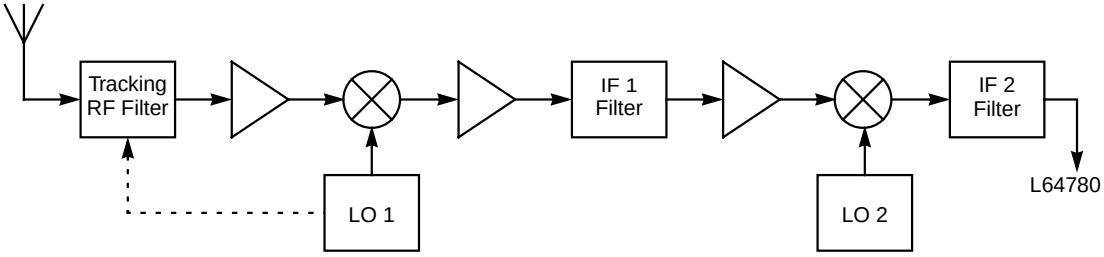


Figure 1.3 illustrates how terrestrial and satellite reception can be combined in one unit. For satellite reception, the IF signal (for example, from 1 to 2 GHz) from the dish unit is fed into a satellite tuner. This tuner:

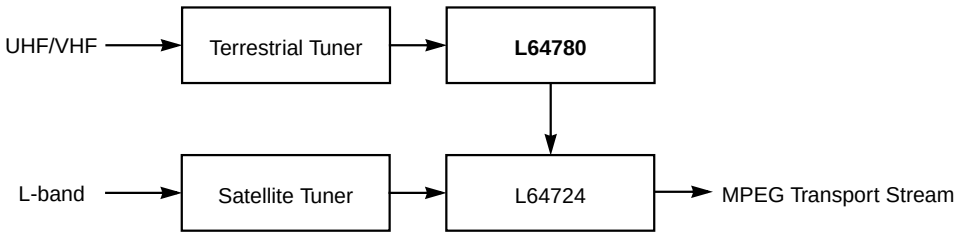
1. Selects one RF signal from the 1 to 2 GHz range
2. Converts the signal to one or more intermediate frequencies
3. Down-converts the signal to base band
4. Feeds its I and Q components into the L64724 single-chip DVB-S satellite receiver

The L64724:

1. Samples the I and Q baseband signals
2. Demodulates the QPSK
3. Processes the error correction functions

The L64724 also implements a bypass of the ADC and demodulation functions. Thus, it can accept the soft decisions delivered by L64780 and feed them directly to the Viterbi decoder. This architecture implements a cost-effective solution for mixed satellite and terrestrial front-ends.

Figure 1.3 Receiver Architecture for Satellite and Terrestrial Reception



1.4 Modes of Operation

The L64780 supports all the modes of the DVB-T specification, including:

- 2 K and 8 K FFT sizes
- Nonhierarchical QPSK, 16 QAM, and 64 QAM constellations
- Hierarchical 16 QAM and 64 QAM constellations
- Constellation scale factors α = 1, 2, and 4
- Code rates of 1/2, 2/3, 3/4, 5/6, and 7/8
- Guard intervals of 1/4, 1/8, 1/16, and 1/32

1.5 Features

The L64780 features include:

- DVB-T compliance
- Internal or external DAC
- Digital real-to-complex conversion
- Spectrum inversion
- 2 K or 8 K FFT size
- Rapid time synchronization
- Rapid frequency synchronization
- Common phase error correction
- High-order filter for frequency interpolation
- Automatic mode switching
- Automatic frame detection
- Use of channel state information for protection against multipath and interference
- 3- or 4-bit soft decision outputs
- Analog or digital AFC
- AGC

- Stand-alone FFT mode (forward or inverse)
- Easy connection to the L64705 or L64724 for FEC
- 160-pin PQFP package

1.6 Typical Performance

Figure 1.4 illustrates the target performance of the L64780 compared to the simulation results in the ETSI specification for all the nonhierarchical modes in a Gaussian channel. Differences between the target performance and the simulations are accounted for as follows:

- About 1.5 dB for the noisy reference effect in the channel equalizer
- 0.1–0.3 dB for noise on the channel state measurement

It is not possible to be specific about the source of the remaining small difference (about 0.4 dB) because we do not have enough information about the conditions under which the simulations were performed.

The two losses (in the channel equalizer and channel state information) are compromises made in the interests of the speed of tracking of a time-varying channel. Sacrificing the tracking ability reduces the losses.

Figure 1.4 Performance with Additive Write Gaussian Noise (AWGN)

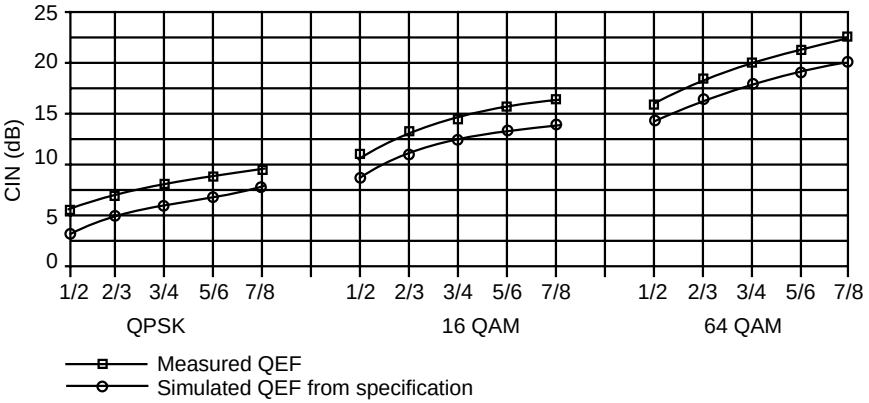


Figure 1.5 illustrates the target protection ratio of PAL-I into DVB-T. The point indicated by “carriers coincident about here” shows the point where the vision carrier of the PAL-I signal lines up directly with one of the carriers on the ODFM frequency raster.

Figure 1.5 DVB-T Carrier to Co-channel PAL-I Interference Ratio for Failure

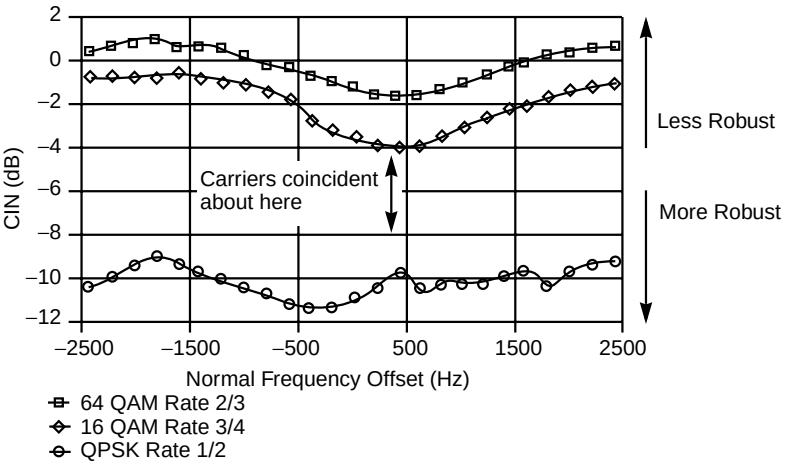
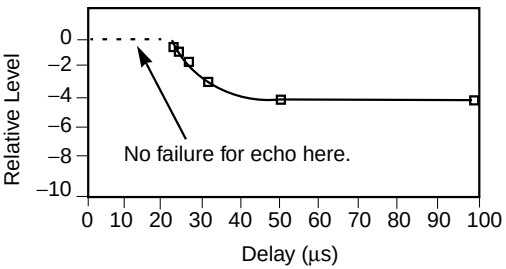


Figure 1.6 illustrates the maximum level of echo acceptable to the demodulator. The graph shows that in the selected mode, the demodulator works without failure inside the guard interval and without failure significantly outside it.

Figure 1.6 Maximum Level of a Single Echo for Failure of QPSK, Rate 1/2, Guard Interval 7



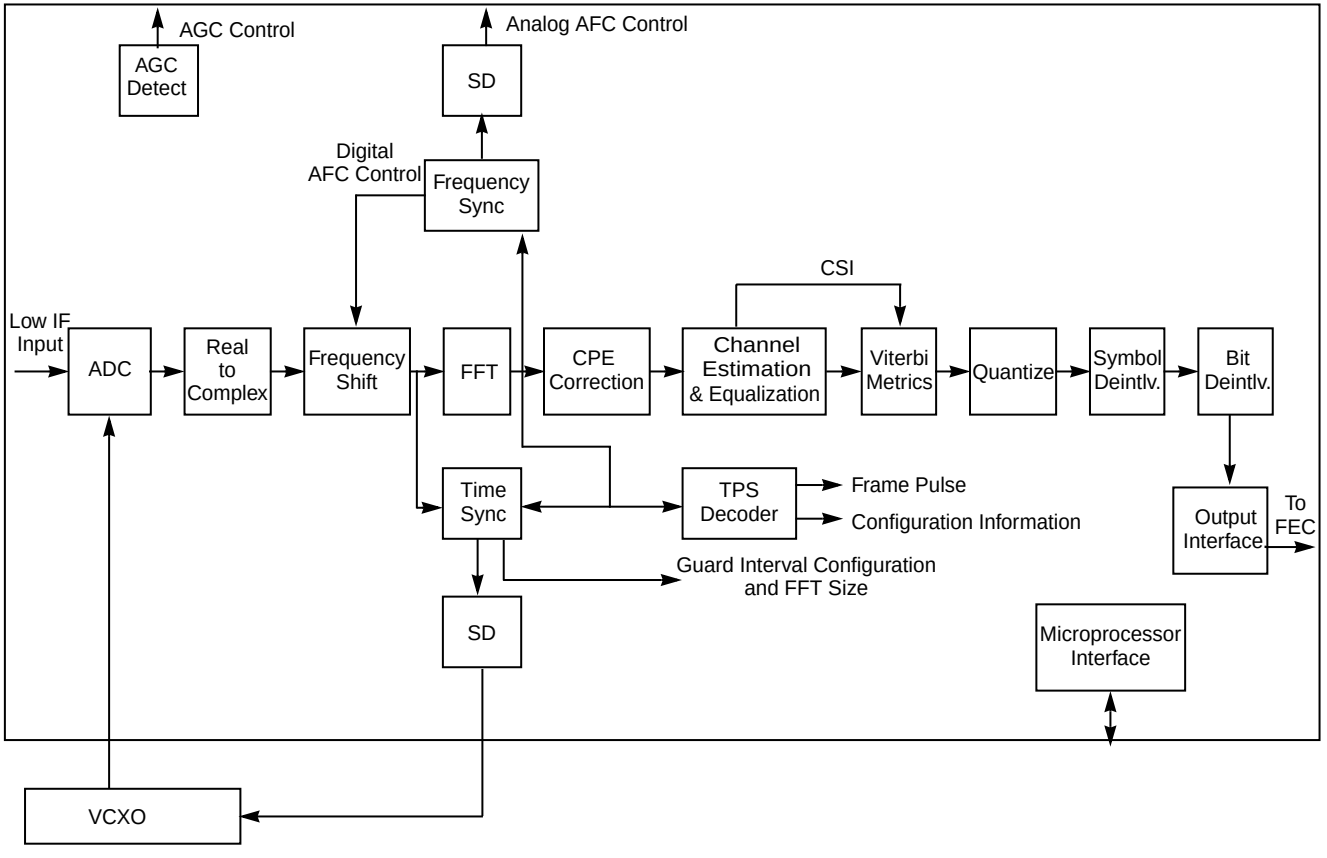
Chapter 2
Architectural Overview

This chapter describes the L64780 architecture and provides a functional description of each of its components. It contains the following sections:

2.1 Demodulator Module Functional Description

The components of the L64780 are integrated to provide a complete system solution for demodulation of terrestrial and satellite originated signals. Figure 2.1 shows the components of the L64780 and indicates their interaction. These components are described in the following sections.

Figure 2.1 DTTV Demodulator Architecture



FFT = Fast Fourier Transform
ADC = Analog-to-digital converter
VCXO = Voltage-controlled crystal oscillator
SD = Sigma-Delta
CSI = Channel state information

2.2 Analog-to-Digital Converter (ADC)

Features of the L64780 analog-to-digital converter include:

- low-IF center frequency input: 4.57 MHz
- input bandwidth: 8 MHz
- sampling clock: 18.29 MHz
- resolution: 8-bit

The L64780 also offers a 10-bit parallel port for connection to an external, 10-bit ADC.

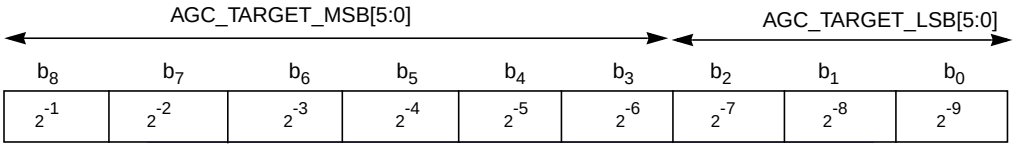
2.3 Automatic Gain Control (AGC)

The Tuner AGC Amplifier amplifies the signal. The resulting signal has an RMS value of σ_0. The AGC amplifies this signal so that its variance allows the FFT to work properly. To do this, the input signal power must be 10.95 dB down on the maximum ADC input range, normalized to 1.0. This means the RMS value of the input to the L64780 is: $\sigma_0 = 0.283$.

2.3.1 AGC Target RMS Value σ_T

Figure 2.2 defines The nine-bit AGC_TARGET register.

Figure 2.2 Structure of 9-Bit AGC_TARGET Register



For the FFT to perform correctly, the input level of the COFDM signal must be 10.95 dB down on the normalized 1.0 Input Range. Thus, the target RMS value, σ, of the input signal must be 0.283, as shown in Equation 2.1.

Equation 2.1 $$\sigma_T = \left\lfloor 512\sqrt{\frac{2}{\pi}} \cdot \sigma \right\rfloor$$

Since the recommended RMS value is $\sigma = 0.283$, the recommended σ_T value is $\sigma = 0.226$, resulting in an AGC_TARGET initial value of 0x74 (0b0111.0100). Thus:

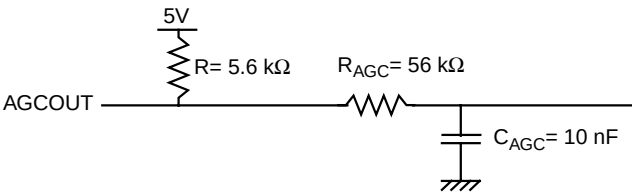
- AGC_TARGET_LSB = 0x4 (0b100)
- AGC_TARGET_MSB = 0x0E (0b01110)

Also see the description in Section 4.4.4, “Address Line 0x0A,” page 4-23.

2.3.2 AGC External Loop Filter

The input power control signal drives the Sigma Delta modulated output, AGCOUT. Use the AGCOUT signal to drive an external passive RC filter that feeds the gain control stage, as shown in Figure 2.3.

Figure 2.3 AGC Loop Pass Filter



The R and C values for the low-pass filter must meet the following requirement:

Equation 2.2 $R_{AGC} \bullet C_{AGC} = 560\ \mu s$

See Figure 2.3 for the recommended values.

2.3.3 AGC Loop Gain K_S

The gain of the loop, K_S, must obey the following rule:

Equation 2.3 $$K_S = \frac{8.5 \times 10^{-5}}{F \cdot \sigma_T}$$

where:

- F is the slope of the tuner AGC characteristics in dB/V.
- σ_T is the target value for the input signal.

With an RMS value of $\sigma = 0.283$, and a tuner characteristic of 50 dB/V, the loop gain is:

Equation 2.4 $$K_S = 7.5 \times 10^{-6}$$

To code K_S, LSI Logic uses an approximation to the nearest power of 2. LSI Logic uses the AGC_GAIN[2:0] register, with the following correspondence:

Equation 2.5 $$K_S \approx 2^{-8-2 \cdot AGC\_GAIN}$$

Because the number of values AGC_GAIN can have is limited, so are those of K_S. Thus,

Equation 2.6 $$AGC\_GAIN \approx \left\lfloor \frac{\log K_S}{2\log 2} - 4 \right\rfloor$$

In our example, AGC_GAIN = 4 is the most appropriate value, giving a value of:

Equation 2.7 $$K_s \approx 1.52 \times 10^{-5}$$

The real-to-complex block takes the input samples from the ADC output and converts them into a complex baseband representation for input to the FFT block.

2.4 Real-to-Complex Conversion

The DVB-T signal occupies a bandwidth of approximately 7.61 MHz; the signal is symmetrically disposed in extent about a notional center carrier. As radiated, this normally lies in the UHF range; however, its spectrum is not symmetrical, because its upper and lower sidebands are different (a double-sideband modulated signal does have a symmetrical spectrum). Thus, a complex representation is needed to describe it at baseband. This spectrum can be derived using the in-phase I and quadrature-phase Q demodulators, but each would have to be sampled separately, using two ADCs and many well-matched components.

The L64780 chip avoids the complexity and expensive matching of analog components. It uses a single ADC, and derives the complex-baseband representation by internal digital processing. The ADC samples the DVB-T signal at a low IF, then the real-to-complex block digitally shifts the samples to complex baseband form, centered on zero frequency. It is fundamental to the operation of this conversion processing that the nominal center frequency (f_{LIF}) of the low IF is related to the sampling frequency, f_{CLK18}, used by the ADC (see Table 2.1, which shows that $f_{CLK18} = 4\ f_{LIF}$ almost exactly). The AFC circuitry of the L64780 ensures that this is the case. The output of the block is complex numbers at the rate of $f_{CLK18}/2$.

The frequencies in Table 2.1 apply for the normal version of the DVB-T specification for use with UHF channels spaced by 8 MHz. To adopt the DVB-T specification for use with 7 MHz or 6 MHz channel spacing, scale the clock frequency and all other frequencies within the system (including the bit-rate capacity and low IF) by factors of 7/8 and 6/8, respectively.

Table 2.1 Approximate and Exact Frequencies for Real to Complex Conversion

	Symbol	Approx. Frequency, MHz	Exact Frequency, MHz
ADC sampling frequency	f_{CLK18}	18.28	128/7
Low-IF center frequency	f_{LIF}	4.57	32/7

2.5 Fast Fourier Transform (FFT) Block

The FFT block converts from the temporal to the frequency domain representation. It has the following modes of operation:

- FFT and Inverse FFT
- 2 k (2048 points) and 8 k (8192 points) mode

2.6 Time Synchronization

This block finds the optimum timing for the start of the FFT window, and synchronizes the frequency of the clock, f_{CLK18}, to the received signal

The options for the duration of the symbol and the duration of the guard interval are given in paragraph 4.4 of the DVB-T/ETSI Specification.

The block takes the sequence of complex numbers from the real-to-complex conversion block and, to synchronize the clock, produces a control signal for the voltage-controlled oscillator. The control voltage of the VCXO is converted into a Sigma-Delta (Σ/Δ) Modulated signal and output as a single wire signal. This signal requires external low-pass filtering to extract its mean value, which represents the control voltage of the oscillator.

The transmitter repeats a segment of the signal during the guard interval. This block detects the repeated portion of the signal. The signal processing resists impairment from high levels of echoes or interference.

2.6.1 Timing Loop Gain

In 2 k mode, the optimal IIRGAIN is 0b01, or $\alpha \approx 3.125 \times 10^{-2}$.

This leads to K_I and K_P values of:

Equation 2.8

$$K_I = \frac{1.69}{K_{VCXO}} \qquad K_P = 512 \times K_I$$

In 8 k mode, the optimal IIRGAIN is 0b11, or $\alpha \approx 7.8 \times 10^{-3}$.

This leads to K_I and K_P values equal to:

Equation 2.9

$$K_I = \frac{0.1}{K_{VCXO}} \qquad K_P = 512 \times K_I$$

2.6.2 TIM_CLK_INIT Register Definition

The TIM_CLK_INIT register is defined as a two's complement 15-bit register that has the following meaning:

Equation 2.10

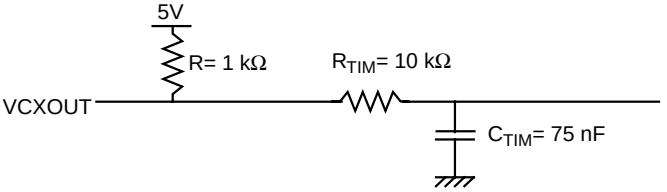
$$W_i = W_0 + \frac{5K_{VCXO} \times \text{TIM\_CLK\_INIT}}{2^{15}}$$

where W_0 is the central frequency of the VCXO.

2.6.3 TIM External Loop Filter

The control voltage signal of the VCXO drives the Sigma Delta modulated output, VCXOUT. Use the VCXOUT to drive an external passive RC filter that feeds the timing clock control stage. See Figure 2.4.

Figure 2.4 External Low-Pass Loop Filter



The –3 dB cutoff frequency of this system is f_0 = 212 Hz, giving an estimate of the TIM Loop Bandwidth and resulting in a low-pass filter time constant $T1 = RC$ = 750 µs.

The R and C values for the low-pass filter must meet the following requirement: $R_{TIM} \bullet C_{TIM}$ = 750 µs.

2.7 Automatic Frequency Control (AFC)

The two methods for applying the correction required to achieve frequency synchronization are analog and digital. The method used depends on the design of the analog tuner. The L64780 allows both options, which are described in the following subsections.

2.7.1 Analog Frequency Synchronization

This block adjusts the frequency of the local oscillator in the tuner so that the center frequency of the low IF is equal to its nominal value of f_{LIF}. The adjustment must be accurate to within a small fraction of the carrier spacing, so that intercarrier interference is kept to an acceptably low level and the tracking ability of the channel estimation is not absorbed in correcting for the error in the frequency of the local oscillator.

The block takes the sequence of complex numbers from the output of the FFT block and produces a control signal for the local oscillator. This control signal is delivered as a single-wire Sigma-Delta (Σ/Δ) signal.

The initial error in the frequency of the local oscillator can be several times the carrier spacing; the measurement of the frequency error relies on the continual pilot carriers. The measurement range is $\pm$ 51.7 kHz in the 8k mode and $\pm$ 143 kHz in the 2k mode. The oscillator control signal is derived from the measured frequency error.

The value of the control signal can also be read and initialized through the microprocessor interface, which allows a previously stored value to be used when a channel is selected, making acquisition faster.

2.7.2 Digital Frequency Synchronization

This block uses digital signal processing (DSP) to correct for the tolerance in the frequency of the local oscillator in the tuner. The DSP shifts the frequency of the complex baseband signal so that its center frequency is zero. The shift needs to be accurate to within a small fraction of the carrier spacing so that intercarrier interference is kept to an acceptably low level and so the tracking ability of the channel estimation is not absorbed in correcting for the error in the frequency of the local oscillator.

The block takes the sequence of complex numbers from the output of the FFT block and produces a numerical control signal. It also takes the sequence of complex numbers from the real-to-complex conversion block and applies the frequency shift to the numbers according to the numerical control signal. Then, it passes the data on to the FFT block.

The digital frequency synchronization block comprises two parts: one to shift the frequency of the complex baseband signal, and one to measure the error in the center frequency of the complex baseband signal as presented to the FFT block.

Multiplying the signal by a rotating vector shifts the frequency of the complex baseband signal. A number-controlled oscillator (NCO) with sine and cosine outputs generates the rotating vector. The frequency range of the NCO is $\pm$ 143 kHz.

The error in the frequency of the local oscillator translates directly into an error in the center frequency of the complex baseband signal. The range of measurement is $\pm$ 51.7 kHz in the 8 k mode, and $\pm$ 143 kHz in the 2 k mode. The numerical control signal is derived from the measured frequency error.

Use the microprocessor interface to read and initialize the value of the control signal. This allows a previously stored value to be used when a channel is selected, thus making acquisition faster.

2.7.3 AFC Loop Gain

In digital AFC mode, the optimal sensitivity (KSENS) is when the AFC_SENSITIVITY field in the Parameter Registers (see page 4-18) is set to 0b110:

Equation 2.11 $K_{SENS} \approx 1.56 \times 10^{-2}$

In analog AFC mode, the optimal AFC_SENSITIVITY is defined as:

Equation 2.12 $K_{SENS} = \frac{74.4}{K_{VCXO}}$

2.7.4 AFC_INIT_FREQ Register Definition

In AFC digital loop mode, the AFC_INIT_FREQ register is defined as a two's complement 24-bit register with the following usage:

Equation 2.13 $$W_i = W_0 + \left(\frac{143 \times 10^3}{2^{23}} \times \text{AFC\_INIT\_FREQ} \right)$$

where W_0 is the central frequency of the VCXO.

In AFC analog loop mode, the AFC_INIT_FREQ register is defined as a two's complement 24-bit register and in the L64780 has the following usage:

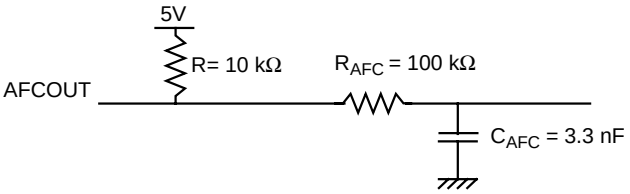
Equation 2.14 $$W_i = W_0 + \left(\frac{5K_{vcxo}}{2^{20}} \times \text{AFC\_INIT\_FREQ} \right)$$

where W_0 is the frequency of the VCXO.

2.7.5 AFC External Loop Filter

The control signal of the frequency loop drives the Sigma-Delta modulated output AFCOUT. Use the AFCOUT signal to drive an external passive RC filter that feeds the timing clock control stage, as shown in Figure 2.5.

Figure 2.5 AFC Loop Pass Filter



The –3 dB cutoff frequency of this circuit is f_0 = 482 Hz, giving a rough estimate of the Frequency Loop Bandwidth and resulting in a low-pass filter time constant:

Equation 2.15 $$T_1 = RC = 300\ \mu s$$

The R and C values for the low-pass filter must meet the requirement shown in Equation 2.16:

Equation 2.16 $R_{AFC} \cdot C_{AFC} = 330\ \mu s$

2.8 TPS Decoding and Frame Synchronization

This block takes the sequence of complex numbers from the output of the FFT block and recovers the Transmission Parameter Signalling (TPS) data defined in paragraph 4.6 of the DVB-T/ETSI specification. The block passes the resulting data to the control logic of the L64780; it thus configures the mode of operation of much of the demodulator's circuitry.

The TPS data contains information on:

- The modulation system
- Whether the transmission is hierarchical
- What the value of α is (if the transmission is hierarchical)
- The inner code rate(s)
- The guard interval
- The mode: 2 k or 8 k

The guard interval and mode interaction cannot be used for acquisition, but assist the receiver in handling a reconfiguration of the transmission.

By implication, the TPS also indicates the phase of the four-symbol sequence of insertion of scattered pilots.

The TPS Decoder extracts the data bits from the TPS carriers and retains the most recent 67 bits. The decoder detects the start of the frame and carries out the Bose-Chaudhuri-Hocque (BCH) error check on the block of 67 bits, so that data containing errors can be discarded. All the data in the list above are passed to the control logic along with two flags: one indicates the start of a frame; the other indicates whether the error check detects errors. If there were no errors, the control logic uses the data to configure the demodulator, discarding any previous settings. The settings can be read and initialized through the microprocessor interface, which allows previously stored settings to be used when a channel is selected, making acquisition faster.

2.9 Mode Control Logic

If previously stored mode data are available, they are used when a channel is selected or when the signal strength rises after a period of signal loss. This is done by the means of an external microprocessor and makes acquisition faster. When the Mode Control Logic becomes an error-free TPS block, mode data from that TPS block replaces any previously determined mode data.

In this context, the mode data consists of:

- 2 k or 8 k mode
- Length of the guard interval
- Modulation system
- Hierarchy information
- Inner code rate

The mode control logic configures all the demodulator blocks whose operation is affected by these parameters. Acquisition of the demodulator is outlined in the following steps:

1. Achieve full synchronization of the FFT start and the clock frequency.
2. Make coarse and fine automatic frequency control (AFC) corrections, and achieve frequency synchronization.
3. Equalize the channel frequency response, once the Symbol Number is zero.
4. Wait up to one frame for the start of a TPS block, and wait another frame for the complete TPS block to be received. There is a wait of one or more additional frames, if necessary, until a TPS block is received without errors.
5. The modulation system, hierarchy information, and code rate from the TPS data are used to configure the Viterbi metric assignment block, and, by means of the microprocessor interface, the external Viterbi decoder(s).

2.10 Channel Estimation and Equalization

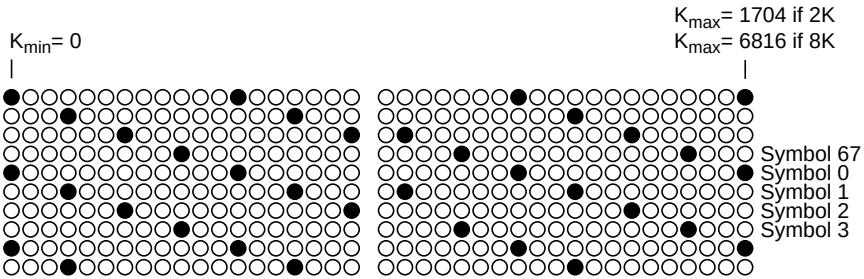
The output from the FFT block is a sequence of complex numbers, each describing the signal received on one of the COFDM carriers. The numbers correspond to the values, chosen from the points of the current constellation, which were used to modulate each carrier at the modulator. However, each carrier is received with unknown amplitude and phase due to the combined effects of:

- The channel through which the RF signal has passed (which, in general, is frequency selective)
- Any minor error in the FFT timing window

The purpose of the channel estimation and equalization block is to correct these effects so that the complex numbers at its output would, if plotted on an Argand diagram, correspond to points of the transmitted constellation (for example, QPSK, 16 QAM, or 64 QAM) except for any superimposed noise or interference.

The transmitted DVB-T signal contains “scattered pilots,” which are distributed among the data cells in a regular pattern (see Figure 2.6). These are transmitted with known values: the imaginary part is always zero, while the real part has a fixed amplitude. The sign of the real part, however, is determined by the carrier number (according to a pseudo-random function that also is used in a similar way to determine the real part of continual pilots).

Figure 2.6 Scattered Pilot Structure



The Channel Estimation and Equalization Block compares each received scattered-pilot cell with the known transmitted value (derived from a

PRBS generator) to obtain a snapshot of the response of the “channel” (including any timing uncertainty) for the corresponding carrier at that time instant.

The data cells that must be corrected lie between the scattered pilots, in both frequency and time. This allows for appropriately generated corrections for each data cell by using a suitable form of interpolation applied to the measured values of the scattered pilots. As well as obtaining “in-between” values of the channel response, the interpolator also slightly reduces the effects of thermal noise on the scattered-pilot measurements. The reduction in noise and the fact that scattered pilots are transmitted with a power approximately 2.5 dB greater than data cells, keeps the inevitable loss of performance due to scattered-pilot noise within acceptable bounds.

2.11 Viterbi Metric Assignment and Quantization

This block takes in the sequence of complex numbers, each describing the signal received on one of the COFDM carriers, after equalization. These are the received versions of the complex numbers chosen at the modulator from the points of the current constellation, according to the coded bits to be sent. This block forms Viterbi metrics (“soft decisions”) for each of the received bits. These metrics are quantized and passed on, after reordering in the deinterleaver stages, to the associated Viterbi convolutional decoder. The use of “soft” rather than “hard” decisions is vital to obtaining the rugged properties of COFDM.

The associated Viterbi convolutional decoder, which resides on a separate chip (for example, the LSI Logic L64724), is capable of accepting soft decisions that are quantized to either three or four bits. Three bits are required for acceptable performance, while four bits improve the performance for higher-order modulation options of the DVB-T specification, especially with non-uniform constellations. Decoder chips designed primarily for QPSK or BPSK modulation commonly use three bits because the advantage of using four bits is minimal.

The L64780 chip provides 4-bit soft decisions, but it also can be used to drive 3-bit decoders.

2.12 Symbol Deinterleaver

From each received constellation point, the Viterbi metric assignment block extracts up to six soft decisions. The symbol deinterleaver accepts one COFDM symbol containing soft decisions and reorders them according to an algorithm defined in the DVB-T specification. It then passes this reordered data to the bit deinterleaver.

Echoes cause minima (“holes”) in the received spectrum, leading to groups of carriers on which the data is unreliable. For optimum operation of the Viterbi decoder, these groups of unreliable carriers must be split up. The symbol deinterleaver fulfills part of this function; the remainder is done by the bit deinterleaver.

In 2 k mode, there are 1705 COFDM carriers, of which 1512 in each symbol carry data. Each of these carriers yields either 2 (QPSK), 4 (16 QAM), or 6 (64 QAM) soft decisions. Each of these soft decisions consists of four bits of information. The effect of the operation of the symbol deinterleaver is to write the possible 1512 24-bit words into a RAM using one address sequence, and to read them using a different address sequence. This means there is a delay of one COFDM symbol between the input and the output. In the 8 k case, there are 6048 (out of a total of 6817) COFDM carriers that convey data; thus, the L64780 provides a 6048 by 24-bit RAM.

2.13 Bit Deinterleaver

In the presence of multipath or interference, some COFDM carriers convey data less ruggedly than others. Each COFDM carrier supplies either two, four, or six soft decisions; these would be impaired if the carrier they came from were impaired. For optimum operation of the Viterbi decoder, it is best if groups of unreliable soft decisions are maximally spaced. The purpose of the bit deinterleaver is to split up unreliable soft decisions caused by a single unreliable COFDM carrier. The symbol deinterleaver separates groups of unreliable COFDM carriers.

The bit deinterleaver accepts groups of 3-bit or 4-bit soft decisions generated from the same COFDM carrier from the symbol deinterleaver.

The bit deinterleaver rearranges these groups of soft decisions to separate soft decisions generated from the same carrier. The bit deinterleaver passes these soft decisions to the output interface of the L64780 for external decoding.

There are 6-bit deinterleavers, I0 to I5. For QPSK, one COFDM carrier provides two soft decisions: one from the real part, and one from the imaginary part. I0 deinterleaves the soft decision extracted from the real part; I1 deinterleaves the soft decision from the imaginary part. In this case, I2 to I5 are not used.

For 16 QAM (both hierarchical and nonhierarchical), one COFDM carrier provides four soft decisions: two from the real part, and two from the imaginary part. Ten deinterleaves the MSB soft decision extracted from the real part; I1 deinterleaves the MSB from the imaginary part. I2 deinterleaves the LSB from the real part; I3 deinterleaves the LSB from the imaginary part. In this case, I4 and I5 are not used.

For 64 QAM (both hierarchical and nonhierarchical), one COFDM carrier provides six soft decisions: three from the real part, three from the imaginary part. I0 deinterleaves the MSB soft decision extracted from the real part; I1 deinterleaves the MSB from the imaginary part. I2 deinterleaves the CSB from the real part; I3 deinterleaves the CSB from the imaginary part. I4 deinterleaves the LSB from the real part; I5 deinterleaves the LSB from the imaginary part.

Chapter 3
Interfaces

This chapter describes the interfaces for the LSI Logic L64780 DVB-T COFDM Demodulator. It consists of the following sections:

3.1 Output Interface

The output interface formats the soft decisions for presentation to the downstream Viterbi decoder. The input to this block is a stream of four-bit or 3-bit Viterbi soft decisions from the inner bit deinterleaver. The output from this block connects to a Viterbi decoder that is external to the L64780. The output from soft decisions is in a format suitable for direct connection to the L64724 or L64705.

This block operates differently in nonhierarchical and hierarchical modes, and can have a serial or parallel output format. This block’s operational modes are described in the following subsections.

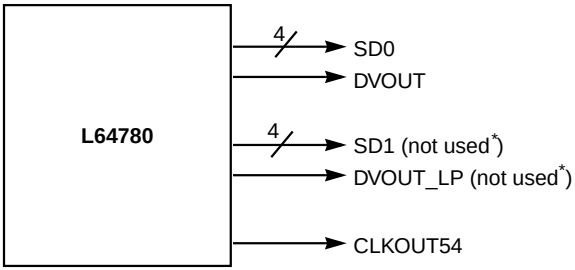
3.1.1 Output Format in Nonhierarchical Mode

In nonhierarchical mode, the output format can be serial or parallel.

3.1.1.1 Serial Output Format

In serial output mode, the output port of the L64780 is configured as shown in Figure 3.1.

Figure 3.1 Output Interface in Nonhierarchical and Serial Modes

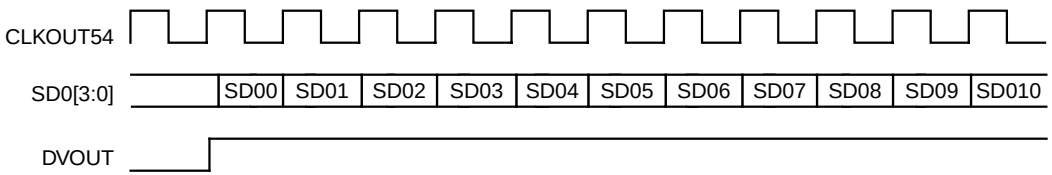


* When not used, the signal is deasserted LOW.

The output interface passes 4-bit or 3-bit soft decisions to the Viterbi decoder through the SD0 signal accompanied by the assertion of DVOUT. All outputs from the output interface are clocked at 54 MHz by CLKOUT54.

With a 64 QAM constellation, the L64780 extracts six soft decisions from every constellation point at 9 MHz; for example, one soft decision is presented every 54 MHz clock cycle. See Figure 3.2.

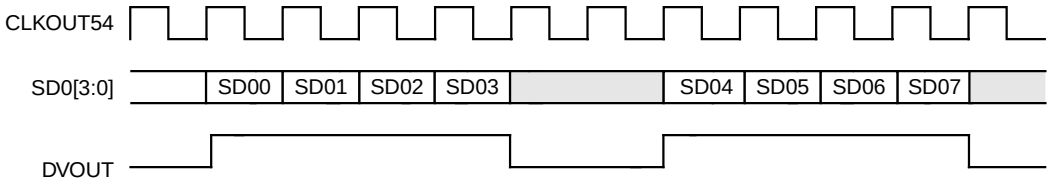
Figure 3.2 Nonhierarchical, Serial Mode, 64 QAM Constellation



Every time a set of soft decisions is received from the bit deinterleaver, the DVOUT signal stays asserted for six 54 MHz clock cycles. The DVOUT signal is deasserted only during the scattered pilots, unused carriers, or guard interval.

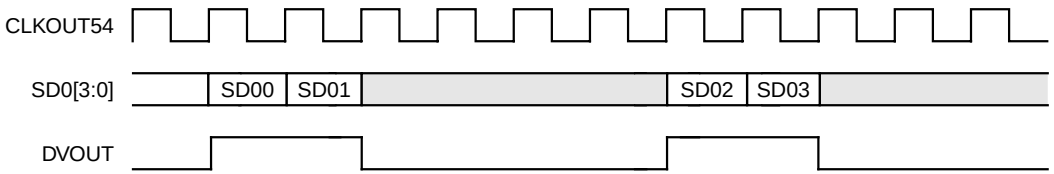
For a 16 QAM constellation, during which four soft decisions are extracted every 9 MHz, the DVOUT signal stays asserted over four out of six 54 MHz clock cycles. See Figure 3.3.

Figure 3.3 Nonhierarchical, Serial Mode, 16 QAM Constellation



For the QPSK constellation, only two soft decisions are extracted every 9 MHz, resulting in DVOUT being asserted over two out of six 54 MHz clock cycles. See Figure 3.4.

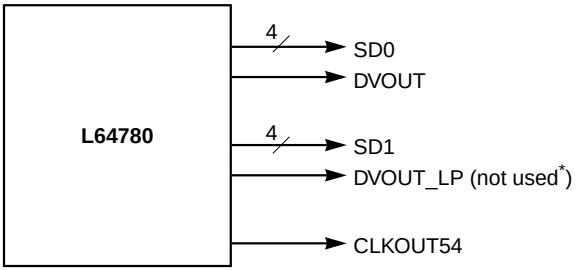
Figure 3.4 Nonhierarchical, Serial Mode, QPSK Constellation



3.1.1.2 Parallel Output Format

In this mode, soft decisions are output in parallel, and the output interface of the L64780 is configured. See Figure 3.5.

Figure 3.5 Output Interface in Nonhierarchical and Parallel Modes

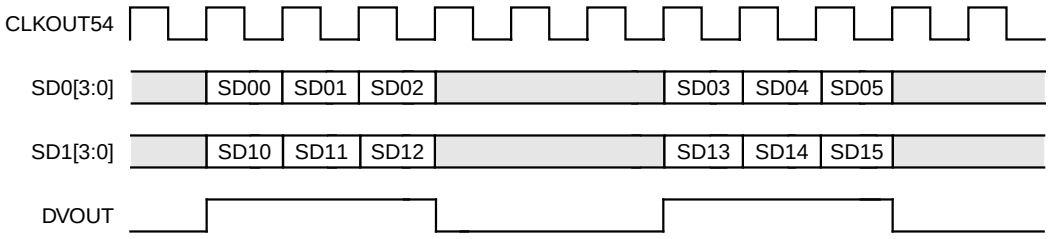


* When not used, the signal is deasserted LOW.

The output interface passes two soft decisions to the Viterbi decoder in parallel through SD0 and SD1, accompanied by a data valid indicator.

Because soft decisions are presented in parallel in 64 QAM, the soft decisions are presented in three consecutive 54 MHz clock cycles over a six 54 MHz clock cycle period (Figure 3.6). The DVOUT signal is deasserted during the scattered pilots, unused carriers, and guard interval.

Figure 3.6 Nonhierarchical, Parallel Mode, 64 QAM Constellation



When a 16 QAM constellation is used, DVOUT is asserted for two 54 MHz clock cycles in six clock cycles (Figure 3.7). When QPSK is used, it is asserted for only one out of six clock cycles (Figure 3.8).

Figure 3.7 Nonhierarchical, Parallel Mode, 16 QAM Constellation

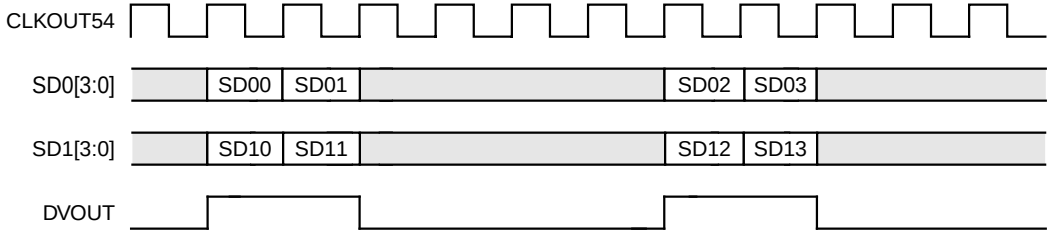
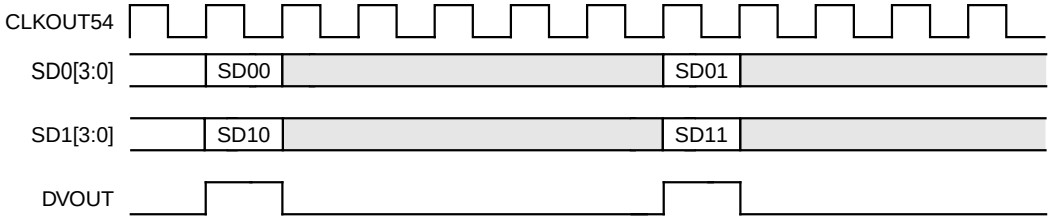


Figure 3.8 Nonhierarchical, Parallel Mode, QPSK Constellation



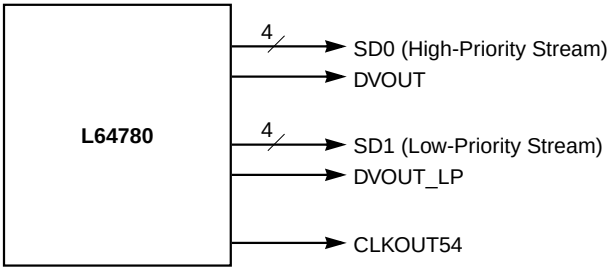
3.1.2 Output Format in Hierarchical Mode

The following subsections describe the decoding of High-Priority and Low-Priority data streams in hierarchical mode.

3.1.2.1 Decoding of HP and LP Streams

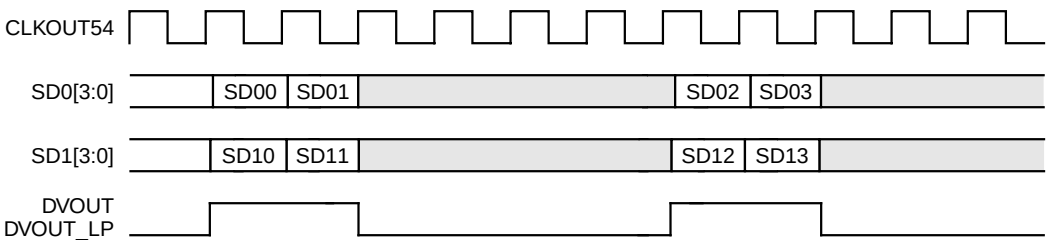
In hierarchical mode, the output port of the L64780 is configured (Figure 3.9). The High- and Low-Priority streams are delivered on SD0 and SD1, respectively. DVOUT validates the High-Priority data stream; DVOUT_LP validates the Low-Priority data stream.

Figure 3.9 Output Interface in Hierarchical and Two FECs Modes



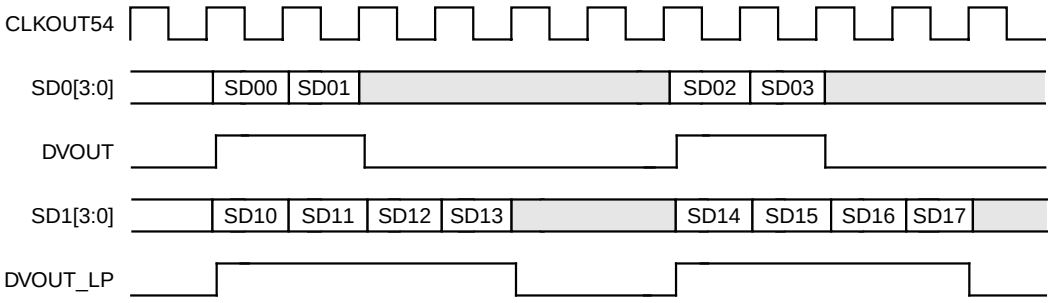
When in 16 QAM mode, two soft decisions are transmitted on SD0 and SD1. DVOUT and DVOUT_LP stay asserted for two of six 54 MHz clock cycles. See Figure 3.10.

Figure 3.10 Hierarchical, Two FEC Decoders, 16 QAM Constellation



When in 64 QAM mode, two soft decisions are transmitted on SD0 and four soft decisions are transmitted on SD1. The DVOUT signal stays asserted during two 540 MHz clock cycles over six 54 MHz clock cycles and the DVOUT_LP signal stays asserted for four of six 54 MHz clock cycles. See Figure 3.11.

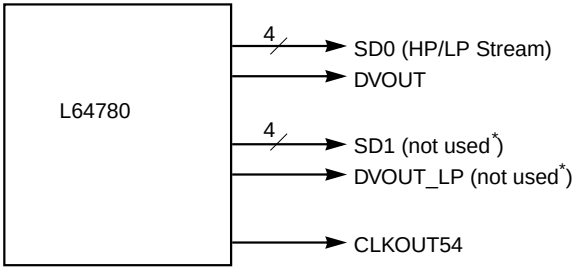
Figure 3.11 Hierarchical, Two FEC Decoders, 64 QAM Constellation



3.1.2.2 Decoding Only One Stream (HP or LP)

In this mode, the output port of the L64780 is configured (Figure 3.12). The DOF_HPLP signal selects between the HP and LP output streams. The data stream in this output format is the same as for the nonhierarchical case.

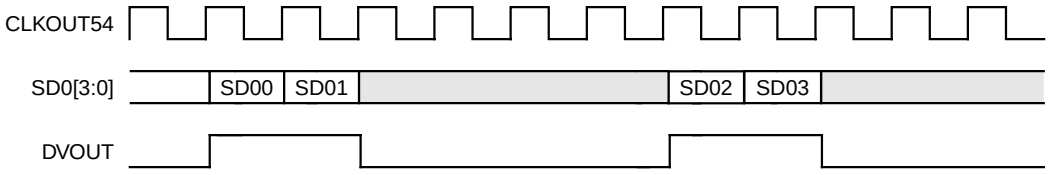
Figure 3.12 Output Interface in Hierarchical and One FEC Mode



* When not used, the signal is deasserted LOW.

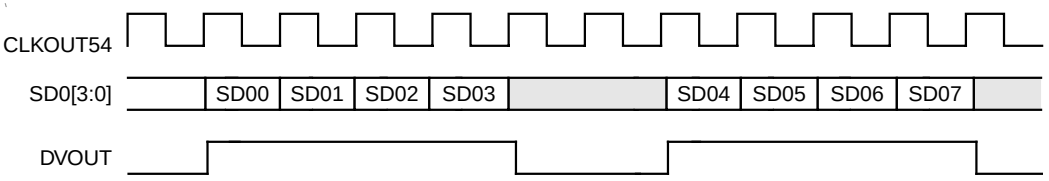
When a set of soft decisions is received from the Bit Deinterleaver block in 16 QAM (HP or LP selected) or in 64 QAM (only HP selected), two soft decisions are transmitted over SD0. The result is that DVOUT is asserted for two of six 54 MHz clock cycles. See Figure 3.13.

Figure 3.13 Hierarchical, One FEC Decoder Mode With 16 QAM (HP or LP Selected) or 64 QAM (LP Selected only)



When a set of soft decisions is received from the Bit Deinterleaver block, and the DOF function is configured in 64 QAM with the LP data stream selected, four consecutive soft decisions must be transmitted over SD0. Thus, DVALIDOUT is asserted for four of six 54 MHz clock cycles. See Figure 3.14.

Figure 3.14 Hierarchical, One FEC Decoder Mode With 64 QAM (HP Selected Only)



3.2 MUXIN Interface

The MUXIN bus lets you enter data (or test vectors) into the device at specific locations, which lets you bypass some front functional blocks and test an internal functional block.

Important: This interface is used for LSI Logic internal testing and is not intended for use in customer production receivers.

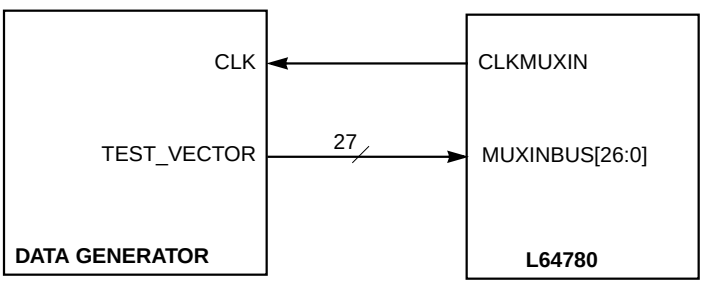
The MUXIN bus (MUXINBUS) is a 27-bit wide bus, multiplexed with the bypass ADC bus (DIGADCIN[9:0]). Table 3.1 shows the bus mapping.

Table 3.1 MUXINBUS Mapping

MUXINBUS[26:10]	MUXINBUS[9:0]
MUXIN[16:0]	DIGADCIN[9:0]

Clocking data into the chip is very simple because the L64780 offers a clock output (CLKMUXIN) that automatically has the correct phase and frequency. CLKMUXIN automatically selects the correct internal clock, depending on the block selected. Figure 3.15 shows how to connect external logic that brings the data to the MUXINBUS.

Figure 3.15 MUXIN Signals Interface



The MUXINBUS is software controlled and provides six testing possibilities. The control word is MUXIN_select[2:0], located at address 0x15, mapped on bits 3 to 5. Table 3.2 defines the MUXIN_select[2:0] word.

Table 3.2 MUXIN Conifguration

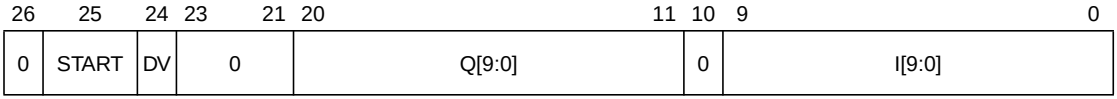
MUXIN_select[2:0]	Definition
0	Normal mode
1	Access to Timing and DDFS block
2	Access to AFC block
3	Access to FFT block
4	Access to CSI block
5	Input to SDI block
6	Reserved
7	Reserved

3.2.1 Access to Timing and DDFS Blocks

When selecting access to the Timing and DDFS blocks, the CLKMUXIN signal is configured as an 18 MHz clock (more precisely, four times the low IF). The DDFS block is the digital rotator that performs the carrier frequency compensation.

The signals on the bus are I and Q data (in two's complement format), a start pulse (START), and a data valid signal (DV). These signals are mapped on the MUXINBUS. See Figure 3.16.

Figure 3.16 Timing and DDFS Input Mapping



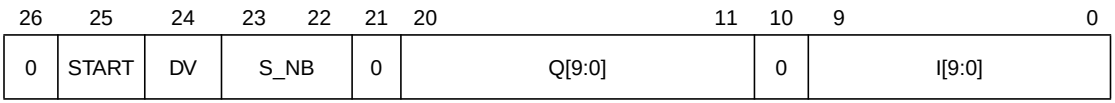
In this mode, you can select whether the start pulse comes from the MUXINBUS or from the Timing recovery unit. The start pulse delimits every COFDM symbol. This selection is done through the DDFS_MODE bit (address 0x9, bit 1). If DDFS_MODE = 0, the start pulse comes from the test bus (test mode); otherwise, the Timing block delivers the start pulse. Note that this mode could correspond to an external down-converter that feeds the I and Q data directly into the Timing and DFFS blocks.

3.2.2 Access to the AFC Block

The AFC block performs the estimation of the carrier frequency drift and produces an analog or digital feedback control signal to compensate for this drift. In this mode, the CLKMUXIN signal is configured as a 36 MHz clock (more precisely, eight times the low IF).

The signals on the bus are I and Q data (in two's complement format), a start pulse (START), a data valid (DV) signal, and the COFDM symbol number (S_NB). These signals are mapped on the MUXINBUS. See Figure 3.17.

Figure 3.17 AFC Input Mapping



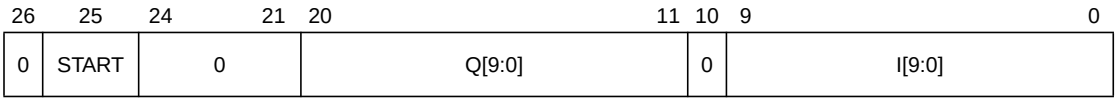
In this mode, you can select whether the COFDM symbol number comes from the TPS informations (Frame Number) or from the MUXINBUS (S_NB). This selection is done through the AFC_MODE bit (address 0x5, bit 6). If AFC_MODE = 0, the COFDM symbol number comes from the MUXINBUS (S_NB) or full MUXIN mode; otherwise, it comes from the TPS register (partial MUXIN mode).

3.2.3 Access to the FFT Block

In this mode, the CLKMUXIN signal is configured as a 36 MHz clock (more precisely, eight times the low IF).

The signals on the bus are I and Q data (in two's complement format) and a start pulse (START). These signals are mapped on the MUXINBUS. See Figure 3.18.

Figure 3.18 FFT Input Mapping



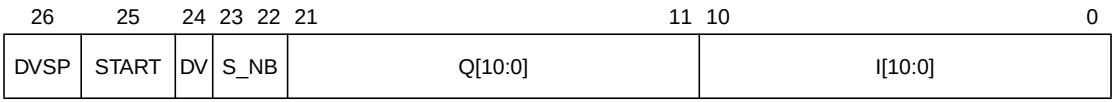
In this mode, the L64780 can be used as a stand-alone FFT processor in forward mode (FFT_DIR = 0) or in inverse mode (FFT_DIR = 1). The FFT_DIR register is located at address 0x11, bit 2.

3.2.4 Access to the CSI Block

The CSI block performs the Channel State Information (CSI) processing, which builds the soft decisions for the Viterbi decoder using *a priori* information from the Channel Equalizer (CE). In this mode, CLKMUXIN is configured as an 18 MHz clock (more precisely: four times the low IF).

The signals on the bus are I and Q data (in twos complement format), a start pulse (START), a data valid (DV) signal, the COFDM symbol number (S_NB), and a marker (or data valid) on scattered pilots (DVSP). These signals are mapped on the MUXINBUS. See Figure 3.19.

Figure 3.19 CSI Input Mapping

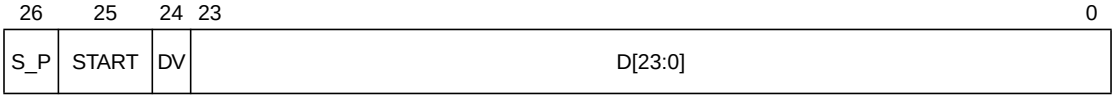


3.2.5 Access to the SDI Block

The SDI block performs Symbol Deinterleaving (SDI) as specified in the ETSI specification. In this mode, the CLKMUXIN signal is configured as an 18 MHz clock (more precisely, four times the low IF).

The signals on the 24-bit data bus (D) contain up to six soft decisions, up to four bits per soft decision, a start pulse (START), a data valid (DV) signal, and the symbol parity (S_P). An odd symbol number is marked by S_P = 1; even symbol numbers are marked by S_P = 0. These signals are mapped on the MUXINBUS. See Figure 3.20.

Figure 3.20 SDI Input Mappings



The data bus (D) is mapped in 3-bit and 4-bit soft decision modes, as shown in Figure 3.21 and Figure 3.22, respectively. The MSB is at the highest weight position. Note that X means reserved.

Figure 3.21 D[23:0] Bus Mapping in Three-Bit Soft Decision

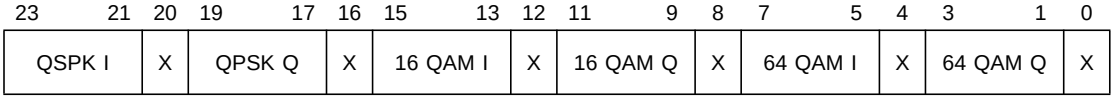
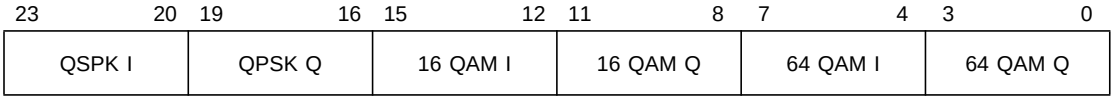


Figure 3.22 D[23:0] Bus Mapping in Four-Bit Soft Decision



3.3 MUXOUT Interface

The MUXOUT bus lets you probe any point in the device while receiving a transport stream (TS).

Important: This interface is used for LSI Logic internal test purposes and is not intended for customer production receivers.

MUXOUTBUS is 27 bits wide. For each probed point, data and control signals are available on this bus (including the clock). The clock has the same aspect ratio as CLKMUXIN; it is not a 50% duty cycle type.

Software controls the MUXOUTBUS, which provides five test possibilities. The control word is MUXOUT_select[2:0], located at address 0x15 (bits 2 to 0). Table 3.3 define the MUXOUT_select word.

Table 3.3 MUXOUT_select Word Definition

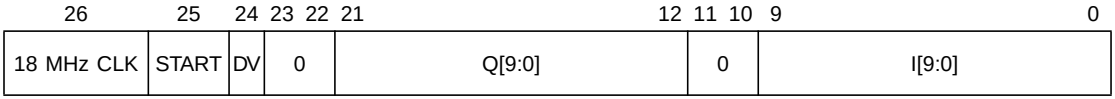
MUXIN_select[2:0]	Definition
0	DDFS output
2	AFC output
3	CE output
4	CSI output
5	ADC output
6	Reserved
7	Reserved

Note that the MUXOUT bus can be 3-stated by asserting the MUX_CTRL bit (bit 3 of the Mode Register Address Line), at address 0x19. The bus is active when MUX_CTRL is set to 0.

3.3.1 DDFS Output

The DDFS output lets you probe signals after carrier frequency compensation and prior to FFT processing. The signals are I and Q data (in two's complement format), a start pulse that delimits the COFDM symbols (START), a data valid (DV) signal that accompanies valid data, and an 18 MHz clock. These signals are mapped on the MUXOUTBUS. See Figure 3.23.

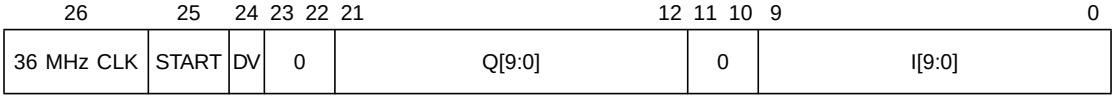
Figure 3.23 DDFS Output Mapping



3.3.2 FFT Output

The FFT output lets you probe data prior to Common Phase Error (CPE) correction and Channel Equalization (CE). The signals are I and Q data (in two's complement format), a start pulse that delimits the COFDM symbols (START), a data valid (DV) signal that accompanies valid data, and a 36 MHz clock. These signals are mapped on the MUXOUTBUS. See Figure 3.24.

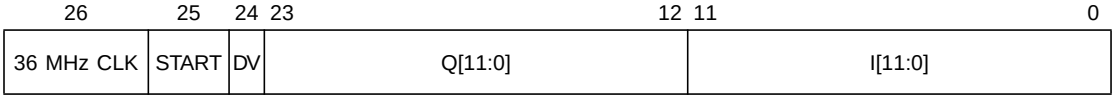
Figure 3.24 FFT Output Mapping



3.3.3 AFC Output

The AFC output lets you probe data after Common Phase Error (CPE) correction and prior to Channel Equalization (CE). The signals are I and Q data (in two's complement format), a start pulse that delimits the COFDM symbols (START), a data valid (DV) signal that accompanies valid data, and a 36 MHz clock. These signals are mapped on the MUXOUTBUS. See Figure 3.25.

Figure 3.25 AFC Output Mappings

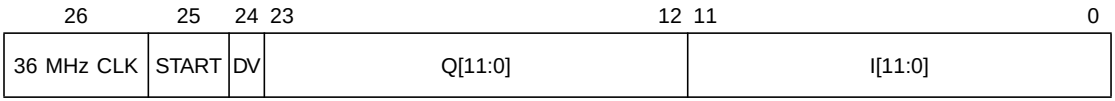


3.3.4 Channel Equalizer (CE) Output

The Channel Equalizer (CE) output lets you probe data after channel equalization or the frequency response of the channel. After channel equalization, you can display the constellation by feeding I and Q data into two DACs. For constellation display purposes, the DACs require only 8-bit resolution.

The signals at this point are I and Q data in two's complement format, a start pulse that delimits the COFDM symbols (START), a data valid (DV) signal that accompanies valid data, and a 36 MHz clock. These signals are mapped on the MUXOUTBUS. See Figure 3.26.

Figure 3.26 CE Output Mappings



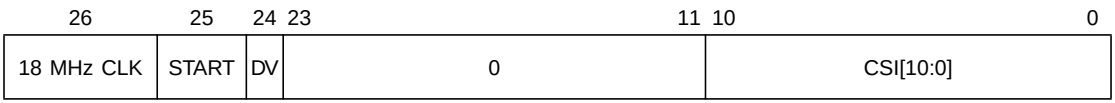
The I and Q data available on the bus represent either the equalized data or frequency response of the channel depending upon the CE_SELECT bit (address 0x11, bit 3). When CE_SELECT = 0, equalized data are present on the MUXOUT bus; otherwise, the MUXOUT bus contains the channel response in the frequency domain.

3.3.5 CSI Output

The CSI output provides an averaged measure per carrier on the confidence to be placed on the hard decision.

The signals present at this point are the degree of confidence (CSI), a start pulse that delimits the COFDM symbols (START), a data valid (DV) signal that accompanies valid data, and an 18 MHz clock. These signals are mapped on the MUXOUTBUS. See Figure 3.27.

Figure 3.27 CSI Output Mappings

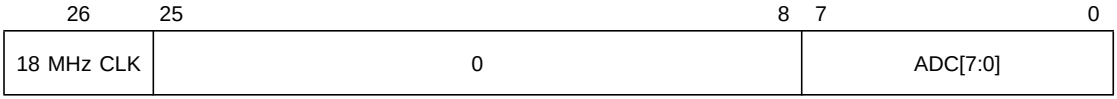


A high value on the CSI bus indicates a low level of confidence, and vice-versa. The CSI word is nonsigned data, which can be used to drive a bar graph representing the quality of reception in a channel.

3.3.6 ADC Output

The ADC output lets you probe the internal ADC. The signals are the digitized input samples (ADC) and the 18 MHz clock. These signals, which are in two's complement format, are mapped on the MUXOUTBUS. See Figure 3.28.

Figure 3.28 ADC Output Mapping



3.4 Microprocessor Interface

The microprocessor interface operates in Serial Mode.

Important: A Parallel mode interface is provided for test purposes. This interface is used for LSI Logic internal testing and is not intended for use in customer production receivers.

The Serial Bus mode interface is a serial interface operating in slave mode. Its protocol is compatible with I^2C specifications. For a more detailed description of the Serial Bus, see Appendix A. The P_S input signal selects either the serial or parallel mode. Table 3.4 summarizes the different modes.

Table 3.4 Mode Selection Using the P_S Input Signal

P_S	Mode	Notes
Low	Parallel	LSI Internal use only
High	Serial	L64780 Serial Interface

When in Serial interface mode, D0 is used as a serial data signal, and A0 is used as a serial clock signal. D[7:1] are used to set the serial bus slave address. When using the serial bus, D[7:1] must be hardwired to set the appropriate device slave address.

Chapter 4
Register Descriptions

This chapter provides an overview of the L64780 register space and gives a detailed description of its registers. This chapter consists of the following sections:

4.1 Memory Map

Table 4.1 lists all L64780 registers and provides the DTTV demodulator internal memory map. A description of each of these registers groups is provided in the following sections.

Table 4.1 L64780 Registers and Internal Memory Map

Space	Address	Register name	Register Width (Bits)	Type
1	0x00	Interrupt register	2	R
	0x01	Interrupt Mask register	2	R/W
	0x02	TPS register 1	4	R/W
	0x03	TPS register 2	6	R/W
	0x04	TPS register 3	7	R/W
	0x05	Parameters register 1	8	R/W
	0x06	Parameters register 2	8	R/W
	0x07	Parameters register 3	8	R/W
	0x08	Parameters register 4	8	R/W

Table 4.1 L64780 Registers and Internal Memory Map (Cont.)

Space	Address	Register name	Register Width (Bits)	Type
2	0x09	Parameters register 5	8	R/W
	0x0A	Parameters register 6	8	R/W
	0x0B	Parameters register 7	8	R/W
	0x0C	Parameters register 8	8	R/W
	0x0D	Parameters register 9	8	R/W
	0x0E	Parameters register 10	8	R/W
	0x0F	Parameters register 11	8	R/W
	0x10	Parameters register 12	8	R/W
	0x11	Parameters register 13	8	R/W
	0x12	Parameters register 14	3	R/W
	0x13	Parameters register 15	6	R/W
	0x14	Parameters register 16	6	R/W
3	0x15	MUX register	6	R/W
	0x16	Performance Monitoring register 1	6	R/W
	0x17	Performance Monitoring register 2	8	R
	0x18	Performance Monitoring register 3	8	R
	0x19	Mode register	6	R/W
	0x1A	3 Wires register	6	RW

Figure 4.1 through Figure 4.3 give a graphical view of the register address space. Shaded parts in these figures denote reserved bits.

Figure 4.1 Graphical View of the L64780 Register Address Space 1

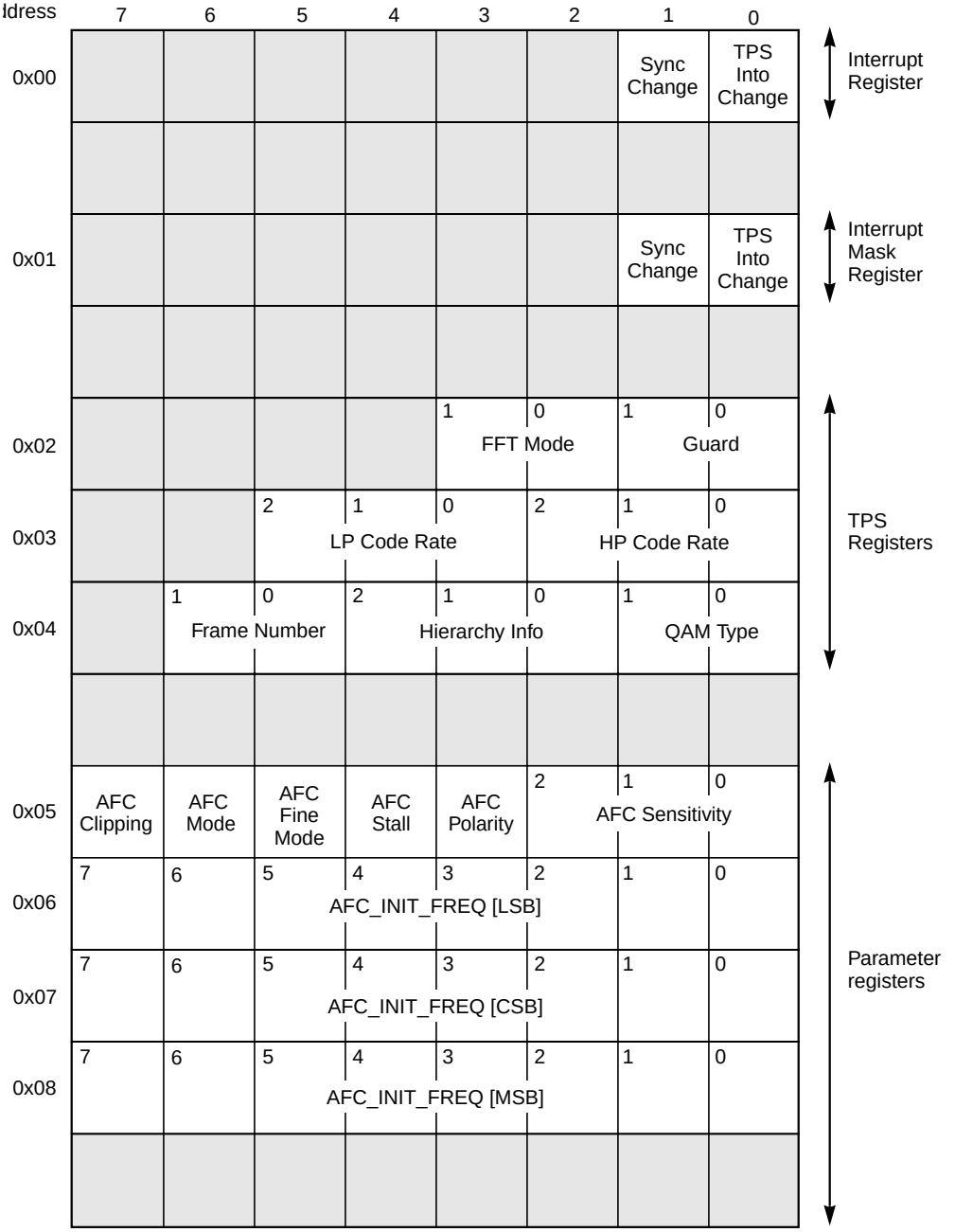


Figure 4.2 Graphical View of the L64780 Register Address Space 2

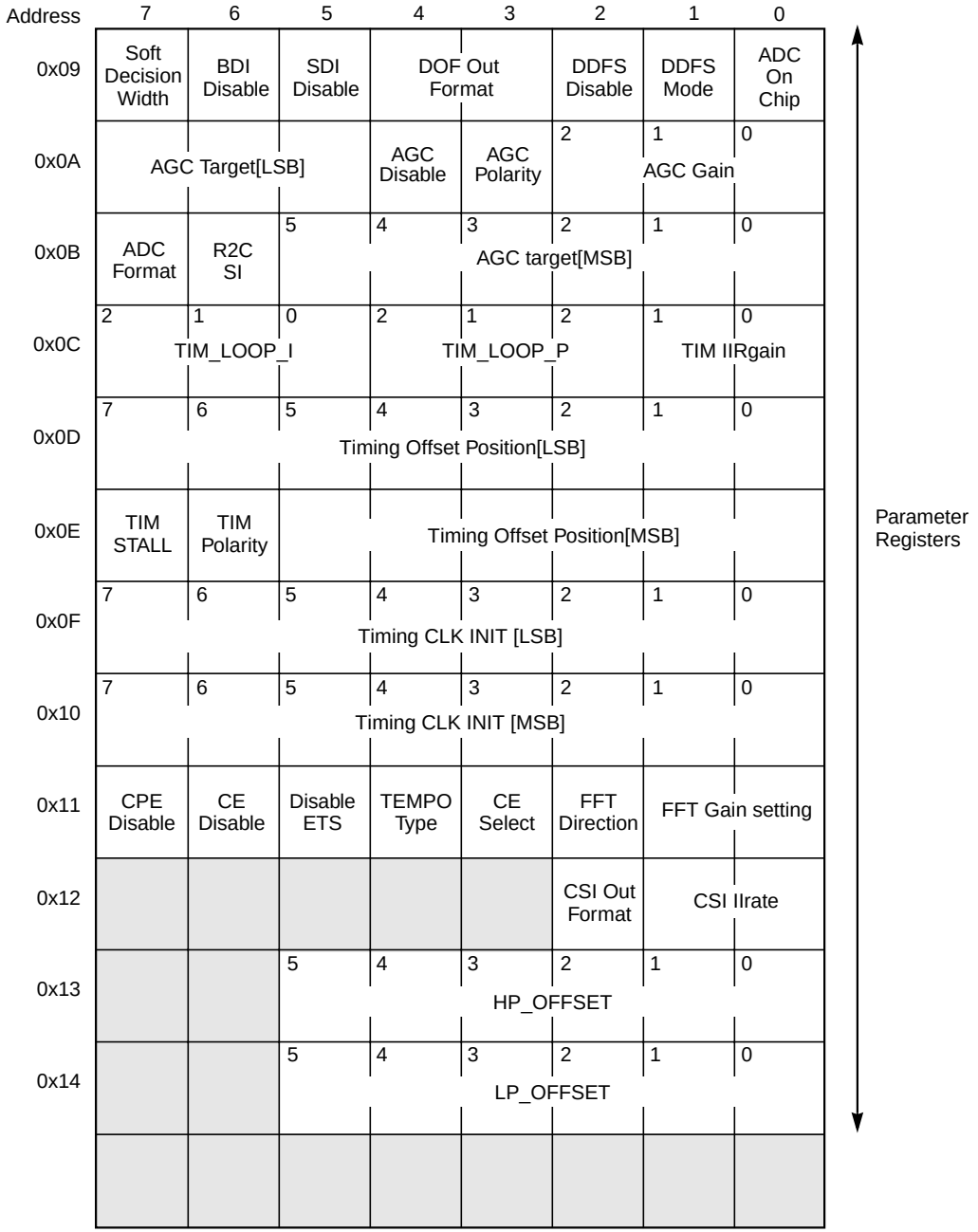
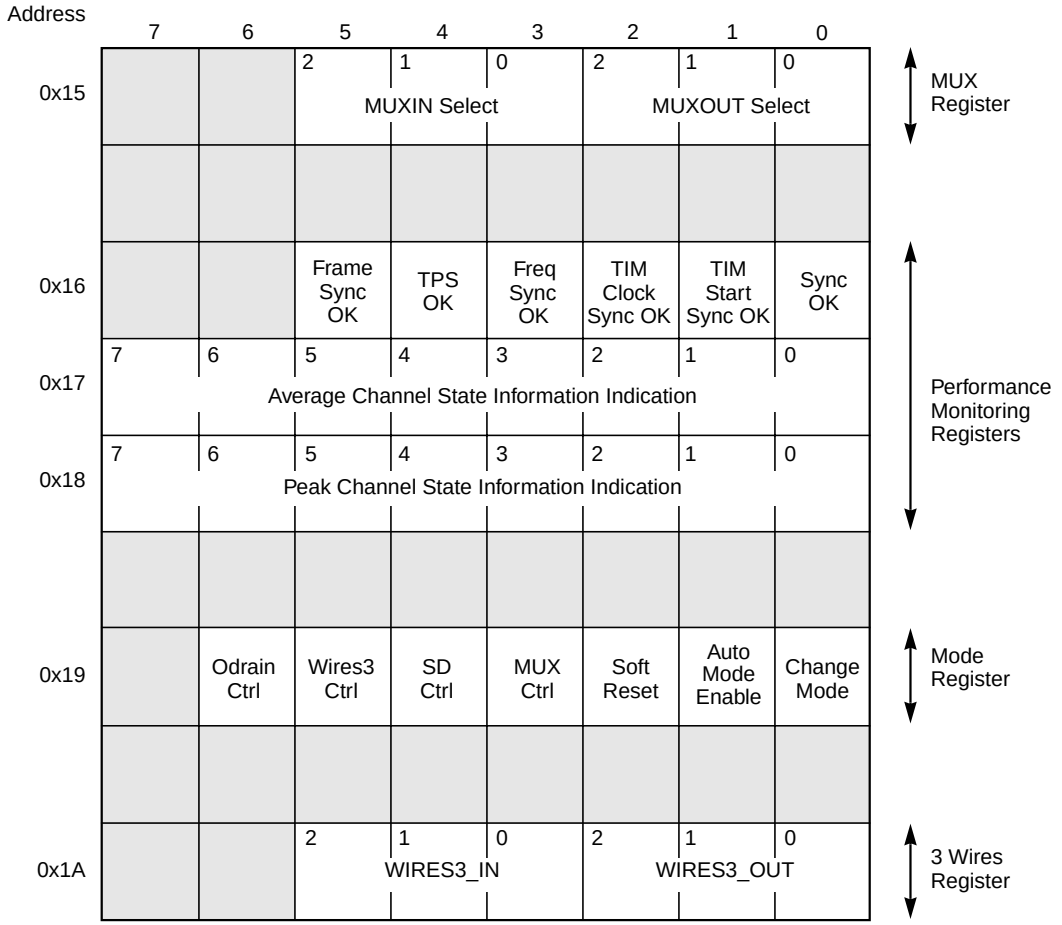


Figure 4.3 Graphical View of the L64780 Register Address Space 3



4.2 Interrupt Registers

The DTTV demodulator generates interrupts based on events in specific functional blocks of the chip. These events are reported to the Interrupt register. Two types of events might be of interest to an external microcontroller:

- Events relating to severe impairments. The external microcontroller must evaluate the severity of these events and take the necessary corrective action.
- Events relating to changes in the operation of the DTTV demodulator. These occur during normal operation and are made available to the external microcontroller for monitoring.

The Interrupt register at address 0x00 provides the microprocessor with events on the DTTV demodulator that can cause an internal interrupt. This read-only register contains a bitmap indicating which events took place. It is associated with the Interrupt Mask register.

4.2.1 Address Line 0x00

	7	2	1	0
0x00	RES		SYNC_CHANGE	TPS_INFO_CHANGE

RES **Reserved** **[7:2]**
These bits are reserved.

SYNC_CHANGE
Synchronization Change Interrupt **R 1**
This bit indicates if one or more aspects of the DTTV demodulator synchronization have changed.

The initial condition for the SYNC_CHANGE bit is 0 (no interrupt). If this bit is set to 1, an interrupt is generated.

The Sync change event is visible through the signal SYNC CHANGE (see Section 4.6, “Performance Monitoring Registers Address Line 0x16”) and occurs when at least one of the following synchronizations has changed during the demodulation:

- The Frame_Sync_OK bit is set to 1 when the frame synchronization is reached and reset to 0 when the frame synchronization is lost. The Frame_Sync_OK bit is visible through the Performance Monitoring register.
- The Freq_Sync_OK bit is set to 1 when the demodulator is frequency locked and reset to 0 when the frequency synchronization is not yet reached or lost. The Freq_Sync_OK bit is visible through Performance Monitoring Register 1.
- The Start_Sync_OK bit is set to 1 when the timing block has properly determined the start of the FFT; it is reset to 0 when this is lost. Start_Sync_OK bit is visible through Performance Monitoring Register 1.
- The Clock_Sync_OK bit is set to 1 when the sampling frequency is properly locked; it is reset to 0 when sync is not reached. Clock_Sync_OK is visible through Performance Monitoring register 1.
- The TPS_Sync_OK bit is set to 1 when the TPS frame is error free; it is reset to 0 when the frame is corrupted. The TPS_Sync_OK bit is visible through Performance Monitoring Register 1.

TPS_INFO_CHANGE

TPS Change Interrupt **R 0**

A valid TPS structure has been received that differs from the current mode of the DTTV demodulator. This interrupt does not occur if the only change is in the frame number.

The TPS_INFO_CHANGE bit is initially reset to 0 (no interrupt). If this bit is set to 1, an interrupt is generated.

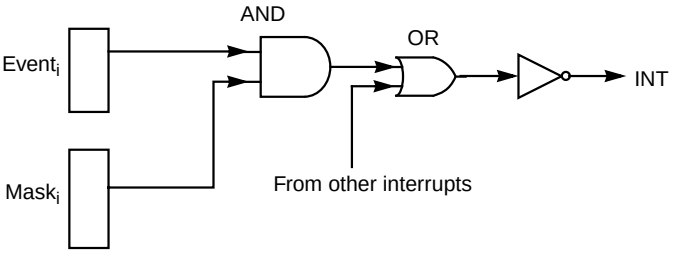
The TPS_INFO_CHANGE bit is set to 1 only when the received error-free (BCH-correct) TPS is different from the last TPS information stored in the TPS registers. This bit is only reset by a microprocessor read access. The TPS_INFO_CHANGE bit is evaluated every COFDM frame, and it is visible through the TPS_INFO_CHANGE signal (see Section 4.3, “TPS Registers”).

4.2.2 Interrupt Mask Register, Address Line 0x01

The microprocessor can select between a polling or interrupt driven approach by programming the Interrupt Mask register. Only when the bit in the Interrupt Mask register associated with the event bit in the Interrupt register is set to 1 is the interrupt for this event is enabled; otherwise, polling is selected.

Any interrupt-related events reported in the Interrupt register lead to the assertion of the INTn signal (active LOW). On receiving an interrupt signal, the microcontroller is expected to read the Interrupt register to identify the cause(s) of this interrupt. The microcontroller thereby resets all interrupt events in the Interrupt register; this remains in effect until a new interrupt (TPS info change or Sync change) occurs. To disable permanently the interrupt mechanism, reset the Interrupt Mask register. Figure 4.4 shows an implementation of the interrupt generation.

Figure 4.4 Interrupt Generation



Note that a read access to Address 0 resets the Interrupt Register. But it does not mask new interrupts that arise at the time the host reads the interrupt register; thus, when the Host reads the interrupt register, each interrupt is either reset, or set again if a new interrupt occurs.

	7	2	1	0
0x01	RES		SYNC_CHANGE_MASK	TPS_INFO_CHANGE_MASK

RES **Reserved** **[7:2]**
These bits are reserved.

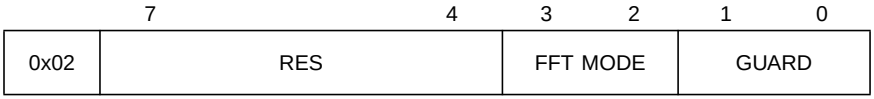
SYNC_CHANGE _MASK
Synchronization Change Interrupt Mask **R/W 1**
This bit enables or disables the generation of an interrupt if one or more aspects of the DTTV demodulator synchronization have changed. If this bit is 0, the interrupt is masked; if the bit is 1, the interrupt is enabled. The initial condition for this bit is 0.

TPS_INFO_CHANGE_MASK
TPS Change Interrupt Mask **R/W 0**
This bit enables or disables the generation of the interrupt for the TPS_INFO_CHANGE bit. If this bit is 0, the interrupt is masked; if the bit is 1, the interrupt is enabled. The initial condition for this bit is 0.

4.3 TPS Registers

These registers have two functions, depending on whether they are read from, or written to. If they are read from, they indicate that the contents of the last TPS structure were correctly received. If they are written to, they set the next mode of operation of the DTTV demodulator. The mode change does not take effect until the CHANGE_MODE command is issued (by setting the CHANGE_MODE bit in the Mode register). The meaning of the bits contained in the TPS are described in the ETSI specification.

4.3.1 Address Line 0x02



RES **Reserved** **[7:4]**
These bits are reserved.

FFTMODE **COFDM Transmission Mode** **R/W [3:2]**
When this register is read, these bits provide the last value received by the channel, using the TPS signalling information.

When the register is written, these bits store the next COFDM transmission mode value that the system uses. The values are:

FFTMODE[1:0]	Definition
00	2 k Mode
01	8 k Mode
10	Unused
11	Unused

The initial condition for the FFTMODE is 0b00 (2k).

GUARD **Guard Interval** **R/W [1:0]**

When this register is read, the Guard Interval provides the last value received by the channel, using the TPS signalling information.

When this register is written, Guard [1:0] stores the next Guard value that the system uses. The values are:

GUARD[1:0]	Definition
00	1/32 Guard Interval
01	1/16 Guard Interval
10	1/8 Guard Interval
11	1/4 Guard Interval

The initial condition for the Guard Interval is 0b00 (1/32).

4.3.2 Address Line 0x03

	7 6	5 3	2 0
0x03	RES	LP_CODE_RATE	HP_CODE_RATE

RES **Reserved** **[7:6]**

These bits are reserved.

LP_CODE_RATE

Viterbi Low-Priority Code Rate **R/W [5:3]**

When this register is read, these bits provide the last value received by the channel, using the TPS signalling information.

When this register is written, these bits store the next Viterbi Code Rate for the Low-Priority stream value that the system uses. The values are:

LP_CODE_RATE[2:0]			Definition
0	0	0	1/2 Code Rate
0	0	1	2/3 Code Rate
0	1	0	3/4 Code Rate
0	1	1	5/6 Code Rate
1	0	0	7/8 Code Rate
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

The initial condition for the LP_CODE_RATE is 0b000 (1/2).

HP_CODE_RATE

Viterbi High-Priority Code Rate **R/W [2:0]**

When this register is read, these bits provide the last value received by the channel, using the TPS signalling information.

When this register is written, these bits store the next Viterbi Code Rate for the High-Priority stream value that the system uses. The values are:

HP_CODE_RATE[2:0]	Definition
000	1/2 Code Rate
001	2/3 Code Rate
010	3/4 Code Rate
011	5/6 Code Rate
100	7/8 Code Rate
101	Reserved
110	Reserved
111	Reserved

The initial condition for these bits is 0b001 (2/3).

4.3.3 Address Line 0x04

	7	6 5	4 2	1 0
0x04	RES	FRAME_NB	HIERARCHY	QAMTYPE

RES **Reserved** **7**
This bit is reserved.

FRAME_NB **COFDM Frame Number** **R [6:5]**
When this register is read, these bits provide the last value received by the channel, using the TPS signalling information. The values are:

FRAME_NB[1:0]		Definition
0	0	Frame 0
0	1	Frame 1
1	0	Frame 2
1	1	Frame 3

The initial condition for the FRAME_NB is 0b00 (Frame 0).

Internally, there are three TPS registers:

- The first (0x02, the active TPS register) contains the current mode of the DTTV demodulator.
- The second (the next TPS register, 0x03) is written by writing to the TPS register in the register map. When the “change mode” command is issued, the next TPS register is copied into the active TPS register, and this becomes the current mode of the demodulator.
- The third register (the received TPS register, 0x04) contains a copy of the last valid TPS that was received in the input signal. This register can be read by reading from the TPS register in the register map.

If the AUTO_MODE_ENABLE bit is set, then every time a valid TPS is received and a super-frame boundary is detected, the demodulator copies the contents of the received TPS register into the active TPS register (and changes the current mode of the DTTV receiver if the received TPS changes).

If the received TPS (stored in the received TPS register) and the current mode of the DTTV demodulator (held in

the active TPS register) differ, the TPS_INFO_CHANGE bit is set to 1 for one CLK18 clock cycle. When the TPS_INFO_CHANGE interrupt is enabled and this event occurs, the DTTV demodulator generates an interrupt to the external microcontroller. The rule for the TPS_INFO_CHANGE applies to all TPS data bits except for the frame number.

HIERARCHY **COFDM Nonuniform Constellation Ratio** **R/W [4:2]**

When this register is read, these bits provide the last value received by the channel, using the TPS signalling information.

When this register is written, these bits store the next Constellation expansion ratio that the system uses. The values are:

HIERARCHY[2:0]	Definition
000	Nonhierarchical
001	$\alpha = 1$
010	$\alpha = 2$
011	$\alpha = 4$
100	Reserved
101	Reserved
110	Reserved
111	Reserved

The initial condition for the HIERARCHY is 0b000 (Nonhierarchical).

QAMTYPE **Constellation Type** **R/W [1:0]**

When this register is read, these bits provide the last value received by the channel, using the TPS signalling information.

When this register is written to, these bits store the next Constellation Type value that the system uses. The values are:

QAMTYPE[1:0]	Definition
00	QPSK
01	16 QAM
10	64 QAM
11	reserved

The initial condition for the QAMTYPE is 0b10 (64 QAM).

4.4 Parameter Registers

The Parameter registers contain configuration information. If the registers are read, they indicate the current parameter value. These Parameter registers are only configurable through the microprocessor.

4.4.1 Address Line 0x05

	7	6	5	4	3	2	0
0x05	AFC_ CLIPPING	AFC_MODE	AFC_FINE _MODE	AFC_STALL	AFC_POL	AFC_SENSITIVITY	

AFC_CLIPPING

AFC Loop Bandwidth Limiter **R/W 7**

This bit selects the combination method between the Fine Algorithm part and the Coarse Algorithm part.

When using Method I (AFC_CLIPPING = 0), the combination is done by adding the two values. When the Coarse part is an integer number of carrier spacing, and the Fine part is a fraction of the carrier spacing, the result is the exact frequency offset.

When using Method II (AFC_CLIPPING = 1), the Fine part is only considered when the AFC Coarse value is 0.

If not, the value applied to the Tuner Oscillator (via the Sigma-Delta) is either +1 or –1. This limits the bandwidth of the system.

The initial condition for the AFC_CLIPPING bit is 1, which is Method II.

AFC_MODE **AFC Muxin Mode** **R/W 6**

When the MUXIN bus is connected to the AFC, this bit determines if the Symbol Number is coming from the OBC (Partial MUXIN Mode), as in Normal functional mode, or coming from the MUXIN bus itself (Full MUXIN Mode). If this bit is 0, the Symbol Number is coming from the Full MUXIN Mode; if this bit is 1, the Symbol Number is coming from the Partial MUXIN Mode.

The initial condition for the AFC_MODE is 0, the Full MUXIN mode. However, this has no effect if the default mode of AFC_MUXIN is 0 (which means that the AFC is taking its Symbol Number from the OBC no matter what the value of AFC_MODE is). See the definition of the MUXIN register for more information.

AFC_FINE_MODE

AFC Fine Algorithm Mode **R/W 5**

This bit determines if the AFC Fine Algorithm performs a weighted mean.

If the Weighted mean mode is chosen (this bit is 0), the AFC algorithm performs a weighted mean on the signal measurements to perform its Fine AFC calculation.

If the Unweighted mean mode is chosen (this bit is 1), the AFC algorithm does not perform a weighted mean on the signal measurements to perform its Fine AFC calculation.

The initial condition for this bit is 0, the Weighted Mean mode.

AFC_STALL **AFC Loop Updating Freeze** **R/W 4**

This bit determines if the AFC Loop is working or frozen.

If the Loop is working (0), the integrator inside the L64780 updates its value from time to time.

If the Loop is stalled (1), the integrator inside the L64780 keeps its internal value constant, enabling you to set the Frequency Offset by means of software (using AFC_INIT_FREQ).

The initial condition for the AFC_STALL is 0, the normal working mode.

AFC_POL **AFC VCO Polarity** **R/W 3**

These bits determine the polarity of the external VCO.

If the polarity is positive (this bit is 0), the output frequency of the external down-converter must increase with increasing voltage from the AFCOUT pin.

If the polarity is negative (this bit is 1), the output frequency of the external down-converter must decrease with increasing voltage from the AFCOUT pin.

The initial condition for the AFC_POL is 0 (positive).

AFC_SENSITIVITY

AFC Loop Gain **R/W [2:0]**

These bits adjust the AFC Gain of the Loop Filter. The value is set according to the sensitivity of the AFC input of the external down-converter. The values in digital AFC loop mode are:

AFC_SENSITIVITY[2:0]			Definition
0	0	0	$K_{SENS} \approx 1.52\times10^{-5}$
0	0	1	$K_{SENS} \approx 3\times10^{-5}$
0	1	0	$K_{SENS} \approx 6\times10^{-5}$
0	1	1	$K_{SENS} \approx 1.22\times10^{-4}$
1	0	0	$K_{SENS} \approx 2.44\times10^{-4}$
1	0	1	$K_{SENS} \approx 4.88\times10^{-4}$
1	1	0	$K_{SENS} \approx 9.8\times10^{-4}$
1	1	1	$K_{SENS} \approx 1.95\times10^{-3}$

The initial condition for these bits is 0b110, or $K_{SENS} \approx 9.8\times10^{-4}$.

The values in Analog AFC loop mode are:

AFC_SENSITIVITY[2:0]			Definition
0	0	0	$K_{SENS} \approx 2.44 \times 10^{-4}$
0	0	1	$K_{SENS} \approx 4.88 \times 10^{-4}$
0	1	0	$K_{SENS} \approx 9.8 \times 10^{-4}$
0	1	1	$K_{SENS} \approx 1.95 \times 10^{-3}$
1	0	0	$K_{SENS} \approx 3.9 \times 10^{-3}$
1	0	1	$K_{SENS} \approx 7.8 \times 10^{-3}$
1	1	0	$K_{SENS} \approx 1.56 \times 10^{-2}$
1	1	1	$K_{SENS} \approx 3.1 \times 10^{-2}$

The initial condition for these bits is 0b110, or $K_{SENS} \approx 1.56 \times 10^{-2}$.

4.4.2 Address Lines 0x06, 0x07, 0x08

	7 ... 0
0x06	AFC_INIT_FRQ_LSB
0x07	AFC_INIT_FRQ_CSB
0x08	AFC_INIT_FRQ_MSB

AFC_INIT_FRQ

AFC Initial Frequency Offset **R/W [7:0]**

These three 8-bit registers select the Initial Frequency Offset that is directed towards the Tuner or the DDFS block.

- When these registers are read, the resultant value represents the actual Frequency Offset (for example, the content of the integrator) recovered by the system.
- When this register is written, the resultant value reinitializes the Integrator value.
- Three OBC accesses are necessary to update these registers; thus, you should first stall the Integrator by setting AFC_STALL to 1, then update the values. You can reactivate the integrator by resetting AFC_STALL to 0.

The initial condition for these registers is 0.

4.4.3 Address Line 0x09

	7	6	5	4 3	2	1	0
0x09	SOFTBIT	BDI_ DISABLE	SDI_ DISABLE	DOF_OUTPUT_ FORMAT	DDFS_ DISABLE	DDFS_ MODE	ADCON

SOFTBIT **Soft Decision Number of Bits** **R/W 7**

This bit determines if a 3-bit (0) or a 4-bit (1) soft decision is used. The initial condition for this bit is 1.

BDI_DISABLE

BDI Disable **R/W 6**

If this bit is 1, the Bit Deinterleaver is disabled; if this bit is 1, the Bit Deinterleaver is enabled. The initial condition for this bit is 0, the Normal Operational Mode.

SDI_DISABLE

SDI Disable **R/W 5**

If this bit is 1, the Symbol Deinterleaver is disabled; if this bit is 0, the Symbol Deinterleaver is enabled. The initial condition for this bit is 0, the Normal Operational Mode.

DOF_OUTPUT_FORMAT

Chip Output Format **R/W [4:3]**

These bits select the output format of the L64780 towards the FEC decoder chip. The different formats are described in Section 3.4, “Microprocessor Interface.” There are three modes:

- When in Nonhierarchical mode, two submodes are provided: Serial and Parallel. In Serial Mode, data is presented only on SD0. In Parallel Mode, data is presented on SD0 and SD1.
- When in Hierarchical mode with only one FEC chip, either the HP stream or the LP Stream is presented.

- When in Hierarchical mode with two FEC chips, HP and LP streams are presented on SD0 and SD1, respectively.

Hierarchical	DOF_OUTPUT_FORMAT[1:0]		Definition
NO	X	0	Serial Mode
NO	X	1	Parallel Mode
YES	0	0	HP stream over SD0, 1 FEC Mode
YES	1	0	LP stream over SD0, 1 FEC Mode
YES	X	1	HP over SD0, LP over SD1, Two FEC Mode

The initial condition for these bits is 0b00.

DDFS_DISABLE

DDFS Disable **R/W 2**

This bit determines if the DDFS performs the Baseband correction (0) or not (1). The initial condition for the DDFS_DISABLE is the Normal Operational Mode (0).

DDFS_MODE

DDFS Start Pulse Selector **R/W 1**

If this bit is 0, the DDFS block gets its START Pulse (pulse delimiting every COFDM symbol) from the Timing Recovery Unit Block; if this bit is 1, the DDFS block gets its START Pulse from the MUXIN Block.

The initial condition value for the DDFS_MODE bit is 0.

The DDFS block can operate in four modes, as listed in Table 4.2.

Table 4.2 DDFS Block Modes

DDFS Mode	DDFS Muxin	DDFS Disable	Functional Mode
X	0	0	Normal
0	1	0	Test
1	1	0	Down-Converter Off-Chip
X	X	1	Disable Mode

When in Normal mode, the L64780 receives a real signal in the intermediate frequency (about 4.5 MHz), and the R2C block performs the baseband conversion. In this mode, the DDFS block receives a complex baseband signal directly from the R2C block and takes the DDFS_XIN, DDFS_YIN, and DDFS_DVIN signals and the symbol synchronization DDFS_STARTIN signal from the Timing synchronization (TIM) block.

In Down-Converter Off-Chip mode, the baseband conversion is done by the tuner, but the COFDM symbol synchronization signal is still provided by the TIM block. In this mode, the DDFS block takes the DDFS_XOFF, DDFS_YOFF, and DDFS_DVOFF signals from the off-chip interface, whereas the symbol synchronization DDFS_STARTIN signal comes from the TIM block (see Section 3.2.1, “Access to Timing and DDFS Blocks,” page 3-10, for the DDFS_XOFF, DDFS_YOFF, and DDFS_DVOFF signals mapping into the MUXIN bus).

When in Test mode, the DDFS block receives the baseband complex data and the symbol synchronization from the off-chip interface. In this mode, the DDFS_XOFF, DDFS_YOFF, DDFS_DVOFF, and DDFS_STARTOFF signals come from the off-chip interface. (See Section 3.2.1, “Access to Timing and DDFS Blocks,” page 3-10, for the DDFS_XOFF, DDFS_YOFF, and DDFS_DVOFF and DDFS_STARTOFF signals mapping into the MUXIN bus.)

In Disable mode, only the DDFS_XIN, DDFS_YIN, DDFS_DVIN, and DDFS_STARTIN signals are used; no frequency shift is applied to the incoming complex data, but the data processing time latency must be preserved.

ADCON **ADC Selector** **R/W 0**

This bit determines if the L64780 uses the 8-bit on-chip (1), or the external 10-bit (0) ADC. The initial condition for the ADCON is 0, the external 10-bit ADC.

4.4.4 Address Line 0x0A

	7 5	4	3	2 0
0x0A	AGC_TARGET_LSB	AGC_DISABLE	AGC_POL	AGC_GAIN

AGC_TARGET_LSB

AGC Target RMS Value (LSB) **R/W [7:5]**

These bits select the LSBs of the Target RMS value of the AGC Loop (see Section 2.3.1, “AGC Target RMS Value”). The initial condition for these bits is 0b100.

AGC_DISABLE

AGC Disable **R/W 4**

This bit determines if the AGC is disabled (1) or not (0). The initial condition for the AGC_DISABLE bit is 0, Normal Operational Mode.

AGC_POL **AGC Loop Polarity** **R/W 3**

This bit selects the polarity of the external AGC Loop.

If the polarity is positive (this bit is 0), the gain of the external down-converter must increase with increasing voltage from the AGCOUT pin.

If the polarity is negative (this bit is 1), the gain of the external down-converter must decrease with increasing voltage from the AGCOUT pin.

The initial condition for the AGC_POL is 1, negative.

AGC_GAIN **AGC Loop Gain** **R/W [2:0]**

These bits adjust the AGC Gain of the Loop Filter. The value is set according to the sensitivity of the AGC loop. The values are:

AGC_GAIN[2:0]			Definition
0	0	0	$K_S \approx 3.9\times10^{-3}$
0	0	1	$K_S \approx 9.8\times10^{-4}$
0	1	0	$K_S \approx 2.4\times10^{-4}$
0	1	1	$K_S \approx 6.1\times10^{-5}$
1	0	0	$K_S \approx 1.5\times10^{-5}$
1	0	1	$K_S \approx 3.8\times10^{-6}$
1	1	0	$K_S \approx 9.5\times10^{-7}$
1	1	1	$K_S \approx 2.4\times10^{-7}$

The initial condition for these bits is 0b011, $K_S \approx 6.1\times10^{-5}$.

4.4.5 Address Line 0x0B

	7	6	5 … 0
0x0B	ADC_FORMAT	R2C_SI	AGC_TARGET_MSB

ADC_FORMAT

Format of ADC Output **R/W 7**

This bit determines if the ADC outputs its values in two's complement (1) or in binary offset format (0). The initial condition for the ADC_FORMAT bit is 0, binary offset.

R2C_SI **COFDM Spectrum Inversion** **R/W 6**

During the up-conversion and the following down-conversion, the COFDM spectrum can be inverted, depending on the equipment used. This bit determines if the COFDM signal should be spectrally inverted (1) or not (0).

The initial condition for the R2C_SI bit is 0, normal operation.

This spectrum inversion changes the sign of the sine function (negative for 0, positive for 1).

AGC_TARGET_MSB

AGC Target RMS Value (MSB) **R/W [5:0]**

These bits select the MSBs of the Target RMS value of the AGC Loop (see Section 2.3.1, “AGC Target RMS Value”).

The initial condition for these bits is 0x0E.

4.4.6 Address Line 0x0C

	7 5	4 2	1 0
0x0C	TIM_LOOP_I	TIM_LOOP_P	TIM_IIRGAIN

TIM_LOOP_I **Timing Gain Loop 2** **R/W [7:5]**

These bits adjust the Timing Gain of the Loop Filter. The value is set according to the sensitivity of the VXCO loop.

TIM_LOOP_I[2:0]			Definition
0	0	0	$K_I \approx 0.125$
0	0	1	$K_I \approx 3.125\times10^{-2}$
0	1	0	$K_I \approx 7.8\times10^{-3}$
0	1	1	$K_I \approx 1.95\times10^{-3}$
1	0	0	$K_I \approx 4.8\times10^{-4}$
1	0	1	$K_I \approx 1.22\times10^{-4}$
1	1	0	$K_I \approx 3\times10^{-5}$
1	1	1	$K_I \approx 7.63\times10^{-6}$

The initial condition for the TIM_LOOP_I is ob011 (Gain 3) $K_I \approx 1.95\times10^{-3}$.

TIM_LOOP_P

Timing Gain Loop 1 **R/W [4:2]**

These bits adjust the Timing Gain of the Loop Filter. The value is set according to the sensitivity of the VXCO loop.

TIM_LOOP_P[2:0]			Definition
0	0	0	$K_P \approx 8.0$
0	0	1	$K_P \approx 4.0$
0	1	0	$K_P \approx 2.0$
0	1	1	$K_P \approx 1.0$
1	0	0	$K_P \approx 0.5$
1	0	1	$K_P \approx 0.25$
1	1	0	$K_P \approx 0.125$
1	1	1	$K_P \approx 6.25 \times 10^{-2}$

The initial condition for the TIM_LOOP_P is 0b011 (Gain 3) $K_P \approx 1.0$.

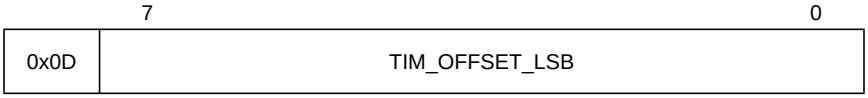
TIM_IIRGAIN **Timing IIR Filter Time Constant** **R/W [1:0]**

These bits govern the amount of IIR Filtering done in the Timing Loop Filter.

TIM_IIRGAIN[1:0]		Definition
0	0	$\alpha \approx 6.25 \times 10^{-2}$
0	1	$\alpha \approx 3.125 \times 10^{-2}$
1	0	$\alpha \approx 1.56 \times 10^{-2}$
1	1	$\alpha \approx 7.8 \times 10^{-3}$

The initial condition for the TIM_IIRGAIN is 0b01 (Gain 1) $\alpha \approx 3.125 \times 10^{-2}$.

4.4.7 Address Line 0x0D

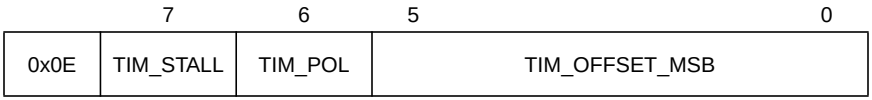


TIM_OFFSET_LSB

Start Pulse Phase Offset (LSB) **R/W [7:0]**

The start pulse is a signal with a periodicity of every FFT-MODE+GUARD 9 MHz cycles (in steady state). The TIM_OFFSET bits adjust the phase of this signal in the periodic window. The initial condition for the TIM_OFFSET_LSB bits is 0x00.

4.4.8 Address Line 0x0E



TIM_STALL **TIM Loop Updating Freeze** **R/W 7**

This bit determines if the Loop is working (this bit is 0) or stalled (this bit is 1).

If the Loop is working, the integrator inside the L64780 updates its value.

If the Loop is stalled, the integrator inside the L64780 keeps its internal value constant, letting you set the VCXO Frequency Offset by means of the TIM_CLK_INIT bits.

The initial condition for the TIM_STALL bit is 0, normal working mode.

TIM_POL **TIM VCXO Polarity** **R/W 6**

This bit determines the polarity of the external VCXO:

- If the polarity is positive (this bit is 0), the output frequency of the external VCXO increases with increasing voltage from VCXOUT.
- If the polarity is negative (this bit is 1), the output frequency of the external VCXO decreases with increasing voltage from VCXOUT.

The initial condition for the TIM_POL is 1, negative polarity.

TIM_OFFSET_MSB

Start Pulse Phase Offset (MSB) **R/W [5:0]**

The start pulse is a signal with a periodicity of every FFT-MODE + GUARD 9 MHz cycles (in steady state). The TIM_OFFSET bits adjust the phase of this signal in the periodic window. The initial condition for these bits is 0x00.

4.4.9 Address Lines 0x0F, 0x10

	7	0
0x0F	TIM_CLK_INIT_LSB	
0x10	TIM_CLK_INIT_MSB	

TIM_CLK_INIT

Timing Initial VCXO Offset **R/W [7:0]**

These two registers, TIM_CLK_INIT_LSB and TIM_CLK_INIT_MSB, select the initial VCXO frequency offset that is directed to the external VCXO.

When this register is read, its value represents the actual VCXO offset (for example, the content of the integrator) recovered by the system.

When this register is written, this value reinitializes the Integrator value.

Two OBC accesses are required to update these registers; thus, you should first stall the Integrator by setting TIM_STALL to 1, then update the values. The process can be unfrozen by clearing TIM_STALL back to 0.

The initial condition for these bits is 0x00 (both registers set to 0x00).

4.4.10 Address Line 0x11

	7	6	5	4	3	2	1 0
0x11	CPE_ DISABLE	CE_ DISABLE	CE_ DISABLE_ ETS	CE_TEMPO- TYPE	CE_SEL ECT	FFT_DIR	FFT_GAIN

CPE_DISABLE

Common Phase Error Disable **R/W 7**

This bit determines if the CPE is disabled (1) or not (0). The initial condition for this bit is 0, normal operation.

CE_DISABLE **CE Disable** **R/W 6**

This bit determines if the CE is disabled (1) or not (0). The initial condition for this bit is 0, normal operation.

CE_DISABLE_ETS

CE Timing Shift Disable **R/W 5**

The Channel Equalizer emulates a negative echo to ease implementation. If this bit has a value of 1, the negative echo generation is disabled. If this bit is set to 0, the negative echo generation is enabled. The initial condition for this bit is 0, Working Mode.

CE_TEMPOTYPE

CE Timing Interpolation Type **R/W 4**

This bit selects the mode of operation of the Channel Equalizer Timing Interpolation. If this bit is 0, the mode is Zero Order Hold; if this bit is 1, the mode is Linear. The initial condition for this bit is 1, Linear.

CE_SELECT **CE MUXOUT Selector** **R/W 3**

When MUXOUT is selected to output the Channel Equalizer value, either the Channel Response (1) or the Equalized Data (0) can be output. Note that both cases do not affect receiver functionality. The initial condition for this bit is 0, Equalized Data.

FFT_DIR **FFT Direction** **R/W 2**

This bit determines if the FFT is in Forward mode (Timing to Frequency Domain, 0) or Backward mode (Frequency to Timing Domain, 1). For L64780 normal operational mode, the FFT direction is Forward. The initial condition for the FFT_DIR is 0, Forward.

FFT_GAIN **FFT Clipping and Rounding** **R/W [1:0]**

This register selects how the FFT clips and rounds in case of overflow. The values are:

FFT_GAIN[1:0]		Definition
0	0	Gain 0
0	1	Gain 1
1	0	Gain 2
1	1	Gain 3

The initial condition for these bits is 0b10, Gain 2.

4.4.11 Address Line 0x12

	7	3	2	1	0
0x12	RES		CSI_OUT_ FORMAT	CSI_IIRATE	

RES **Reserved** **[7:3]**

These bits are reserved.

CSI_OUT_FORMAT

CSI Softbits Format **R/W 2**

This bit allows the generation of softbit values either in two's complement (1) or in binary offset (0). The initial condition for this bit is 0, binary offset.

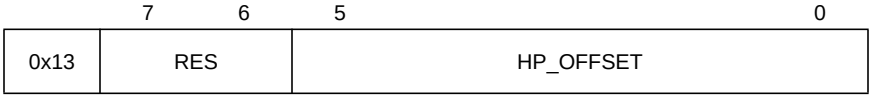
CSI_IIRATE **CSI IIR Filter Gain** **R/W [1:0]**

These bits set the IIR Gain of the Channel State Information Unit. The values are:

CSI_IIRATE[1:0]		Definition
0	0	Gain 0
0	1	Gain 1
1	0	Gain 2
1	1	Gain 3

The initial condition for the CSI_IIRATE is 0b01, Gain 1.

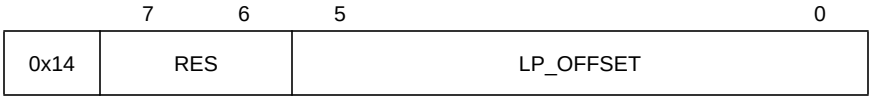
4.4.12 Address Line 0x13



RES **Reserved** **[7:6]**
These bits are reserved.

HP_OFFSET **CSI HP Stream Quantizer Gains** **R/W [5:0]**
These bits set the Quantizer Gain of the Channel State Information Unit for the High-Priority stream. The initial value for the HP_OFFSET bits is 0x36.

4.4.13 Address Line 0x14



RES **Reserved** **[7:6]**
These bits are reserved.

LP_OFFSET **CSI LP Stream Quantizer Gains** **R/W [5:0]**
These bits set the Quantizer Gain of the Channel State Information Unit for the Low-Priority stream. The initial value for the LP_OFFSET is 0x36.

4.5 Mux Register Address Line 0x15

This register brings data to and from specific blocks. The MUXIN register is directly output from the OBC and goes to the Clock generator block.

	7	6	5	3	2	0
0x15	RES		MUXIN		MUXOUT	

RES **Reserved** **[7:6]**
These bits are reserved.

MUXIN **MUXIN Selector** **R/W [5:3]**
These bits select the point in the system to be driven through the MUXIN input pins and the CLKMUXIN clock to sample the data coming into the L64780. There are six possibilities:

MUXIN	Definition	Muxin Clock
000	Normal Mode	Set LOW
001	MUXIN inputs to Timing and DDFS Block	18 MHz
010	MUXIN inputs to AFC Block	36 MHz
011	MUXIN inputs to FFT Block	36 MHz
100	MUXIN inputs to CSI Block	18 MHz
101	MUXIN inputs to SDI Block	18 MHz
110	unused	Set LOW
111	unused	Set LOW

The initial value for MUXIN is 0b000 (no MUXIN).

Table 4.3 defines how to set the different MUXIN signals and the Muxin clock.

Table 4.3 MUXIN Signal Settings and MUXIN Clock

MUXIN	TIM Muxin	DDFS Muxin	AFC Muxin	FFT Muxin	CSI Muxin	SDI Muxin	Muxin Clock
000	0	0	0	0	0	0	Set LOW
001	1	1	0	0	0	0	CLK18
010	0	0	1	0	0	0	CLK36
011	0	0	0	1	0	0	CLK36
100	0	0	0	0	1	0	CLK18
101	0	0	0	0	0	1	CLK18
110	0	0	0	0	0	0	Set LOW
111	0	0	0	0	0	0	Set LOW

MUXOUT **MUXOUT Selector** **R/W [2:0]**

These bits select the point in the system to be monitored through the output block. There are six possibilities:

MUXOUT[2:0]			Definition
0	0	0	DDFS Output Presented
0	0	1	FFT Output Presented
0	1	0	AFC Output Presented
0	1	1	CE Output Presented
1	0	0	CSI Output Presented
1	0	1	AFC Output Presented
1	1	0	unused
1	1	1	unused

The initial value for these bits is 0b011, CE Output.

4.6 Performance Monitoring Registers Address Line 0x16

These registers contain the aggregate statistical and monitoring information available to the OBC block.

	7	6	5	4	3	2	1	0
0x16	RES		FRAME_ SYNC_ OK	TPS_ SYNC_ OK	AFC_ SYNC_ OK	TIM_CLK_ SYNC_OK	TIM_ START_ SYNC_OK	SYNC_OK

RES **Reserved** **[7:6]**
These bits are reserved.

FRAME_SYNC_OK
COFDM Frame Synchronization **R/W 5**
If the frame synchronization in the DTTV demodulator is correct, this bit is 1 (ODFM frame is locked). If this bit is 0, the COFDM frame is unlocked. The initial condition for this bit is 1, locked.

TPS_SYNC_OK
TPS Synchronization **R/W 4**
If the BCH code in the TPS indicates that the TPS is valid, this bit is 1 (TPS is locked). If this bit is 0, TPS is unlocked. The initial condition for this bit is 1, locked.

AFC_SYNC_OK
AFC Synchronization **R/W 3**
If the frequency synchronization in the DTTV demodulator is correct, this bit is 1 (AFC locked); otherwise, it is 0 (unlocked). The initial condition for this bit is 1, locked.

TIM_CLK_SYNC_OK
Timing Synchronization **R/W 2**
If the sampling frequency synchronization in the DTTV demodulator is correct, this bit is 1 (VCXO is locked); otherwise, it is unlocked. The initial condition for this bit is 1, locked.

TIM_START_SYNC_OK

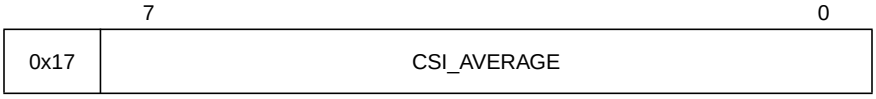
Start Pulse Synchronization **R/W 1**

If the start FFT window synchronization (start pulse is locked) in the DTTV demodulator is correct, this location is 1; otherwise, the start pulse is unlocked. The initial condition for this bit is 1, locked.

SYNC_OK **Overall Chip Synchronization** **R/W 0**

If all aspects of the DTTV demodulator are synchronized, this bit is 1. If this bit is 0, at least one unit is not locked. The initial condition for this bit is 1, locked.

4.6.1 Address Line 0x17

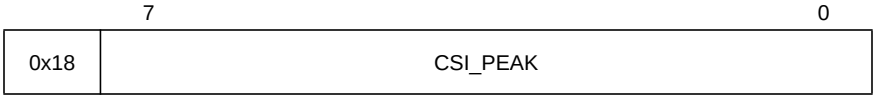


CSI_AVERAGE

CSI Reliability Average **R [7:0]**

This register indicates the overall reliability of the carriers by making an average (integer number) of the reliability of each carrier.

4.6.2 Address Line 0x18



CSI_PEAK **CSI Reliability Peak** **R [7:0]**

This register gives the integer number of carriers when the value of the filtered Channel State Information exceeds a given threshold. If more than 255 carriers exceed this value, then 255 is returned.

4.7 Mode Register Address Line 0x19

This register influences how the DTTV demodulator operates.

	7	6	5	4	3	2	1	0
0x19	RES	ODRAIN_CTRL	WIRES3_CTRL	SD_CTRL	MUX_CTRL	SOFT_RESET	AUTO_MODE_ENABLE	CHANGE_MODE

RES **Reserved** **7**

This bit is reserved.

ODRAIN_CTRL

Output Drain Controller **R/W 6**

This bit allows the 3-Wire Bus pins to be set in Open Drain Mode. When this bit is 1, the 3-wire output bus is working in open drain (1 => Z, 0 => 0). When this bit is 0, the bus is in normal mode. The initial condition for this bit is 1, Output Drain Mode.

The WIRES3_CTRL and ODRAIN_CTRL bits generate the OBC_WIRE3_CTRL[2:0] 3-state control signals, as specified in the following table.

OBC_WIRE3_OUT	ODRAIN_CTRL	WIRE3_CTRL	OUT
0	0	0	0
0	1	0	0
0	0	1	Z
0	1	1	Z
1	0	0	1
1	1	0	Z
1	0	1	Z
1	1	1	Z

WIRES3_CTRL

3-Wire Bus 3-State Controller **R/W 5**

When this bit is 1, the 3-Wires Bus pins are 3-stated. When this bit is 0, the bus pins are in normal mode. The initial condition for this bit is 0, normal mode.

SD_CTRL **Normal Output 3-State Controller** **R/W 4**

When this bit is 1, all Normal pins are 3-stated. The initial condition for this bit is 0, normal mode.

MUX_CTRL **MUXOUT 3-State Controller** **R/W 3**

When this bit is 1, all MUXOUT pins are 3-stated. The initial condition for this bit is 0, normal mode.

SOFT_RESET **Chip Soft Reset** **R/W 2**

Setting this bit enables a hard reset of the L64780 logic (except the OBC registers, which keep their values). This allows a proper reset of the chip in any default configuration (memories are also reset to 0). Note that the Soft Reset must be asserted from the external microcontroller; it is not a pulse. When this bit is 1, soft reset is enabled. When this bit is 0, no soft reset is possible.

AUTO_MODE_ENABLE

TPS Auto Updating **R/W 1**

This bit determines if the TPS updating is controlled by the external microcontroller, or if the Active registers are automatically updated each time new value TPS arrive from the Broadcaster.

If this bit is 1, the current mode (as defined by the TPS register) of the demodulator is updated whenever a valid TPS is received.

If this bit is 0, manual configuration of the TPS register is required.

The initial condition for this bit is 0, Manual Update.

CHANGE_MODE

TPS Updating Register **W 0**

When a new mode of operation has been written into the TPS register, writing the value 1 into this location causes the demodulator to change mode. See Section 4.3, “TPS Registers,” page 4-11 for more information.

4.8 3-Wires Register Address Line 0x1A

The 3-wires register emulates the 3-Wires Bus protocol and controls the tuner. It can also be used to emulate a software I^2C interface towards the tuner.

	7 6	5 3	2 0
0x1A	RES	WIRES3_IN	WIRES3_OUT

RES **Reserved** **[7:6]**
These bits are reserved.

WIRES3_IN **3-Wires Input** **R/W [5:3]**
These bits collect the information coming from the 3-Wires off-chip inputs. The initial condition for WIRES3_IN is 0x0.

WIRES3_OUT **3-Wires Output** **R/W [2:0]**
These bits are directly presented off-chip to the control Tuner. The initial condition for WIRES3_OUT is 0x0.

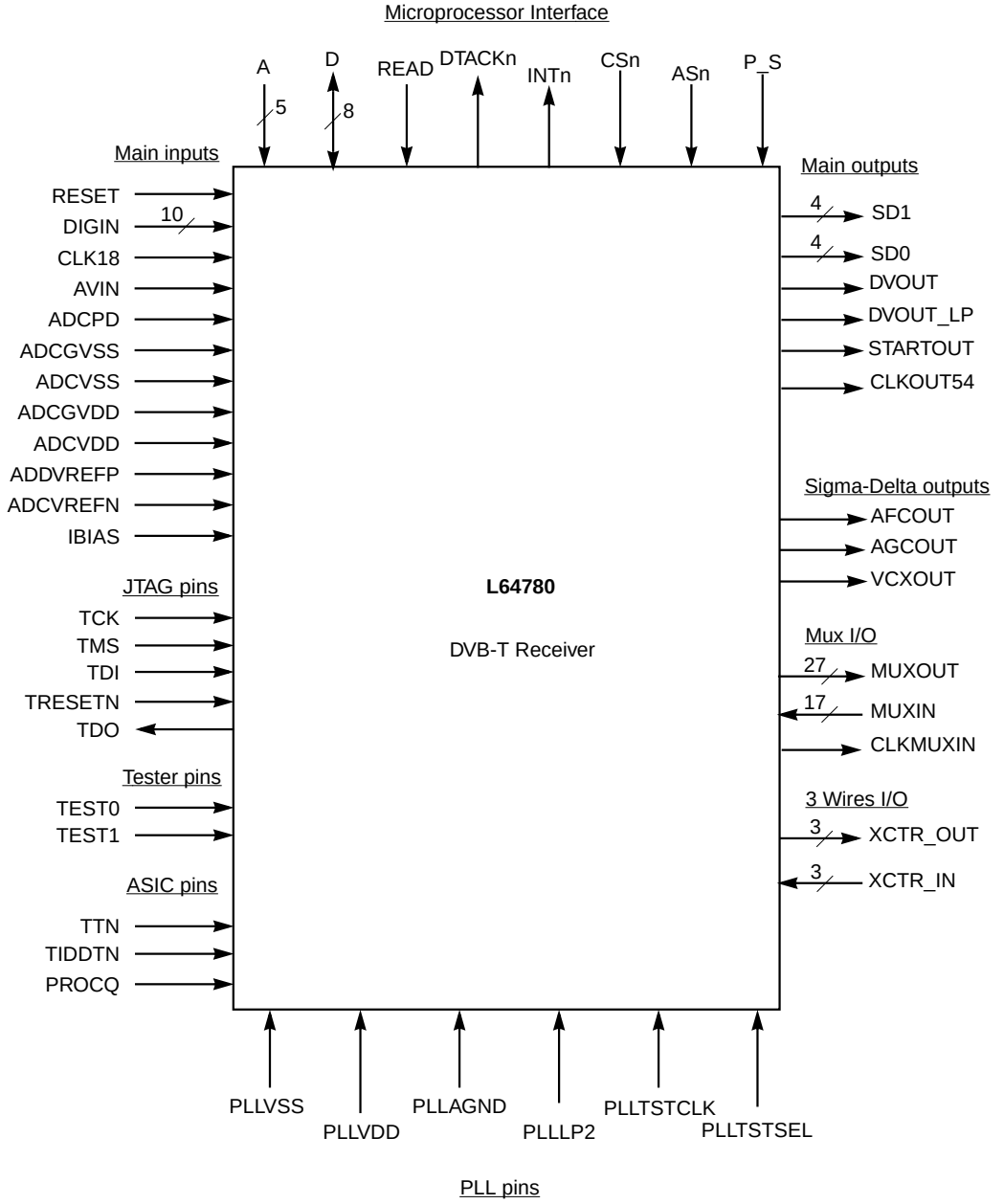
Chapter 5
Signal Descriptions

This chapter describes the L64780 signals. These signals are grouped by function. Within each group, the signals are described in alphabetical order. This chapter consists of the following sections:

5.1 Overview

Figure 5.1 provides the logic symbol for the L64780.

Figure 5.1 L64780 Logic Symbol



5.2 Microprocessor Interface

This section lists and describes the microprocessor interface signals.

Note that the parallel interface mode is used for LSI Logic internal testing and is not intended for use in customer production receivers. The serial mode interface is used for production systems.

A[4:0] **Address Bus** **I**
The DTTV receiver has a five-bit address bus, A[4:0], that is used with an eight-bit data bus, D[7:0], a read/write strobe, Read, an address strobe, ASn, and a chip select strobe, CSn, to read and write internal registers. The address lines select internal registers. In Serial Mode, A0 is used as the serial clock, and A[4:1] must be connected to ground.

ASn **Address Strobe** **I**
Active LOW address strobe input. Latches the address on the A[4:0] bus on the falling edge. In Serial interface mode, ASn must be connected to VDD.

CSn **Chip Select** **I**
Active LOW chip select strobe input. During a read cycle, CSn must be LOW to access the on-chip data registers. During a read access, the external controller can latch the data from the DTTV receiver with the rising edge of CSn. During a write access, CSn must go LOW prior to data being valid from the external controller to the DTTV receiver. In Serial Interface mode, CSn must be connected to VDD.

D[7:0] **Microprocessor Data Bus** **I/O**
This bidirectional bus is used as an input when data is written to the chip, and as an output when the chip is read. When the L64780 is not being read or written to, the data lines are 3-stated. In Serial Interface Mode, D0 is used as the serial data, and D[7:1] are used for the programmable Serial Bus interface.

DTACKn **Data Transaction Acknowledge** **O**
Active LOW output indicating that the transaction has been completed. When not driven, the line is open-drain 3-stated.

INTn **Interrupt** **O**
The DTTV receiver asserts INTn when an internal, unmasked interrupt flag is set. INTn remains asserted as long as the interrupt condition persists and the interrupt flag is not masked. When not driven, the line is open-drain 3-stated.

P_S **Microprocessor Operation Mode** **I**
When this signal is LOW, operation is Parallel Mode; when HIGH, operation is Serial Mode.

READ **Read Strobe** **I**
When HIGH, a read operation is selected; when LOW, a write operation is selected. In Serial interface mode, READ must be connected to VDD.

5.3 Main Signals

This section lists and describes the main signals input to the L64780 or output to the L64705/L64724.

ADCGVDD **Guard VDD for Internal ADC** **I**
Must be connected to VDD.

ADCGVSS **Internal ADC Guard VSS** **I**
Must be connected to ground.

ADCPD **Power-Down Mode for Internal ADC** **I**
This pin is active HIGH and in normal mode must be connected to ground.

ADCVDD **Analog VDD for Internal ADC** **I**
Must be connected to VDD.

ADCVREFN **Internal ADC Negative Reference Voltage** **I**
When not used, this pin must be connected to ground.

ADCVREFP **Internal ADC Positive Reference Voltage** **I**
When not used, this pin must be connected to ground.

ADCVSS **Analog VSS for Internal ADC** **I**
Must be connected to ground.

AVIN **Analog Input for Internal ADC** **I**
For an external ADC, this pin must be connected to ground.

CLK18 **18 MHz Clock** **I**
This is the 18 MHz input clock coming from the external VCXO.

CLKOUT54 **54 MHz Clock** **O**
This is the 54 MHz clock output and is used to clock the L64705 or the L64724.

DIGIN[9:0] **Digital Inputs** **I**
Digital inputs in normal mode when a 10-bit off-chip ADC is used. DIGIN0 represents the LSB, while DIGIN9 represents the MSB. This bus is latched with the CLK18 clock. In MUXIN mode, DIGIN[9:0] represents the 10 LSBs of the 27 MUXIN bits, with DIGIN[0] mapped to MUXIN0, and DIGIN9 to MUXIN9. For an on-chip ADC, this bus must be connected to ground.

DVOUT **SD0 Data Valid Out** **O 3-State**
When asserted HIGH, this signal validates the SD0[3:0] bus.

DVOUT_LP **SD1 Data Valid Out** **O 3-State**
When asserted HIGH, this signal validates the SD1[3:0] bus.

IBIAS **Input Bias Current for Internal ADC** **I**
When not used, this pin must be connected to ground.

RESET **Reset** **I**
Hard reset. This pin is active-HIGH. See Section Table 6.6, “Reset AC Timing Parameters,” page 6-5, for the minimum and maximum assertion time for a valid reset.

SD0[3:0] **SD0 Bus** **O 3-State**
The first 4-bit output bus used to output the high- and low-priority streams.

SD1[3:0] **SD1 Bus** **O 3-State**
The second 4-bit output bus used to output the high- and low-priority streams.

STARTOUT **First Soft Decision Mark** **O 3-State**
When asserted HIGH, this signal marks the first soft decision of an COFDM symbol to be presented off-chip.

5.4 Sigma-Delta Outputs

This section lists and describes the output signals to the L64705/L64724.

AGCOUT **AGC Output** **O Open Drain**
Sigma-Delta output of the AGC.

VCXOUT **O Open Drain**
Sigma Delta output of the VCXOUT.

AFCOUT **AFC Output** **O Open Drain**
Sigma Delta output of the AFCOUT.

5.5 MUX Signals

This section lists and describes the MUX input and output signals.

This interface is used for LSI Logic internal testing and is not intended for use in customer production receivers.

MUXIN[16:0] **Muxin Bus** **I Pull-Down**
This bus is combined with the 10-bit ADCIN[9:0] to form a 27-input MUXIN bus. When not used, this bus must be connected to ground.

CLKMUXIN **Clock for MUXIN** **I Clock**
This pin provides the clock to latch the MUXIN bus.

MUXOUT[26:0]
MUX Test Bus **O 3-State**
This 27-input bus is used for testing.

5.6 3-Wires Signals

This section lists and describes the 3-wire signals.

XCTR_OUT[2:0]
Tuner Control Output **O 3-State**
These three output pins are mainly used to control the tuner and are directly controlled through the microprocessor.

XCTR_IN[2:0] **Tuner Control Input** **I**
These three input pins collect information from the tuner. When not used, these pins must be connected to ground.

5.7 JTAG Signals

This section lists and describes the JTAG signals.

TCK **JTAG TAP Clock** **I Pull-Up**
When in normal operating mode, this pin must be connected to VDD.

TDI **JTAG TAP Test Data Input** **I Pull-UP**
When in normal operating mode, this pin must be connected to VDD.

TDO **JTAG TAP Test Data Output** **O 3-State**
JTAG TAP Test Data output.

TMS **JTAG TAP Test Mode Select** **I Pull-Up**
When in normal operating mode, this pin must be connected to VDD.

TRESETN **JTAG TAP Reset** **I Pull-Up**
When in normal operating mode, this pin must be connected to VDD.

5.8 Test Pins

This section lists and describes the test signals.

TEST0 **Test Selection 0** **I**
This pin is used for test selection. When in normal operating mode, this pin must be connected to ground.

TEST1 **Test Selection 1** **I**
This pin is used for test selection. When in normal operating mode, this pin must be connected to ground.

5.9 ASIC Pins

This section lists and describes the ASIC signals.

TTn **I**
This pin is active LOW and controls all the output pins. In normal operating mode, it must be connected to VDD.

TIDDTN **I**
This pin is active HIGH. In normal operating mode, it must be connected to ground.

PROCQ **O**
Dedicated output for ASIC characterization.

5.10 PLL Pins

This section lists and describes the PLL signals.

PLLVSS **Ground for Internal PLL** **I**
This signal must be connected to ground.

PLLVDD **VDD for Internal PLL** **I**
This signal must be connected to VDD.

PLLAGND **Analog Ground for Internal PLL** **I**
This signal must be connected to ground.

PLLLP2 **VCO Voltage Control** **I**
This signal must be connected to the external filter.

5.11 Tester Pins

This section lists and describes the internal tester signals.

PLLTSTCLK **I**

Pin dedicated to internal test purposes. In normal operating mode, this pin must be connected to ground.

PLLTSTSEL **I**

Pin dedicated to internal test purposes. In normal operating mode, this pin must be connected to ground.

Chapter 6
Specifications

This chapter describes the electrical specifications, power requirements, DC characteristics, and AC timing parameters for the L6780. It consists of the following sections:

6.1 Electrical Specifications

This section specifies the electrical requirements for L64780.

Table 6.1 lists the absolute maximum ratings for the L64780.

Table 6.1 Absolute Maximum Ratings

Parameter	Symbol	Limits[1]	Unit
DC Supply Voltage	V_{DD}	–0.3 to +3.9	V
LVTTL Input Voltage	V_{IN}	–1.0 to V_{DD} + 0.3	V
5 V Compatible Input Voltage	V_{IN}	–1.0 to 6.5	V
DC Input Current	I_{IN}	± 10	mA
Storage Temperature Range (Plastic)	T_{STG}	–40 to +125	°C

1. The ratings in this table are those beyond which permanent device damage is likely to occur. These values should not be used as the limits for normal device operation.

Table 6.2 lists the recommended operating conditions for the L64780.

Table 6.2 Recommended Operating Conditions

Parameter	Symbol	Limits[1]	Unit
DC Supply Voltage	V_{DD}	+3.0 to +3.6	V
Operating Ambient Temperature Range	T_A	0 to +70	°C

1. For normal device operation, adhere to the limits in this table. Sustained operation of the device at conditions exceeding these values, even if they are within the absolute maximum rating limits, can result in permanent device damage or impaired device reliability. Device functionality to stated DC and AC limits is not guaranteed if conditions exceed recommended operating conditions.

Table 6.3 lists the DC characteristics of L64780, which is produced with the LCBG10p process. This is a 0.35-micron drawn gate length cell-based process. Characteristics in the table are the same for any device that has a buffer with the listed parameters.

Table 6.3 DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IL}	Input Low Voltage		V_{SS} – 0.5		0.8	V
V_{IH}	Input High Voltage	LVTTL Temp Range	2.0		V_{DD} +0.3	V
		5-V Compatible	2.0		5.5	V
V_T	Switching Threshold			1.4	2.0	V
V_{T+}	Schmitt Trigger, Positive-going Threshold			1.7	2.0	V
V_{T-}	Schmitt Trigger, Negative-going Threshold		0.8	1.0		V
	Schmitt Trigger, Hysteresis		0.6	0.7		V
I_{IN}	Input Current Inputs with Pulldown Resistors Inputs with Pullup Resistors	$V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$	–10 35 -35	± 1 115 –115	10 222 –214	mA mA mA

Table 6.3 DC Characteristics (Cont.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage					
	Type B1	I_{OH} = -1 mA[2]	2.4		V_{DD}	V
	Type B2	I_{OH} = -2 mA[3]	2.4		V_{DD}	V
	Type B4	I_{OH} = -4 mA[3]	2.4		V_{DD}	V
	Type B6	I_{OH} = -6 mA[3]	2.4		V_{DD}	V
	Type B8	I_{OH} = -8 mA[3]	2.4		V_{DD}	V
	Type B12[1]	I_{OH} =-12 mA[3]	2.4		V_{DD}	V
V_{OL}	Output Low Voltage					
	Type B1	I_{OL} = 1 mA		0.2	0.4	V
	Type B2	I_{OL} = 2 mA		0.2	0.4	V
	Type B4	I_{OL} = 4 mA		0.2	0.4	V
	Type B6	I_{OL} = 6 mA		0.2	0.4	V
	Type B8	I_{OL} = 8 mA		0.2	0.4	V
	Type B12[2]	I_{OL} =12 mA		0.2	0.4	V
I_{OZ}	3-state Output Leakage Current	$V_{OH} = V_{SS}$ or V_{DD}	–10	± 1	10	mA
I_{OS}	Output Short Circuit Current[3, BT4]	$V_O = V_{DD}$			140	mA
		$V_O = V_{SS}$			–40	mA
	Output Short Circuit, BT4F	$V_O = V_{DD}$			67	mA
		$V_O = V_{SS}$			–86	mA
I_{DD}	Quiescent Supply Current	$V_{IN} = V_{DD}$ or V_{SS}				
I_{CC}	Dynamic Supply Current		tbd			mA
C_{IN}	Input Capacitance[4]	Input and Bidirectional Buffers	2.5			pF
		5-volt Compatible	3.0			pF
C_{OUT}	Output Capacitance[5]	Output Buffer[5]	2.0			pF
		5-volt Compatible	3.0			pF

1. Requires two output pads.
2. See the “Interfacing to 5 V Signals Using G10®-p Technologies” application note for “F” series output buffer I_{OH} values.
3. Type B4 output. Output short circuit current for other outputs will scale.
4. Excluding package capacitance.
5. Output using single buffer structure (excluding package).

6.2 AC Timing

The following subsections provide the AC timing for the input data interface and output data interface.

6.2.1 Input Data Interface

Figure 6.1 shows the waveform timing for the input data interface.

Figure 6.1 Input Data AC Timing

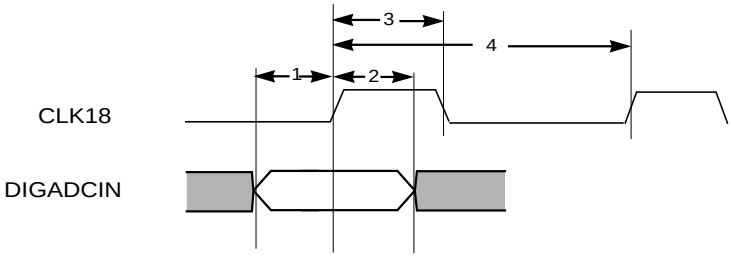


Table 6.4 lists the AC timings for the input data interface of the L64780.

Table 6.4 Input Data AC Timing Parameters

No.	Parameter	Description	Min	Max	Unit
1	t_s	Input Setup time to CLK18	6	–	ns
2	t_h	Input Hold time to CLK18	–	13	ns
3	t_{pwh}	Clock pulse width high	24.9	–	ns
4	t_{cycle}	Clock cycle time	55.5	–	ns

6.2.2 Output Data Interface

Figure 6.2 shows the waveform timing for the output data interface.

Figure 6.2 Output Data AC Timing

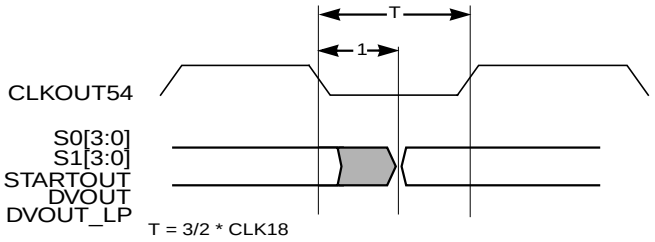


Table 6.5 lists the AC timing parameters for the output data interface of the L64780.

Table 6.5 Output Data AC Timing Parameters

	Parameter	Description	Min	Max	Unit
1	t_{od}	Output delay from CLKOUT54 falling edge	–	5.0	ns

6.2.3 Reset Timing

Figure 6.3 illustrates the reset timing for L64780. Table 6.6 lists and describes the output data AC timing parameters.

Figure 6.3 Reset Timing

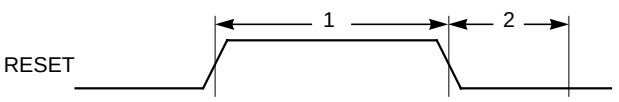


Table 6.6 Reset AC Timing Parameters

	Parameter	Description	Min	Max	Unit
1	t_{RWH}	Reset Pulse Width High	3	–	CLK18 cycles
2	t_{WK}	Wake-Up time (PLL acquisition time)	300	–	ms

6.3 Signal Specifications

Table 6.7 provides a summary of the pin numbers and their associated signals, grouped by function.

Table 6.7 Signal Summary List

Pin	Pin Name	Description	Buffer Type	5-Volt Comp-atible	Drive (mA)	Type	Active
Major I/Os							
99	CLK18	Input clock	LVTTL Input	Yes			–
20	RESET	Main Reset	LVTTL Input	Yes			High
34	CLKOUT54	Clock output to the L64705 or L64724	LVTTL Output	Yes			–
Microprocessor Interface							
125–9	A[4:0]	Address Bus[1]	LVTTL Input	Yes		Pull-Down	–
109–18	D[7:0]	Data Bus[2]	LVTTL Bidir	Yes	4		–
108	READ	Read/Write selection	LVTTL Input	Yes		Pull-Up	–
107	CSn	Chip Select	LVTTL Input	Yes		Pull-Up	Low
106	ASn	Address Strobe	LVTTL Input	Yes		Pull-Up	Low
35	DTACKn	Data Acknowledge	LVTTL Output	Yes	4	3-State	Low
36	INTn	Interrupt	LVTTL Output	Yes	4	Open Drain	Low
105	P_S	Serial/Parallel Mode	LVTTL Input	Yes			–

Table 6.7 Signal Summary List (Cont.)

Pin	Pin Name	Description	Buffer Type	5-Volt Comp-atible	Drive (mA)	Type	Active
Main Input							
144–142, 139, 138, 135–133, 131, 130	DIGIN[9:0]	Digital Input in normal mode. Testin input otherwise	LVTTL Input	Yes		Pull-Down	–
152	ADCPD	ADC Power Down	Analog Input	Yes			HIGH
153	ADCGVSS	Guard VSS Supply	Analog Input	Yes			–
154	ADCVSS	Analog VSS supply	Analog Input	Yes			–
155	ADCVREFP	Positive Reference Voltage	Analog Input	Yes			–
156	ADCVREFN	Negative Reference Voltage	Analog Input	Yes			–
157	AVIN	Analog Input when using the internal ADC	Analog Input	YES			–
158	IBIAS	Input bias current	Analog Input	Yes			–
159	ADCVDD	Analog VDD supply	Analog Input	Yes			–
160	ADCGVDD	Guard VDD Supply	Analog Input	Yes			–

Table 6.7 Signal Summary List (Cont.)

Pin	Pin Name	Description	Buffer Type	5-Volt Comp-atible	Drive (mA)	Type	Active
Main Output							
63	DVOUT	SD0 Data Valid Out	LVTTL Output	Yes	4	3-state	–
62	DVOUT_LP	SD1 Data Valid Out	LVTTL Output	Yes	4	3-state	–
61	STARTOUT	First Soft Decision Mark	LVTTL Output	Yes	4	3-state	–
56–8, 60	SD0[3:0]	SD0 Bus	LVTTL Output	Yes	4	3-state	–
51–3, 55	SD1[3:0]	SD1 Bus	LVTTL Output	Yes	4	3-state	–
PWM Output							
42	VCXOUT	VCXOUT Timing Loop	LVTTL Output	Yes	4	Open Drain	–
122	AFCOUT	Output to the Tuner	LVTTL Output	Yes	4	Open Drain	–
150	AGCOUT	Output to the AGC	LVTTL Output	Yes	6	Open Drain	–
Mux In Pins							
5, 6, 8–12, 14–18, 21–24, 26	MUXIN[16:0]	Input Mux. Combined with DIGADCIN to form 27 input bits	LVTTL Input	Yes		Pull-Down	–
50	CLKMUXIN	Clock output use to Generate MUXIN bus	LVTTL Output	Yes	4		–

Table 6.7 Signal Summary List (Cont.)

Pin	Pin Name	Description	Buffer Type	5-Volt Comp-atible	Drive (mA)	Type	Active
Mux Out							
64, 66–69, 71–74, 76–79, 82–85, 87–90, 92–97,	MUXOUT[26:0]	Output Mux: Mainly for test issues	LVTTL Output	Yes	4	3-state	–
3 Wires Buffer							
37–39	XCTR_OUT[2:0]	Pins used to control the Tuner	LVTTL Output	Yes	4	3-state	–
2–4	XCTR_IN[2:0]	Pins used to retrieve informations from Tuner	LVTTL Input	Yes			–
JTAG: Test Access Port (TAP)							
28	TCK	JTAG Tap Clock	LVTTL Input	Yes		Pull-Up	–
29	TMS	JTAG Tap Test Mode Select	LVTTL Input	Yes		Pull-Up	–
30	TDI	JTAG Tap Test Data Input	LVTTL Input	Yes		Pull-Up	–
33	TDO	JTAG Tap Test Data Output	LVTTL Output	Yes	4	3-state	–
27	TRESETN	JTAG Tap Reset	LVTTL Input	Yes		Pull-Up	Low
Test PLL; Scan Mode; Bist Mode							
46	TEST0	Test Mode Selection	LVTTL Input	Yes			–
47	TEST1	Test Mode Selection	LVTTL Input	Yes			–

Table 6.7 Signal Summary List (Cont.)

Pin	Pin Name	Description	Buffer Type	5-Volt Comp-atible	Drive (mA)	Type	Active
ASIC Specific Pins							
45	TTN	Control tn pins of all bidirectional and 3-state outputs	LVTTL Input	Yes			Low
140	TIDDTN	Control power down PLL, oscillator and disable pull up/pull down	LVTTL Input	Yes			High
147	PROCQ	Dedicated output of Procmon	LVTTL Output	Yes			–
Internal PLL Pins							
103	PLLVSS	PLL ground	Analog Input	Yes			–
100	PLLVDD	PLL power	Analog Input	Yes			–
102	PLLLP2	VCO control voltage pin, connection to external loop filter	Analog Bidir	Yes			–
101	PLLAGND	PLL analog ground	Analog Output	Yes			–
Tester Pins							
145	PLLTSTCLK	open pll loop	LVTTL Input	Yes			–
146	PLLTSTSEL	replace pll clk output and feedback loop	LVTTL Input	Yes			High

1. A0 is also used as the I^2C Serial Clock. Therefore Pin A0 is a Schmitt Buffer.
2. D0 is also used as the I^2C Serial Data. Therefore, Pin D0 is a Bidirectional Schmitt Buffer.

6.4 Pinouts

The following subsections provide a numerical and alphabetic listing of the L64780 pins, as well as a pinout package drawing showing the location of the pins.

6.4.1 Pin List

Table 6.8 numerically lists the L64780 pins and their associated signals.

Table 6.8 Pin List by Number

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
VDD	1	VSS	43	MUXOUT10	85	A2	127
XCTR_IN0	2	VSS2	44	VSS	86	A1	128
XCTR_IN1	3	TTN	45	MUXOUT9	87	A0	129
XCTR_IN2	4	TEST0	46	MUXOUT8	88	DIGIN_0	130
MUXIN0	5	TEST1	47	MUXOUT7	89	DIGIN_1	131
MUXIN1	6	VDD	48	MUXOUT6	90	VDD	132
VSS2	7	VDD	49	VDD	91	DIGIN_2	133
MUXIN2	8	CLKMUXIN	50	MUXOUT5	92	DIGIN_3	134
MUXIN3	9	SD1_3	51	MUXOUT4	93	DIGIN_4	135
MUXIN4	10	SD1_2	52	MUXOUT3	94	VSS	136
MUXIN5	11	SD1_1	53	MUXOUT2	95	VDD	137
MUXIN6	12	VSS	54	MUXOUT1	96	DIGIN_5	138
VDD	13	SD1_0	55	MUXOUT0	97	DIGIN_6	139
MUXIN7	14	SD0_3	56	VSS	98	TIDDTN	140
MUXIN8	15	SD0_2	57	CLK18	99	VSS2	141
MUXIN9	16	SD0_1	58	PLLVDD	100	DIGIN_7	142
MUXIN10	17	VDD	59	PLLAGND	101	DIGIN_8	143
MUXIN11	18	SD0_0	60	PLLLP2	102	DIGIN_9	144
VSS2	19	STARTOUT	61	PLLVSS	103	PLLTSTCLK	145
RESET	20	DVOUT_LP	62	VSS2	104	PLLTSTSEL	146
MUXIN12	21	DVOUT	63	P_S	105	PROCQ	147
MUXIN13	22	MUXOUT26	64	ASn	106	VDD	148
MUXIN14	23	VSS	65	CSn	107	VDD	149
MUXIN15	24	MUXOUT25	66	READ	108	AGCOUT	150
VDD	25	MUXOUT24	67	D_7	109	VSS	151
MUXIN16	26	MUXOUT23	68	VDD	110	ADCPD	152
TRESETN	27	MUXOUT22	69	VDD	111	ADCGVSS	153
TCK	28	VDD	70	D_6	112	ADCVSS	154
TMS	29	MUXOUT21	71	D_5	113	ADCVREFP	155
TDI	30	MUXOUT20	72	D_4	114	ADCVREFN	156
VSS2	31	MUXOUT19	73	D_3	115	AVIN	157
VSS	32	MUXOUT18	74	D_2	116	IBIAS	158
TDO	33	VSS	75	D_1	117	ADCVDD	159
CLKOUT54	34	MUXOUT17	76	D_0	118	ADCGVDD	160
DTACKn	35	MUXOUT16	77	VSS	119		
INTn	36	MUXOUT15	78	VSS2	120		
XCTR_OUT0	37	MUXOUT14	79	VSS	121		
XCTR_OUT1	38	VDD	80	AFCOUT	122		
XCTR_OUT2	39	VDD	81	VDD	123		
VDD	40	MUXOUT13	82	VSS2	124		
VDD	41	MUXOUT12	83	A_4	125		
VCXOUT	42	MUXOUT11	84	A_3	126		

Table 6.9 alphabetically lists the L64780 signals and their associated pins.

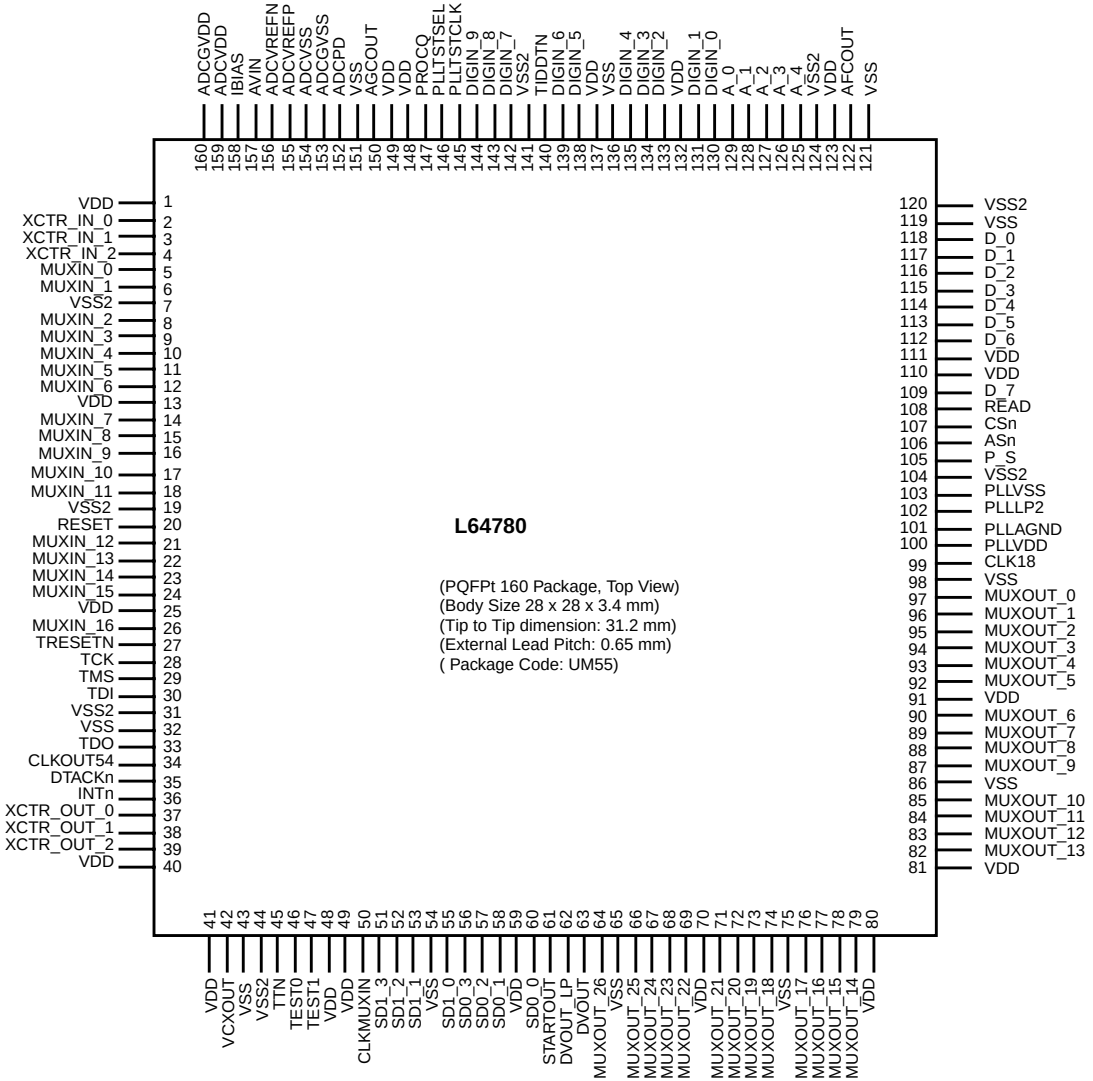
Table 6.9 Pin List by Name

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A0	129	INTn	36	MUXOUT24	67	VDD	137
A1	128	MUXIN0	5	MUXOUT25	66	VDD	149
A2	127	MUXIN1	6	MUXOUT26	64	VDD	1
A3	126	MUXIN2	8	PLLAGND	101	VDD	13
A4	125	MUXIN3	9	PLLLP2	102	VDD	25
ADCGVDD	160	MUXIN4	10	PLLTSTCLK	145	VDD	48
ADCGVSS	153	MUXIN5	11	PLLTSTSEL	146	VDD	110
ADCPD	152	MUXIN6	12	PLLVDD	100	VDD	132
ADCVDD	159	MUXIN7	14	PLLVSS	103	VDD	148
ADCVREFN	156	MUXIN8	15	PROCQ	147	VSS	32
ADCVREFP	155	MUXIN9	16	READ	108	VSS	43
ADCVSS	154	MUXIN10	17	RESET	20	VSS	54
AFCOUT	122	MUXIN11	18	P_S	105	VSS	65
AGCOUT	150	MUXIN12	21	SD0_0	60	VSS	75
ASn	106	MUXIN13	22	SD0_1	58	VSS	86
AVIN	157	MUXIN14	23	SD0_2	57	VSS	98
CLK18	99	MUXIN15	24	SD0_3	56	VSS	119
CLKMUXIN	50	MUXIN16	26	SD1_2	52	VSS	121
CLKOUT54	34	MUXOUT0	97	SD1_0	55	VSS	136
CSn	107	MUXOUT1	96	SD1_1	53	VSS	151
D0	118	MUXOUT2	95	SD1_3	51	VSS2	7
D1	117	MUXOUT3	94	STARTOUT	61	VSS2	19
D2	116	MUXOUT4	93	TCK	28	VSS2	31
D3	115	MUXOUT5	92	TDI	30	VSS2	44
D4	114	MUXOUT6	90	TDO	33	VSS2	104
D5	113	MUXOUT7	89	TEST0	46	VSS2	120
D6	112	MUXOUT8	88	TEST1	47	VSS2	124
D7	109	MUXOUT9	87	TIDDTN	140	VSS2	141
DIGIN0	130	MUXOUT10	85	TMS	29	XCTR_IN0	2
DIGIN1	131	MUXOUT11	84	TRESETN	27	XCTR_IN1	3
DIGIN2	133	MUXOUT12	83	TTN	45	XCTR_IN2	4
DIGIN3	134	MUXOUT13	82	VCXOUT	42	XCTR_OUT0	37
DIGIN4	135	MUXOUT14	79	VDD	40	XCTR_OUT1	38
DIGIN5	138	MUXOUT15	78	VDD	41	XCTR_OUT2	39
DIGIN6	139	MUXOUT16	77	VDD	49		
DIGIN7	142	MUXOUT17	76	VDD	59		
DIGIN8	143	MUXOUT18	74	VDD	70		
DIGIN9	144	MUXOUT19	73	VDD	80		
DTACKn	35	MUXOUT20	72	VDD	81		
DVOUT	63	MUXOUT21	71	VDD	91		
DVOUT_LP	62	MUXOUT22	69	VDD	111		
IBIAS	158	MUXOUT23	68	VDD	123		

6.4.2 Pin Layout

Figure 6.4 illustrates the L64780 package pin layout.

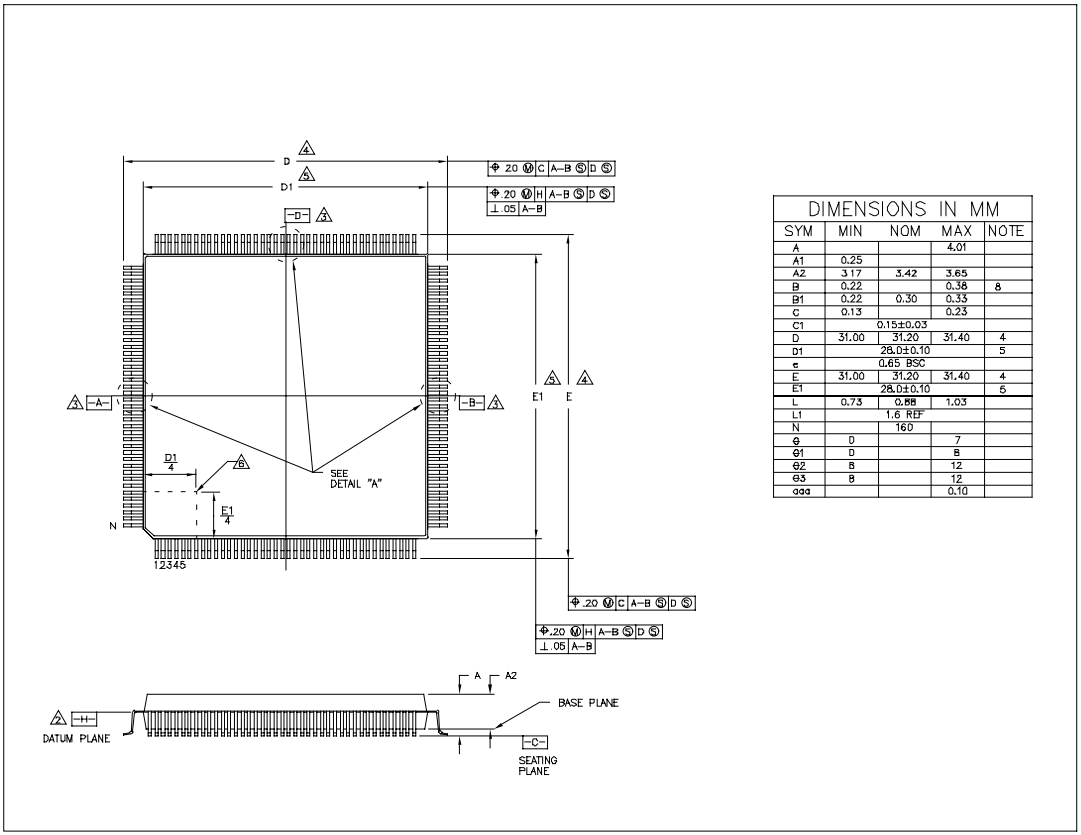
Figure 6.4 Package Pin Layout



6.5 Mechanical Drawing

Figure 6.5 shows the mechanical drawing for the L64780 160-pin PQFP.

Figure 6.5 160 PQFP Mechanical Drawing: Top and Side Views

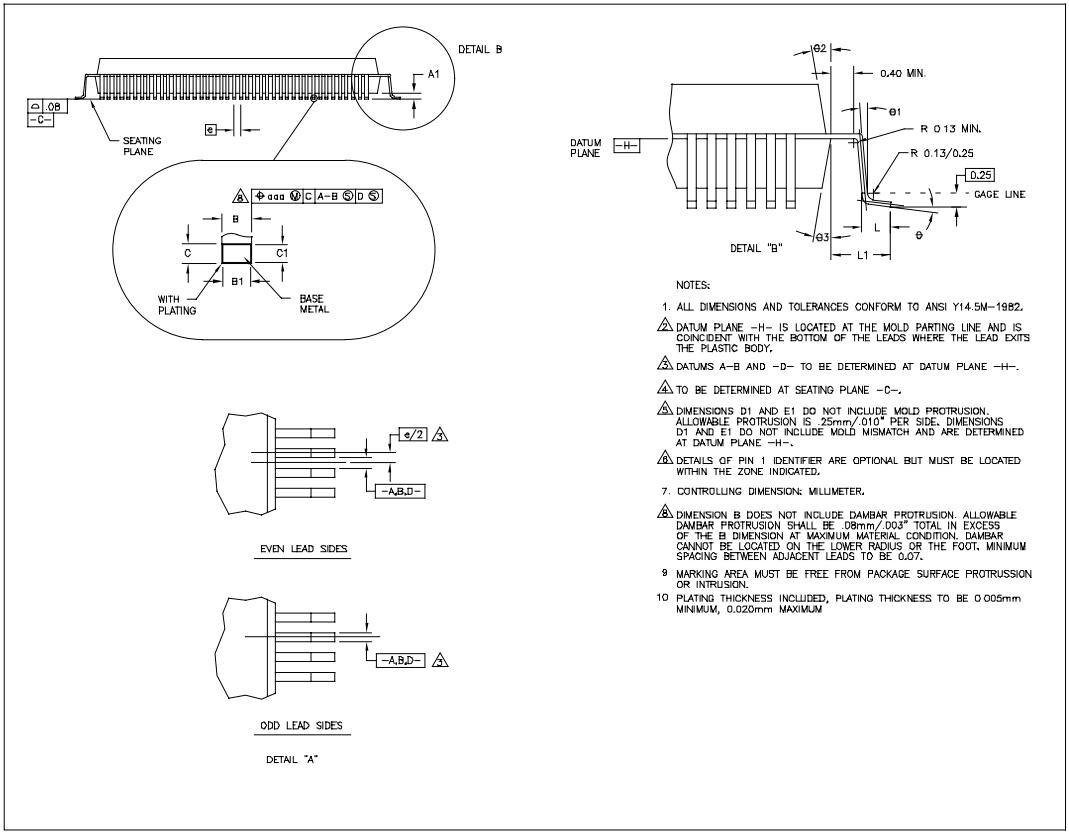


DIMENSIONS IN MM

SYM	MIN	NOM	MAX	NOTE
A			4.01	
A1	0.25			
A2	3.17	3.42	3.65	
B	0.22		0.38	8
B1	0.22	0.30	0.33	
C	0.13		0.23	
C1		0.15±0.03		
D	31.00	31.20	31.40	4
D1		28.0±0.10		5
e		0.65 BSC		
E	31.00	31.20	31.40	4
E1		28.0±0.10		5
L	0.73	0.88	1.03	
L1		1.6 REF		
N		160		
φ	0		7	
θ1	0		8	
θ2	5		12	
θ3	8		12	
aaa			0.10	

Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code UM55.**

Figure 6.6 160 PQFP Mechanical Drawing: Detail



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code UM55.**

Appendix A Programming the L64780 Using The Serial Bus Interface

This appendix discusses how to program the L64780 internal registers and data tables using the serial bus protocol. This appendix is intended primarily for system programmers who are developing software drivers using the serial bus.

It consists of the following sections:

A.1 Serial Bus Protocol Overview

The multimaster Serial bus interface has two one-bit lines: A0 (Serial Clock), and D0 (Serial Data). These are connected to the bus (see Figure A.1). External pullup resistors hold the bus at a logic 1 when it is not in operation. See the Serial Bus protocol documentation for a detailed explanation and electrical characteristics. D[7:1] are used to set the serial bus slave address. When using the serial bus, D[7:1] must be hardwired to set the appropriate device slave address.

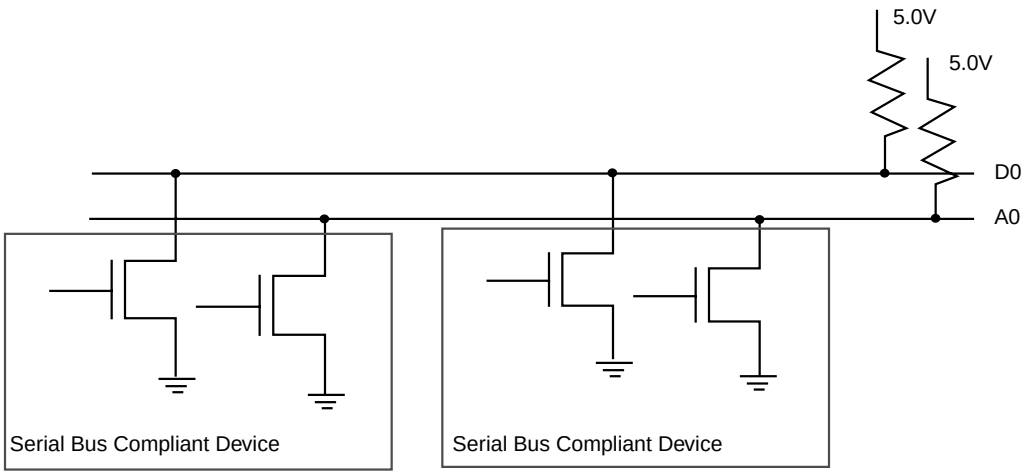
Select the serial bus mode on the L64780 by asserting P_S.

Features of the serial bus protocol include:

- Two one-bit lines: A0 and D0.
- D0: Serial Data.
- A0: serial clock (maximum frequency = 400 kHz).
- A0 and D0 have external pull-up resistors (the bus is normally HIGH).
- The Master always generates the clock, A0, and cycle start/stop conditions.

Figure A.1 provides an overview illustration of the serial bus.

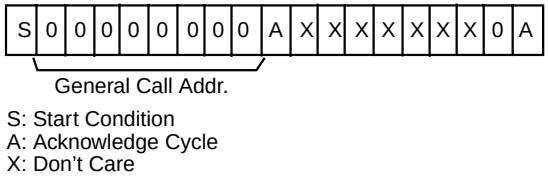
Figure A.1 Serial Bus Overview



A.2 Programming the Slave Address Using the Serial Bus

A general call (Master issues a start condition followed by eight zeroes) is used to address every device on the serial bus. Any device that requires information to be supplied through this general call must acknowledge the cycle.

Figure A.2 General Call Address



A.2.1 Write Cycle Using the Serial Bus

The following steps describe a write cycle using the serial bus.

1. The cycle is started by the Master issuing a start condition.
2. The 7-bit slave address is transmitted.
3. The R/W bit is reset to 0 and transmitted, indicating a write cycle.
4. The addressed Slave acknowledges the reception of the slave address by driving SDA LOW in the ACK cycle.
5. The Master sends the 8-bit address.
6. The addressed Slave acknowledges the reception of the address by driving SDA LOW in the ACK cycle.
7. The Master sends the 8-bit data.
8. The addressed Slave acknowledges the reception of the data by driving SDA LOW in the ACK cycle.
9. The Master terminates the cycle by issuing a stop condition.

A.2.2 Read Cycle Using the Serial Bus

1. The cycle is started with the start condition.
2. The 7-bit slave address is transmitted.
3. The R/W bit is reset to 0 and transmitted, indicating a write cycle.
4. The addressed Slave acknowledges the reception of the slave address by driving SDA LOW in the ACK cycle.
5. The Master sends the 8-bit address.
6. The addressed Slave acknowledges the reception of the address by driving SDA LOW in the ACK cycle.
7. The Master issues another start condition.
8. The 7-bit slave address is transmitted.
9. The R/W bit is set to 1 bit and transmitted, indicating a read cycle.
10. The addressed Slave acknowledges the reception of the slave address by driving SDA LOW in the ACK cycle.
11. The slave starts transmitting the data.
12. The Master must acknowledge receipt of the data by driving SDA LOW during the ACK cycle.
13. The Master terminates the cycle by issuing a stop condition.

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