Integrated Device Technology, Inc.

CMOS STATIC RAMS 256K (64K x 4-BIT)

Separate Data Inputs and Outputs

ADVANCE INFORMATION
IDT71281S/L
IDT71282S/L

FEATURES:

- Separate data inputs and outputs
- IDT71281S/L: outputs track inputs during write mode
- IDT71282S/L: high impedance outputs during write mode
- High speed (equal access and cycle time)
  - — Military: 30/35/45/55ns (max.)
  - — Commercial: 25/35/45ns (max.)
- Low power consumption
  - — IDT71281/2S
    Active: 400mW (typ.)
    Standby: 400µw (typ.)
  - — IDT71281/2L
    Active: 350mW (typ.)
    Standby: 100µw (typ.)
- Battery backup operation — 2V data retention (L version only)
- High-density 28-pin DIP, 28-pin SOJ, and 28-pin LCC
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (+10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-8831 Class B

DESCRIPTION:

The IDT71281/IDT71282 are 262,144-bit high-speed static RAMs organized as 64K x 4. They are fabricated using IDT's high-performance, high-reliability technology — CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

Access times as fast as 25ns are available with typical power consumption of only 350mW. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, this standby mode. The ultralow-power standby mode capability provides significant system level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 100µW operating off a 2V battery.

All inputs and outputs of the IDT71281/IDT71282 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT71281/IDT71282 are packaged in 28-pin sidebraze and plastic DIPs, SOJs and LCCs providing high board-level packing densities.

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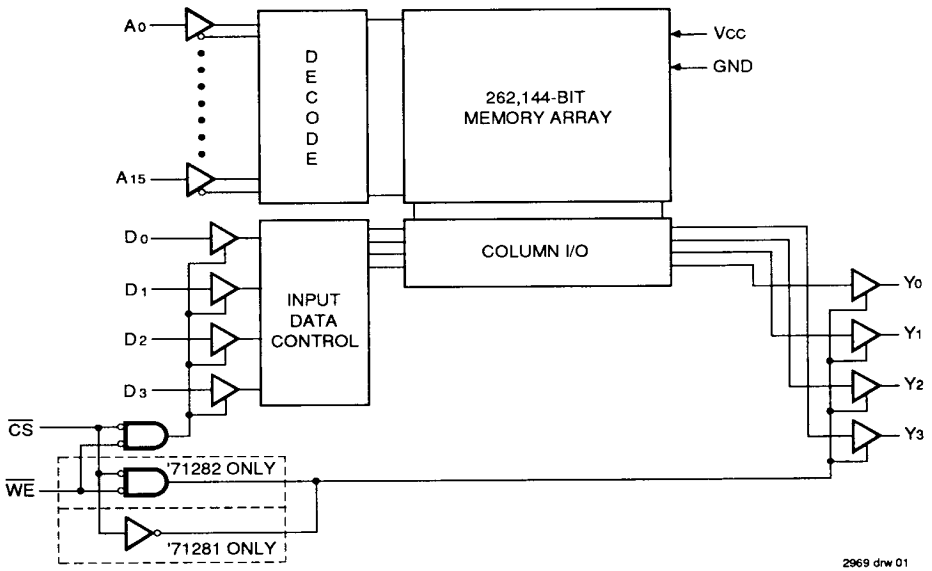
FUNCTIONAL BLOCK DIAGRAM

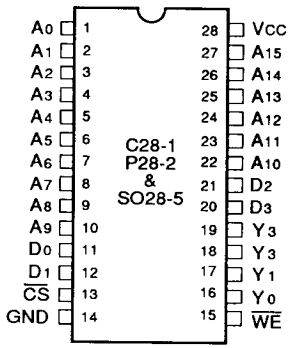


CEMOS is a trademark of Integrated Device Technology, Inc.

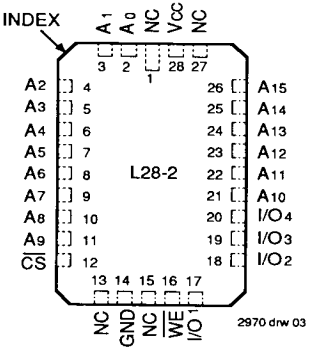
DESCRIPTION (Continued)

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP/SOJ
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A_0–A_{15}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
D_0–D_3	$DATA_{IN}$
Y_0–Y_3	$DATA_{OUT}$
GND	Ground

2969 tbl 01

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	D_{OUT}	Active
Write[1]	L	L	D_{IN}	Active
Write[2]	L	L	High-Z	Active

NOTE: 2969 tbl 02
1. For IDT71281 only.
2. For IDT71282 only.
3. H = V_{IH}, L = V_{IL}, X = Don't Care.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2969 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE: 2969 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2969 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. VIL (min.)= -3.0V for pulse width less than 20ns.

2969 tbl 06

DC ELECTRICAL CHARACTERISTICS(1)

(Vcc = 5V ± 10%, VLC = 0.2V, VHC = Vcc - 0.2V)

Symbol	Parameter	Power	71281/2S25 71281/2L25		71281/2S30 71281/2L30		71281/2S35 71281/2L35		71281/2S45 71281/2L45		71281/2S55 71281/2L55		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
ICC1	Operating Power Supply Current $\overline{CS}$ = VIL, Outputs Open Vcc = Max., f = 0(3)	S	130	—	—	140	120	130	120	130	—	130	mA
		L	120	—	—	130	110	120	110	120	—	120	
ICC2	Dynamic Operating Current $\overline{CS}$ = VIL, Outputs Open Vcc = Max., f = fMAX(2)	S	170	—	—	180	160	170	160	170	—	170	mA
		L	150	—	—	150	130	140	130	140	—	150	
ISB	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ VIH, Vcc = Max., Outputs Open, f = fMAX(2)	S	35	—	—	35	35	35	35	35	—	35	mA
		L	20	—	—	20	20	20	20	20	—	20	
ISB1	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ VHC, Vcc = Max., f = 0(2)	S	30	—	—	35	30	35	30	35	—	35	mA
		L	1.5	—	—	4.5	1.5	4.5	1.5	4.5	—	4.5	

NOTES:
1. All values are maximum guaranteed values.
2. At f = fMAX address and data inputs are cycling at the maximum frequency of read cycles of 1/tRC. f = 0 means no input lines change.

2969 tbl 07

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2969 tbl 08

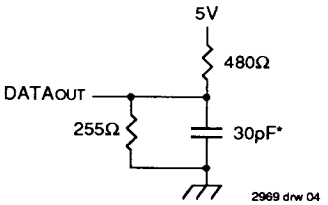


Figure 1. Output Load

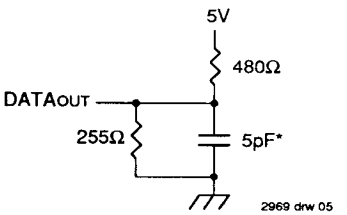


Figure 2. Output Load (for t_{CLZ}, t_{CHZ}, t_{OW}, and t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71281S/L Min.	IDT71281S/L Typ.(1)	IDT71281S/L Max.	IDT71282S/L Min.	IDT71282S/L Typ.	IDT71282S/L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL COM'L	— —	— —	10 5	— —	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL COM'L	— —	— —	10 5	— —	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min. I_{OL} = 10mA, V_{CC} = Min.		— —	— —	0.4 0.5	— —	— —	0.4 0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

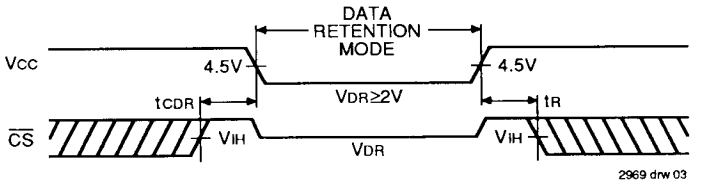
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.(1) Vcc @ 2.0v	Typ.(1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL. COM'L.	— —	50 50	75 75	2000 500	3000 750	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$		0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—	—	2	2	µA

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

2969 tbl 10

LOW Vcc DATA RETENTION WAVEFORM



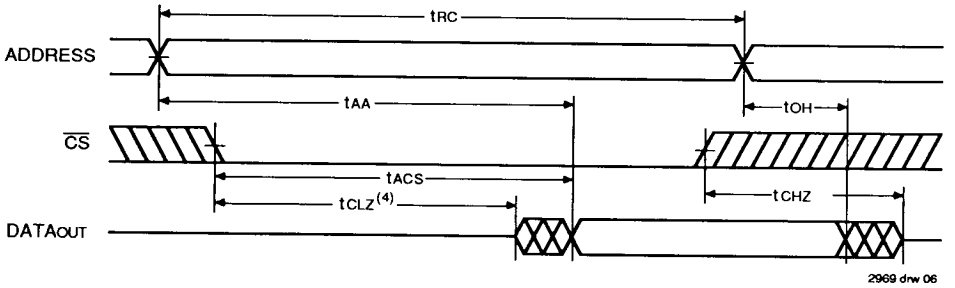
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71281S/L25(1) 71282S/L25(1) Min.	Max.	71281S/L30(2) 71282S/L30(2) Min.	Max.	71281S/L35 71282S/L35 Min.	Max.	71281S/L45 71282S/L45 Min.	Max.	71281S/L55(2) 71282S/L55(2) Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	25	—	30	—	35	—	45	—	55	—	ns
tAA	Address Access Time	—	25	—	30	—	35	—	45	—	55	ns
tACS	Chip Select Access Time(3)	—	25	—	30	—	35	—	45	—	55	ns
tCLZ	Chip Select to Output in Low Z(4)	5	—	5	—	5	—	5	—	5	—	ns
tCHZ	Chip Select to Output in High Z(4)	—	13	—	13	—	15	—	20	—	25	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
tPU	Chip Select to Power Up Time(4)	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power Down Time(4)	—	25	—	30	—	35	—	45	—	55	ns
Write Cycle												
tWC	Write Cycle Time	20	—	20	—	30	—	40	—	50	—	ns
tCW	Chip Select to End of Write(3)	20	—	20	—	30	—	40	—	50	—	ns
tAW	Address Valid to End of Write	20	—	20	—	30	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	20	—	30	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z(4,7)	—	13	—	13	—	15	—	20	—	25	ns
tDW	Data Valid to End of Write	15	—	15	—	20	—	25	—	30	—	ns
tDH	Data HoldTime	0	—	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write(4,7)	5	—	5	—	5	—	5	—	5	—	ns
tIY	Data Valid to Output Valid(4,6)	—	20	—	20	—	30	—	35	—	40	ns
tWY	Write Enable to Output Valid(4,6)	—	20	—	20	—	30	—	35	—	40	ns

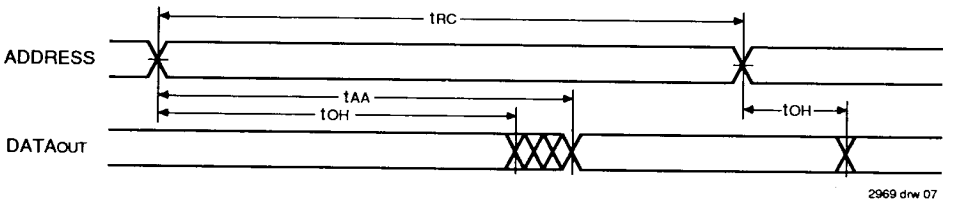
2969 tbl 11

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.
5. Preliminary data for military devices only.
6. For IDT71281S/L only.
7. For IDT71282S/L only.

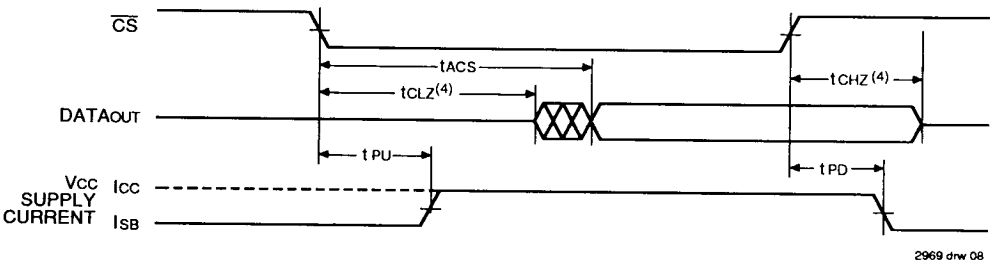
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2)

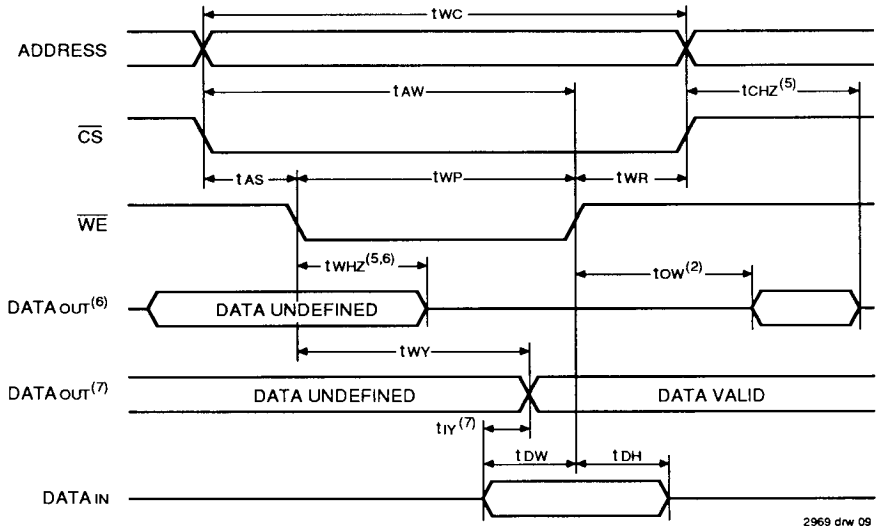


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3)

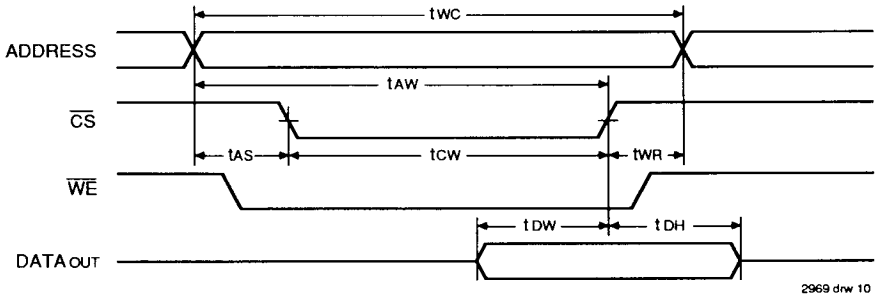


NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 4)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
6. IDT71282 only.
7. IDT71281 only.

ORDERING INFORMATION