IBM0364404 IBM03644B4

PC133 Synchronous DRAM - 64Mb Revision B

Features

- High Performance:

		-75A, CL=3	Units
f_{CK}	Clock Frequency	133	MHz
t_{CK}	Clock Cycle	7.5	ns
t_{AC}	Clock Access Time	5.4	ns
t_{RP}	Precharge Time	20	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	ns
t_{RC}	Bank Cycle Time	67.5	ns

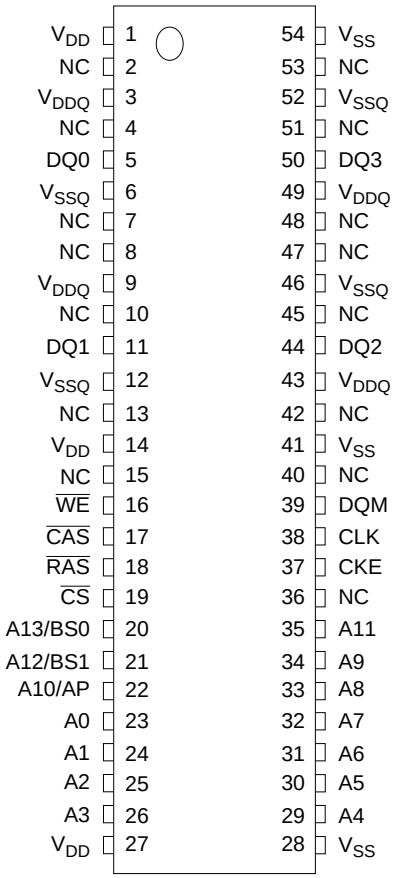
- Single Pulsed $\overline{RAS}$ Interface
- Fully Synchronous to Positive Clock Edge
- Four Banks controlled by Bank Selects
- Programmable Burst Length: 1, 2, 4, 8, full-page;
- Programmable CAS Latency: 3
- Programmable Wrap: Sequential or Interleave
- Multiple Burst Read with Single Write Option
- Automatic and Controlled Precharge Command
- Data Mask for Read/Write control
- Auto Refresh (CBR) and Self Refresh
- Suspend Mode and Power Down Mode
- Standard Power operation
- 4096 refresh cycles/64ms
- Random Column Address every CLK (1-N Rule)
- Single 3.3V ± 0.3V Power Supply
- LVTTL compatible
- Package: 54-pin 400 mil TSOP-Type II
  54-pin 2 High Stack TSOJ

Description

The IBM0364404CT3 is a four-bank 64Mb Synchronous DRAM organized as 4Mbit x 4 I/O x 4 Bank. IBM03644B4CT3 is a stacked version of the 64Mb, x 4 component.

This datasheet provides timing information for the 133 MHz performance sort for this synchronous device. For the complete functional description and timing diagrams refer to the datasheet 19L3264.

Pin Assignments for Planar Components (Top View)

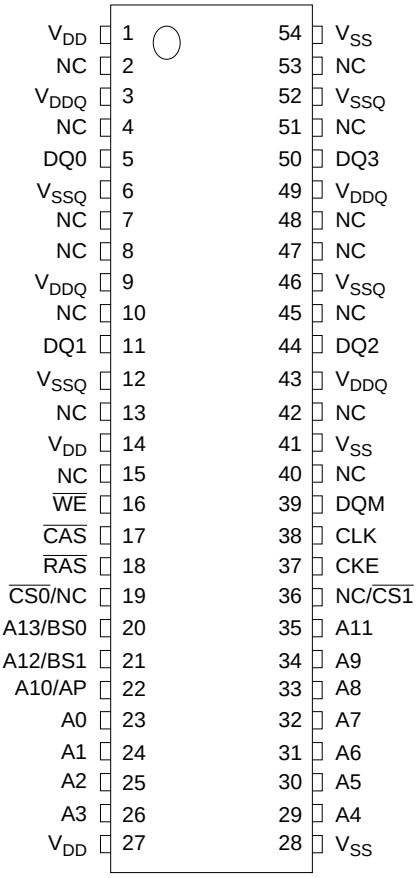


54-pin Plastic TSOP(II) 400 mil

4Mbit x 4 I/O x 4 Bank

IBM0364404CT3

Pin Assignments for 2 High Stack Package (Dual CS Pin) (Top View)



54-pin Plastic TSOJ(II) 400 mil

(4Mbit x 4 I/O x 4 Bank) x 2High

IBM03644B4CT3

***** $\overline{CS0}$ selects the lower DRAM in the stack.
***** $\overline{CS1}$ selects the upper DRAM in the stack.

Pin Description

CLK	Clock Input	DQ0-DQ3	Data Input/Output
CKE	Clock Enable	DQM	Data Mask
$\overline{CS}$ (2High Stack: $\overline{CS0}$, $\overline{CS1}$)	Chip Select	V_{DD}	Power (+3.3V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	V_{DDQ}	Power for DQs (+3.3V)
$\overline{WE}$	Write Enable	V_{SSQ}	Ground for DQs
BS1, BS0	Bank Select	NC	No Connection
A0-A11	Address Inputs	—	—

Input/Output Functional Description

Symbol	Type	Polarity	Function
CLK	Input	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Active High	CKE activates the CLK signal when high and deactivates the CLK signal when low. By deactivating the clock, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{CS}$, $\overline{CS0}$, $\overline{CS1}$	Input	Active Low	$\overline{CS}$ ($\overline{CS0}$, $\overline{CS1}$ for stacked devices) enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BS1, BS0	Input	—	Selects which bank is to be active.
A0 - A11	Input	—	During a Bank Activate command cycle, A0-A11 defines the row address when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address when sampled at the rising clock edge. A10 is used to invoke auto-precharge operation at the end of the burst read or write cycle. If A10 is high, auto-precharge is selected and BS0, BS1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10 is used in conjunction with BS0, BS1 to control which bank(s) to precharge. If A10 is high, all banks will be precharged regardless of the state of BS. If A10 is low, then BS0 and BS1 are used to define which bank to precharge.
DQ0-DQ3	Input-Output	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
DQM	Input	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. DQM low turns the output buffers on and DQM high turns them off. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.
V_{DD}, V_{SS}	Supply		Power and ground for the input buffers and the core logic.
V_{DDQ}, V_{SSQ}	Supply	—	Isolated power supply and ground for the output buffers to provide improved noise immunity.

Ordering Information - Planar Devices (Single $\overline{CS}$ Pin)

Part Number	CAS Latencies	Power Supply	Clock Cycle	Package	Org.
IBM0364404CT3B-75A	3	3.3V	7.5ns	400mil Type II TSOP-54	x4

Ordering Information - 2 High Stacked Devices (Dual $\overline{CS}$ Pin)

Part Number	CAS Latencies	Power Supply	Clock Cycle	Package	Org.
IBM03644B4CT3B-75A	3	3.3V	7.5ns	400mil Type II TSOJ-54	x4

Command Truth Table (See note 1)

Function	Device State	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	Bank Selects	A10	Address	Notes
		Previous Cycle	Current Cycle									
Mode Register Set	Idle	H	X	L	L	L	L	X	OP Code			
Auto (CBR) Refresh	Idle	H	H	L	L	L	H	X	X	X	X	
Entry Self Refresh	Idle	H	L	L	L	L	H	X	X	X	X	
Exit Self Refresh	Idle (Self-Refresh)	L	H	H	X	X	X	X	X	X	X	
				L	H	H	H					
Single Bank Precharge	See Current State Table	H	X	L	L	H	L	X	BS	L	X	2
Precharge all Banks	See Current State Table	H	X	L	L	H	L	X	X	H	X	
Bank Activate	Idle	H	X	L	L	H	H	X	BS	Row Address		2
Write	Active	H	X	L	H	L	L	X	BS	L	Column	2
Write with Auto-Precharge	Active	H	X	L	H	L	L	X	BS	H	Column	2
Read	Active	H	X	L	H	L	H	X	BS	L	Column	2
Read with Auto-Precharge	Active	H	X	L	H	L	H	X	BS	H	Column	2
Burst Termination	Active	H	X	L	H	H	L	X	X	X	X	3, 8
No Operation	Any	H	X	L	H	H	H	X	X	X	X	
Device Deselect	Any	H	X	H	X	X	X	X	X	X	X	
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X	4
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X	
Data Write/Output Enable	Active	H	X	X	X	X	X	L	X	X	X	5
Data Mask/Output Disable	Active	H	X	X	X	X	X	H	X	X	X	
Power Down Mode Entry	Idle/Active	H	L	H	X	X	X	X	X	X	X	6, 7
				L	H	H	H					
Power Down Mode Exit	Any (Power Down)	L	H	H	X	X	X	X	X	X	X	6, 7
				L	H	H	H					

1. All of the SDRAM operations are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, and DQM at the positive rising edge of the clock.Operation of both decks of a stacked device at the same time is allowed, depending on the operation being performed on the other deck. Refer to the Current State Truth Table.
2. Bank Select (BS0, BS1): BS0, BS1 = 0,0 selects bank 0; BS0, BS1 = 0,1 selects bank 1; BS0, BS1 = 1,0 selects bank 2; BS0, BS1 = 1,1 selects bank 3.
3. During a Burst Write cycle there is a zero clock delay, for a Burst Read cycle the delay is equal to the $\overline{CAS}$ latency.
4. During normal access mode, CKE is held high and CLK is enabled. When it is low, it freezes the internal clock and extends data Read and Write operations. One clock delay is required for mode entry and exit.
5. The DQM has two functions for the data DQ Read and Write operations. During a Read cycle, when DQM goes high at a clock timing the data outputs are disabled and become high impedance after a two clock delay. DQM also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibited (zero clock latency).
6. All banks must be precharged before entering the Power Down Mode.(If this command is issued during a burst operation, the device state will be Clock Suspend Mode.)The Power Down Mode does not perform any refresh operations, therefore the device can't remain in this mode longer than the Refresh period (t_{REF}) of the device. One clock delay is required for mode entry and exit.
7. A No Operation or Device Deselect command is required on the next clock edge following CKE going high.
8. Device state is full page burst operation. Use of this command to terminate other burst length operations is illegal.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Power Supply Voltage	-0.3 to +4.6	V	1
V_{DDQ}	Power Supply Voltage for Output	-0.3 to +4.6	V	1
V_{IN}	Input Voltage	-0.3 to V_{DD}+0.3	V	1
V_{OUT}	Output Voltage	-0.3 to V_{DD}+0.3	V	1
T_A	Operating Temperature (ambient)	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	1
V_{DDQ}	Supply Voltage for Output	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{DD} + 0.3	V	1, 2
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1, 3

1. All voltages referenced to V_{SS} and V_{SSQ}.
2. V_{IH} (max) = V_{DD}/V_{DDQ} + 1.2V for pulse width ≤ 5ns.
3. V_{IL} (min) = V_{SS}/V_{SSQ} - 1.2V for pulse width ≤ 5ns.

Capacitance (T_A = 25°C, f = 1MHz, V_{DD} = 3.3V ±0.3V)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
C_I	Input Capacitance (A0-A11, BS0, BS1, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, DQM)	2.5	2.9	3.8	pF	1
	Input Capacitance (CLK)	2.5	3.2	3.5		
C_O	Output Capacitance (DQ0 - DQ3)	4.0	5.4	6.5		

1. Multiply given planar values by 2 for 2-High stacked device except $\overline{CS}$.

DC Electrical Characteristics (T_A = 0 to +70°C, V_{DD} = 3.3V ±0.3V)

Symbol	Parameter	Min.	Max.	Units	Notes
$I_{I(L)}$	Input Leakage Current, any input (0.0V ≤ V_{IN} ≤ V_{DD}), All Other Pins Not Under Test = 0V	-1	+1	µA	1
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0V ≤ V_{OUT} ≤ V_{DDQ})	-1	+1	µA	1
V_{OH}	Output Level (LVTTL) Output “H” Level Voltage ($_{IOUT}$ = -2.0mA)	2.4	—	V	
V_{OL}	Output Level (LVTTL) Output “L” Level Voltage (I_{OUT} = +2.0mA)	—	0.4	V	

1. Multiply given planar values by 2 for 2-High stacked device.

Operating, Standby, and Refresh Currents (T_A = 0 to +70°C, V_{DD} = 3.3V ± 0.3V)

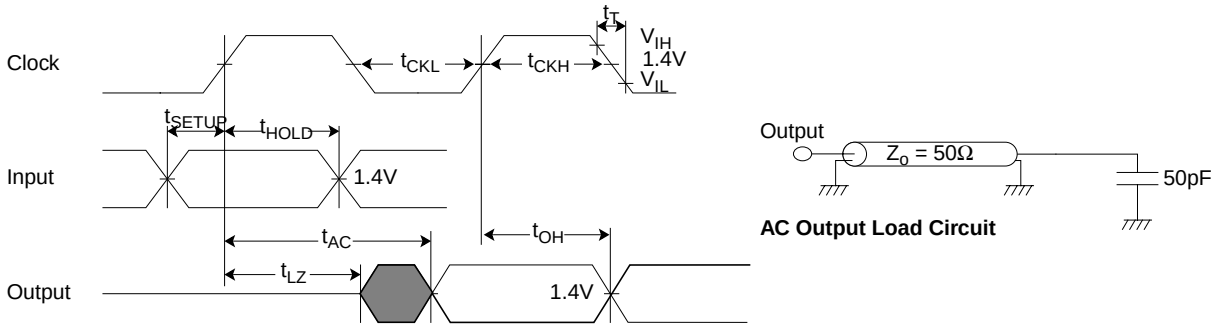
Parameter	Symbol	Test Condition	Speed -75A	Units	Notes
Operating Current	I_{CC1}	1 bank operation t_{RC} = t_{RC}(min), t_{CK} = min Active-Precharge command cycling without burst operation	75	mA	1, 2, 3
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CK} = min, $\overline{CS}$ =V_{IH}(min)	1	mA	1
	I_{CC2PS}	CKE ≤ V_{IL}(max), t_{CK} = Infinity, $\overline{CS}$ =V_{IH}(min)	1	mA	1
Precharge Standby Current in Non-Power Down Mode	I_{CC2N}	CKE ≥ V_{IH}(min), t_{CK} = min, $\overline{CS}$ =V_{IH} (min)	35	mA	1, 5
	I_{CC2NS}	CKE ≥ V_{IH}(min), t_{CK} = Infinity,	5	mA	1, 7
No Operating Current (Active state: 4 bank)	I_{CC3N}	CKE ≥ V_{IH}(min), t_{CK} = min, $\overline{CS}$ =V_{IH} (min)	40	mA	1, 5
	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CK} = min	7	mA	1, 6
Operating Current (Burst Mode)	I_{CC4}	t_{CK} = min, Read/ Write command cycling, Multiple banks active, gapless data,BL=4	120	mA	1, 3, 4
Auto (CBR) Refresh Current	I_{CC5}	t_{CK} = min, t_{RC} = t_{RC}(min) CBR command cycling	145	mA	1
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	1	mA	1

1. Currents given are valid for a single device. The total current for a stacked device depends on the operation being performed on the other deck.
2. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC}. Input signals are changed up to three times during t_{RC}(min).
3. The specified values are obtained with the output open.
4. Input signals are changed once during t_{CK}(min).
5. Input signals are changed once during three clock cycles.
6. Active Standby Current will be higher if Clock Suspend is entered during a burst read cycle (add 1mA per DQ).
7. Input signals are stable.

AC Characteristics (T_A = 0 to +70°C, V_{DD} = 3.3V ±0.3V)

1. See full specification (19L3264) for power-up requirements.
2. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
3. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC timing tests have V_{IL} = 0.8 V and V_{IH} = 2.0 V with the timing referenced to the 1.40V crossover point
5. AC measurements assume t_T = 1.2ns.

AC Characteristics Diagram



Clock and Clock Enable Parameters

Symbol	Parameter	-75A		Units	Notes
		Min.	Max.		
t_{CK3}	Clock Cycle Time, $\overline{CAS}$ Latency = 3	7.5	1000	ns	
t_{CK2}	Clock Cycle Time, $\overline{CAS}$ Latency = 2	—	—	ns	
t_{AC3}	Clock Access Time, $\overline{CAS}$ Latency = 3	—	5.4	ns	1
t_{AC2}	Clock Access Time, $\overline{CAS}$ Latency = 2	—	—	ns	1
t_{CKH}	Clock High Pulse Width	2.5	—	ns	
t_{CKL}	Clock Low Pulse Width	2.5	—	ns	
t_{CES}	Clock Enable Set-up Time	1.5	—	ns	
t_{CEH}	Clock Enable Hold Time	0.8	—	ns	
t_{SB}	Power down mode Entry Time	0	7.5	ns	
t_T	Transition Time (Rise and Fall)	0.5	10	ns	

1. Access time is measured at 1.4V.

Common Parameters

Symbol	Parameter	-75A		Units	Notes
		Min.	Max.		
t_{CS}	Command Setup Time	1.5	—	ns	
t_{CH}	Command Hold Time	0.8	—	ns	
t_{AS}	Address and Bank Select Set-up Time	1.5	—	ns	
t_{AH}	Address and Bank Select Hold Time	0.8	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	—	ns	1
t_{RC}	Bank Cycle Time	67.5	—	ns	1
t_{RAS}	Active Command Period	45	100K	ns	1
t_{RP}	Precharge Time	20	—	ns	1
t_{RRD}	Bank to Bank Delay Time	15	—	ns	1
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time	1	—	CLK	

1. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Mode Register Set Cycle

Symbol	Parameter	-75A		Units	Notes
		Min.	Max.		
t_{RSC}	Mode Register Set Cycle Time	2	—	CLK	1

1. These parameters account for the number of clock cycles and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Read Cycle

Symbol	Parameter	-75A		Units	Notes
		Min.	Max.		
t_{OH}	Data Out Hold Time	2.7	—	ns	1
t_{LZ}	Data Out to Low Impedance Time	0	—	ns	
t_{HZ}	Data Out to High Impedance Time	3	5.4	ns	2
t_{DQZ}	DQM Data Out Disable Latency	2	—	CLK	

1. Data Out Hold Time with no load must meet 1.8ns.
2. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

Refresh Cycle

Symbol	Parameter	-75A		Units
		Min.	Max.	
t_{REF}	Refresh Period	—	64	ms
t_{RFC}	Row Refresh Cycle Time	75	—	ns
t_{SREX}	Self Refresh Exit Time	10	—	ns

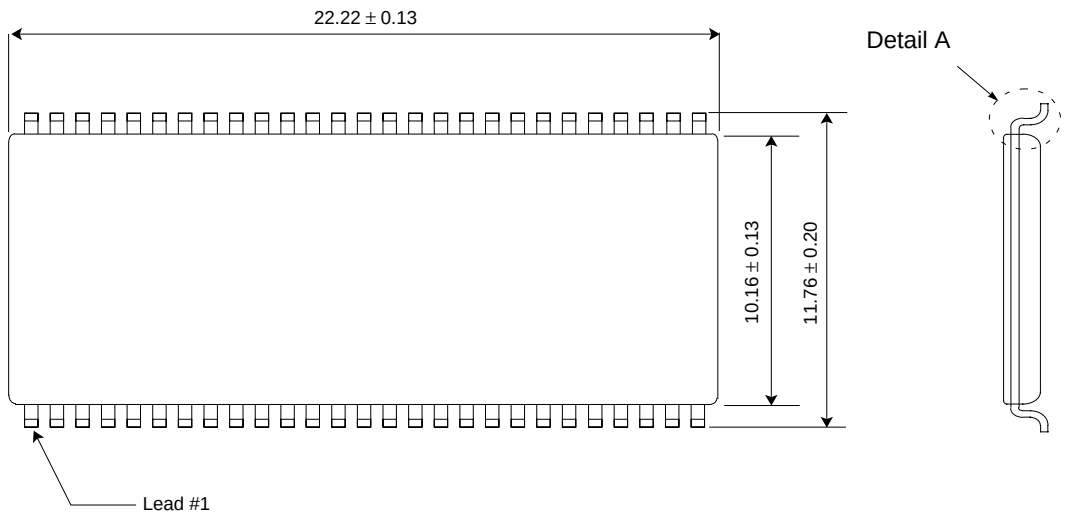
Write Cycle

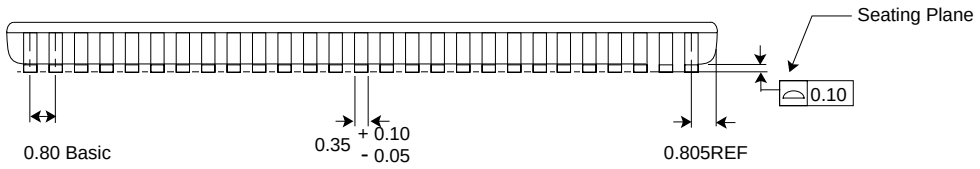
Symbol	Parameter	-75A		Units
		Min.	Max.	
t_{DS}	Data In Set-up Time	1.5	—	ns
t_{DH}	Data In Hold Time	0.8	—	ns
t_{DPL}	Data input to Precharge	2	—	CLK
t_{DAL}	Data input to Activate	5	—	CLK
t_{DQW}	DQM Write Mask Latency	0	—	CLK

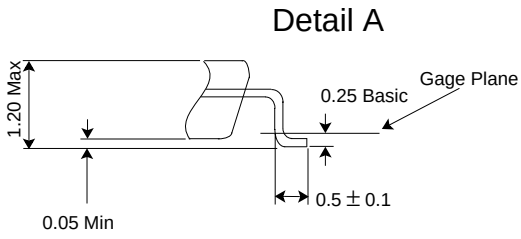
Clock Frequency and Latency

Symbol	Parameter	-75A	Units
f_{CK}	**Clock Frequency**	**133**	**MHz**
t_{CK}	Clock Cycle Time	7.5	ns
t_{AA}	$\overline{CAS}$ Latency	**3**	CLK
t_{RP}	Precharge Time	**3**	CLK
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	**3**	CLK
t_{RC}	Bank Cycle Time	9	CLK
t_{RAS}	Minimum Bank Active Time	6	CLK
t_{DPL}	Data In to Precharge	2	CLK
t_{DAL}	Data In to Active	5	CLK
t_{RRD}	Bank to Bank Delay Time	2	CLK
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time	1	CLK
t_{WL}	Write Latency	0	CLK
t_{DQW}	DQM Write Mask Latency	0	CLK
t_{DQZ}	DQM Data Disable Latency	2	CLK
t_{CSL}	Clock Suspend Latency	1	CLK

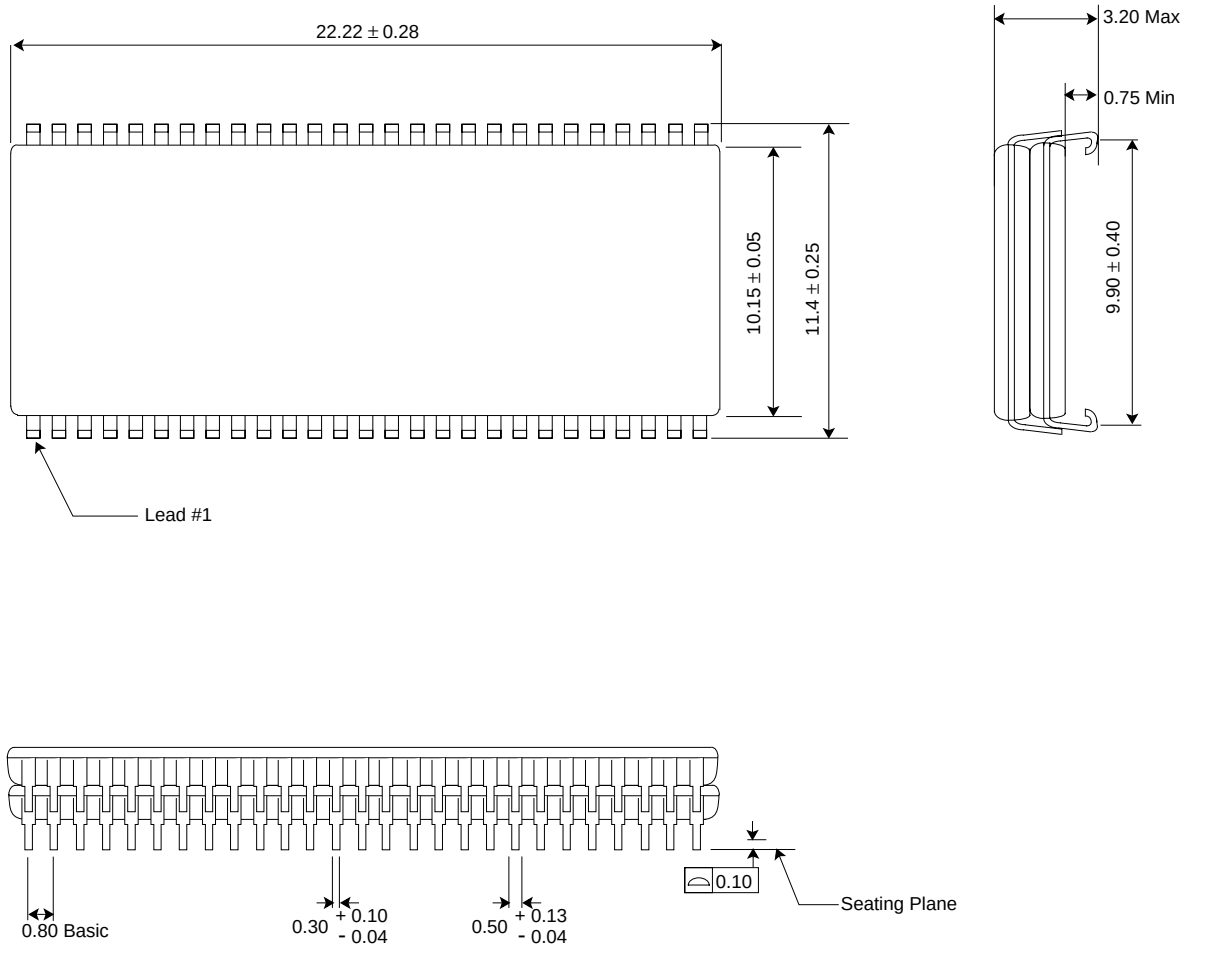
Package Dimensions (400mil; 54 lead; Thin Small Outline Package)







Stack Package Dimensions (400mil; 54 lead; 2 High Stack; Thin Small Outline J Lead Package)



Revision Log

Revision	Contents of Modification
1/14/99	Initial release.
3/1/99	Remove - 75D, 64Mb Rev C, and 256Mb Rev A.
3/21/99	Change t_{RP}, t_{RCD} for -75A (22.5 to 20ns).
7/99	Removed Preliminary.

Discontinued (8/99 - last order; 12/99 - last ship)

For more information contact your IBM Microelectronics sales representative or visit us on World Wide Web at http://www.chips.ibm.com

IBM Microelectronics manufacturing is ISO 9000 compliant.