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# HM621100A Series

1048576-word × 1-bit High Speed CMOS Static RAM

# HITACHI

Rev. 0.0  
Dec. 1, 1995

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## Description

The Hitachi HM621100A is a high speed 1M Static RAM organized as 1048576-word × 1-bit. It realizes high speed access time (20/25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU. The HM621100A, packaged in a 400-mil plastic SOJ is available for high density mounting.

## Features

- Single 5 V supply and high density 28-pin package (DIP and SOJ)
- High speed  
Access time: 20/25/35 ns (max)
- Low power dissipation  
Active mode: 350 mW (typ)  
Standby mode: 100 μW (typ)
- Completely static memory required  
No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible  
All inputs and outputs

## Ordering Information

Type No.	Access Time	Package
HM621100AP-20	20 ns	400-mil 28-pin plastic DIP (DP-28C)
HM621100AP-25	25 ns	
HM621100AP-35	35 ns	
HM621100ALP-20	20 ns	
HM621100ALP-25	25 ns	
HM621100ALP-35	35 ns	
HM621100AJP-20	20 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM621100AJP-25	25 ns	
HM621100AJP-35	35 ns	
HM621100ALJP-20	20 ns	
HM621100ALJP-25	25 ns	
HM621100ALJP-35	35 ns	

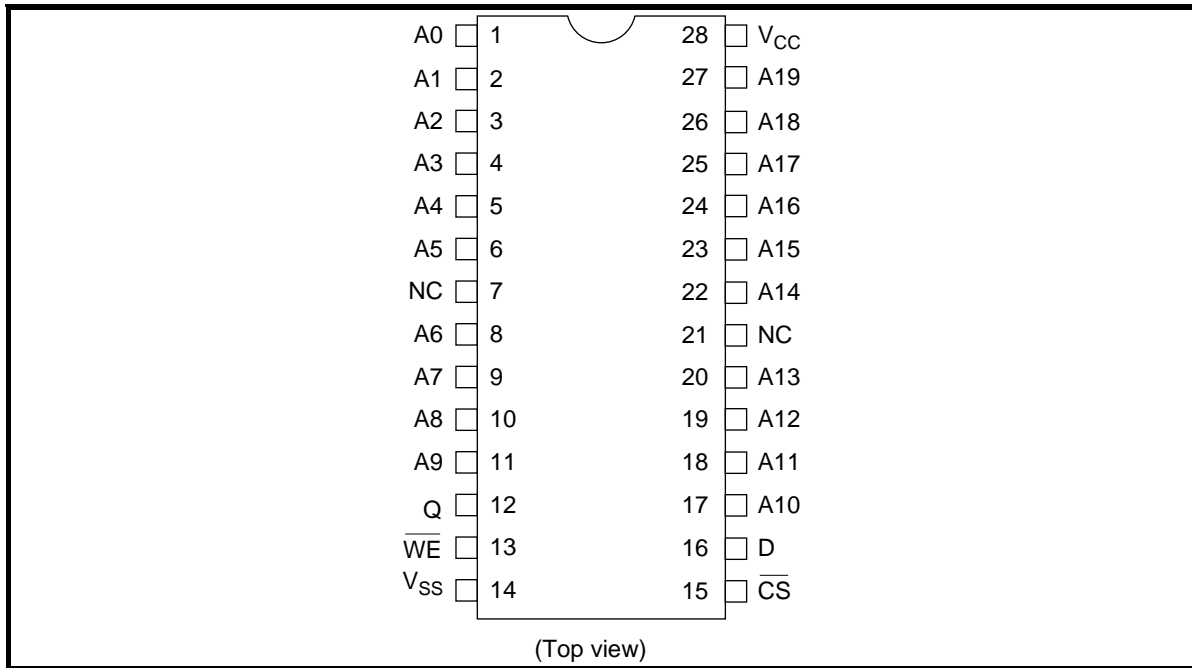
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## HM621100A Series

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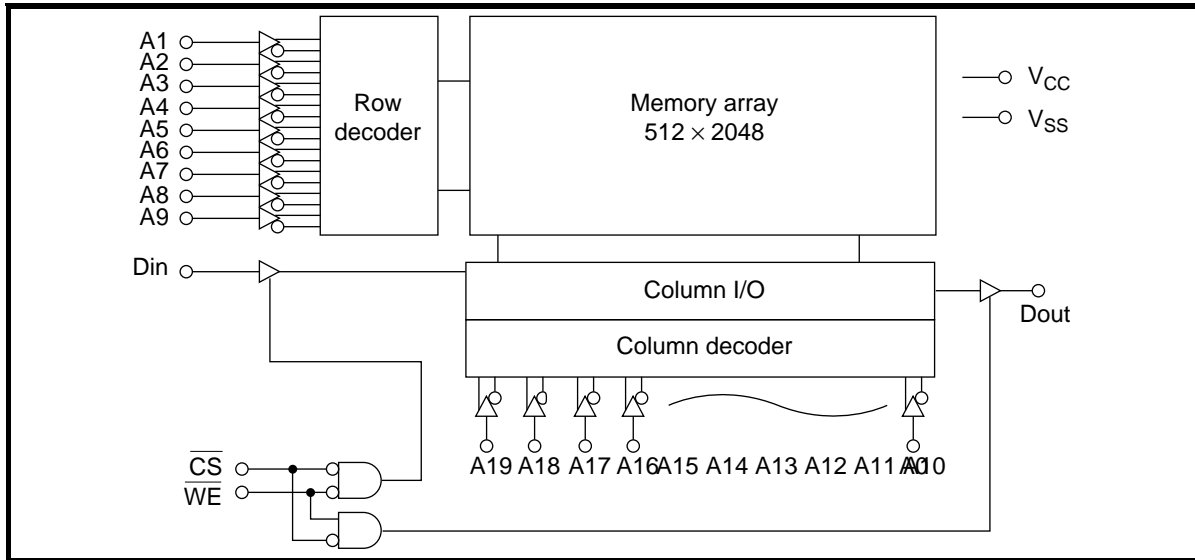
### Pin Arrangement



### Pin Description

Pin Name	Function
A0 – A19	Address
D	Input
Q	Output
CS	Chip select
WE	Write enable
V <sub>cc</sub>	Power supply
V <sub>ss</sub>	Ground

Block Diagram



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### Function Table

CS	WE	Mode	V <sub>CC</sub> Current	Output Pin	Ref. Cycle
H	X	Not selected	I <sub>SB</sub> , I <sub>SB1</sub>	High-Z	—
L	H	Read	I <sub>CC</sub>	Dout	Read cycle
L	L	Write	I <sub>CC</sub>	High-Z	Write cycle

Note: X : H or L

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V <sub>SS</sub>	V <sub>in</sub>	-0.5 <sup>1</sup> to +7.0	V
Power dissipation	P <sub>T</sub>	1.0	W
Operating temperature range	T <sub>opr</sub>	0 to +70	°C
Storage temperature range	T <sub>stg</sub>	-55 to +125	°C
Storage temperature range under bias	T <sub>bias</sub>	-10 to +85	°C

Note: 1. V<sub>in</sub> min = -2.0 V for pulse width ≤ 10 ns.

### Recommended DC Operating Conditions (T<sub>a</sub> = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
	V <sub>SS</sub>	0	0	0	V
Input high (logic 1) voltage	V <sub>IH</sub>	2.2	—	6.0	V
Input low (logic 0) voltage	V <sub>IL</sub>	-0.5 <sup>1</sup>	—	0.8	V

Note: 1. V<sub>IL</sub> min = -2.0 V for pulse width ≤ 10 ns.

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### DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V)

Parameter	Symbol	HM621100A-20			HM621100A-25/35			Unit	Test Conditions
		Min	Typ <sup>*1</sup>	Max	Min	Typ <sup>*1</sup>	Max		
Input leakage current	I <sub>Li</sub>	—	—	2.0	—	—	2.0	μA	V <sub>CC</sub> = max Vin = V <sub>SS</sub> to V <sub>CC</sub>
Output leakage current	I <sub>Lo</sub>	—	—	2.0	—	—	2.0	μA	CS = V <sub>IH</sub> V <sub>IO</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Operating power supply current	I <sub>CC</sub>	—	—	150	—	—	120	mA	CS = V <sub>IL</sub> , I <sub>IO</sub> = 0 mA, min cycle
Standby power supply current	I <sub>SB</sub>	—	—	60	—	—	40	mA	CS = V <sub>IH</sub> , min cycle
Standby power supply current (1)	I <sub>SB1</sub> <sup>*2</sup>	—	0.02	2.0	—	0.02	2.0	mA	CS ≥ V <sub>CC</sub> - 0.2 V 0 V ≤ Vin ≤ 0.2 V or Vin ≥ V <sub>CC</sub> - 0.2 V
	I <sub>SB1</sub> <sup>*3</sup>	—	—	100	—	—	100	μA	
Output low voltage	V <sub>OL</sub>	—	—	0.4	—	—	0.4	V	I <sub>OL</sub> = 8 mA
Output high voltage	V <sub>OH</sub>	2.4	—	—	2.4	—	—	V	I <sub>OH</sub> = -4 mA

Notes: 1. Typical values are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and not guaranteed.

2. P and JP version

3. LP and LJP version

### Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	5 <sup>*2</sup> 6 <sup>*3</sup>	pF	Vin = 0 V
Output capacitance	Cout	—	8	pF	Vout = 0 V

Notes: 1. This parameter is sampled and not 100% tested.

2. SOJ package

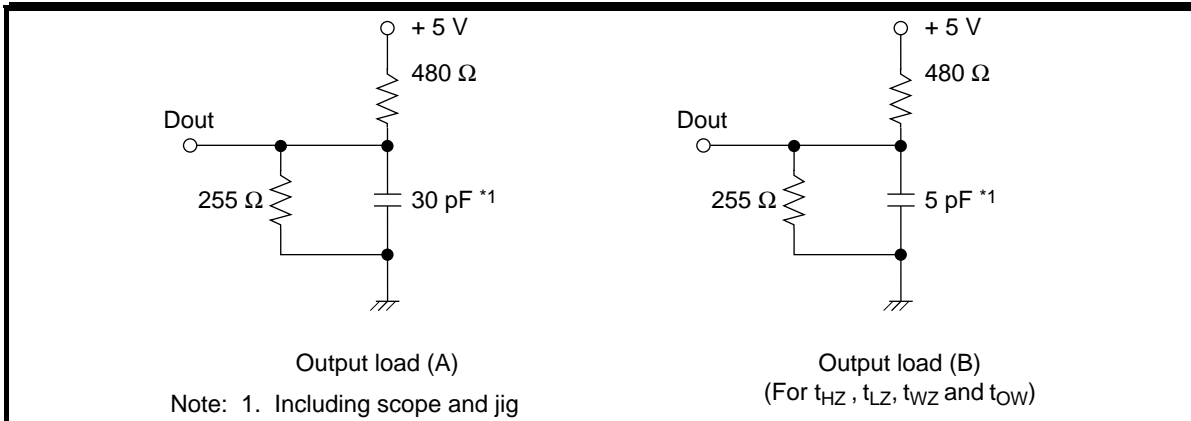
3. DIP package

### AC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, unless otherwise noted.)

#### Test Conditions

- \_ Input pulse levels: 0 V to 3.0 V
- \_ Input rise and fall time: 4 ns
- \_ Input timing reference levels: 1.5 V
- \_ Output timing reference levels: 1.5 V
- \_ Output load: See figures

## HM621100A Series

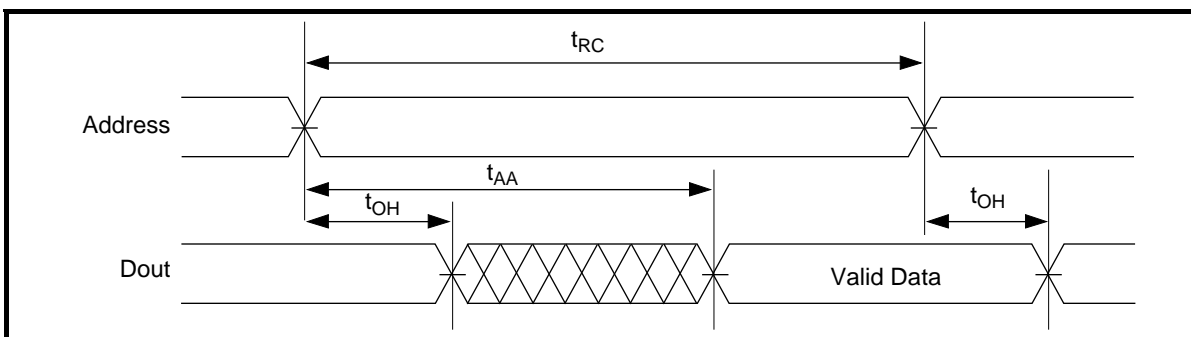


### Read Cycle

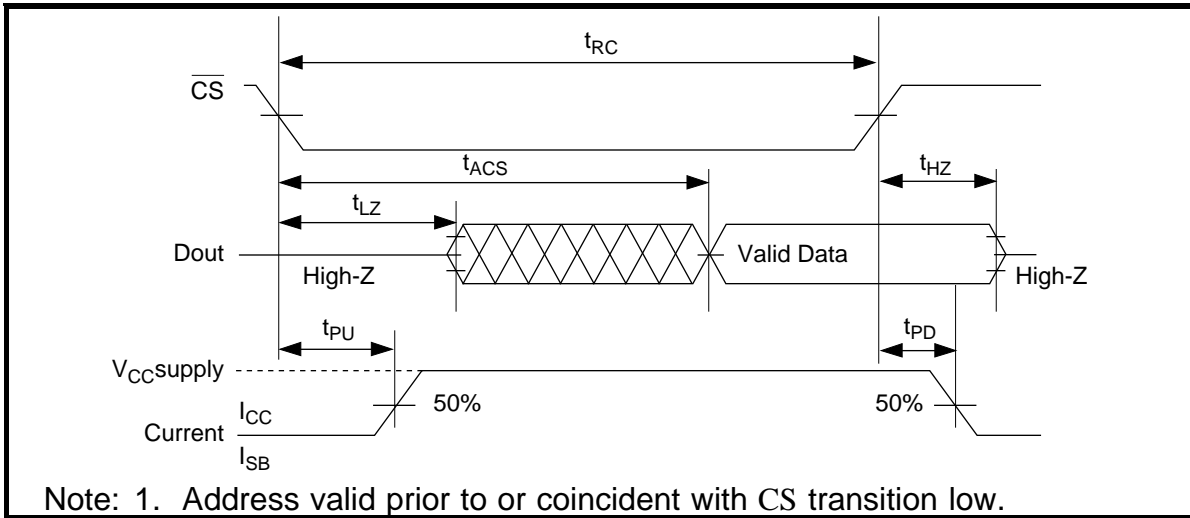
Parameter	Symbol	HM621100A-20		HM621100A-25		HM621100A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	$t_{RC}$	20	—	25	—	35	—	ns
Address access time	$t_{AA}$	—	20	—	25	—	35	ns
Chip select access time	$t_{ACS}$	—	20	—	25	—	35	ns
Chip selection to output in low-Z	$t_{LZ}^{-1}$	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	$t_{HZ}^{-1}$	0	10	0	12	0	15	ns
Output hold from address change	$t_{OH}$	5	—	5	—	5	—	ns
Chip selection to power up time	$t_{PU}$	0	—	0	—	0	—	ns
Chip deselection to power down time	$t_{PD}$	—	12	—	15	—	25	ns

Note: 1. Transition is measured  $\pm 200$  mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

### Read Timing Waveform (1) ( $\overline{WE} = V_{IH}$ , $\overline{CS} = V_{IL}$ )



Read Timing Waveform (2)\*1 ( $\overline{WE} = V_{IH}$ )



Write Cycle

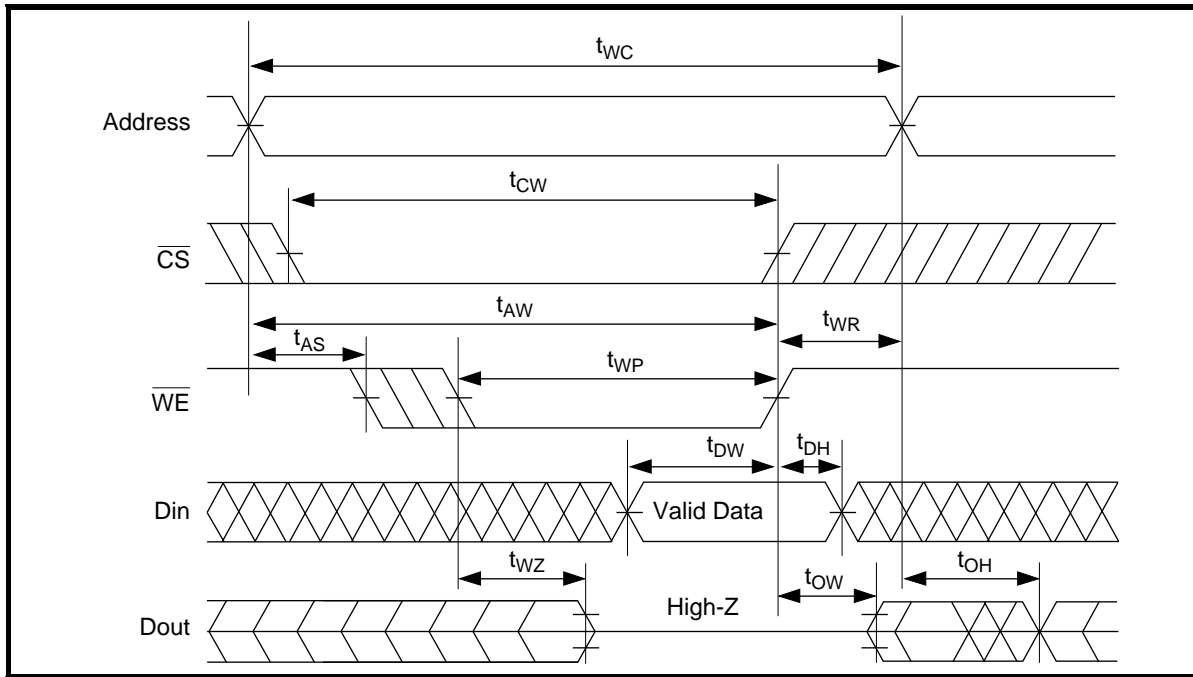
Parameter	Symbol	HM621100A-20		HM621100A-25		HM621100A-35		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	$t_{WC}$	20	—	25	—	35	—	ns
Chip selection to end of write	$t_{CW}$	15	—	17	—	25	—	ns
Address valid to end of write	$t_{AW}$	16	—	20	—	30	—	ns
Address setup time	$t_{AS}$	0	—	0	—	0	—	ns
Write pulse width	$t_{WP}^{*2}$	15	—	17	—	25	—	ns
Write recovery time	$t_{WR}^{*3}$	0	—	0	—	0	—	ns
Write to output in high-Z	$t_{WZ}^{*1}$	0	12	0	15	0	15	ns
Data to write time overlap	$t_{DW}$	12	—	15	—	20	—	ns
Data hold from write time	$t_{DH}$	0	—	0	—	0	—	ns
Output active from end of write	$t_{OW}^{*1}$	0	—	0	—	0	—	ns
Output hold from address change	$t_{OH}^{*4}$	5	—	5	—	5	—	ns

Notes: 1. Transition is measured  $\pm 200$  mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

2. A write occurs during the overlap of a low CS and a low WE.
3.  $t_{WR}$  is measured from the earlier of CS or WE going high to the end of write cycle.
4. Dout is the same phase of write data of this write cycle, if  $t_{WR}$  is long enough.

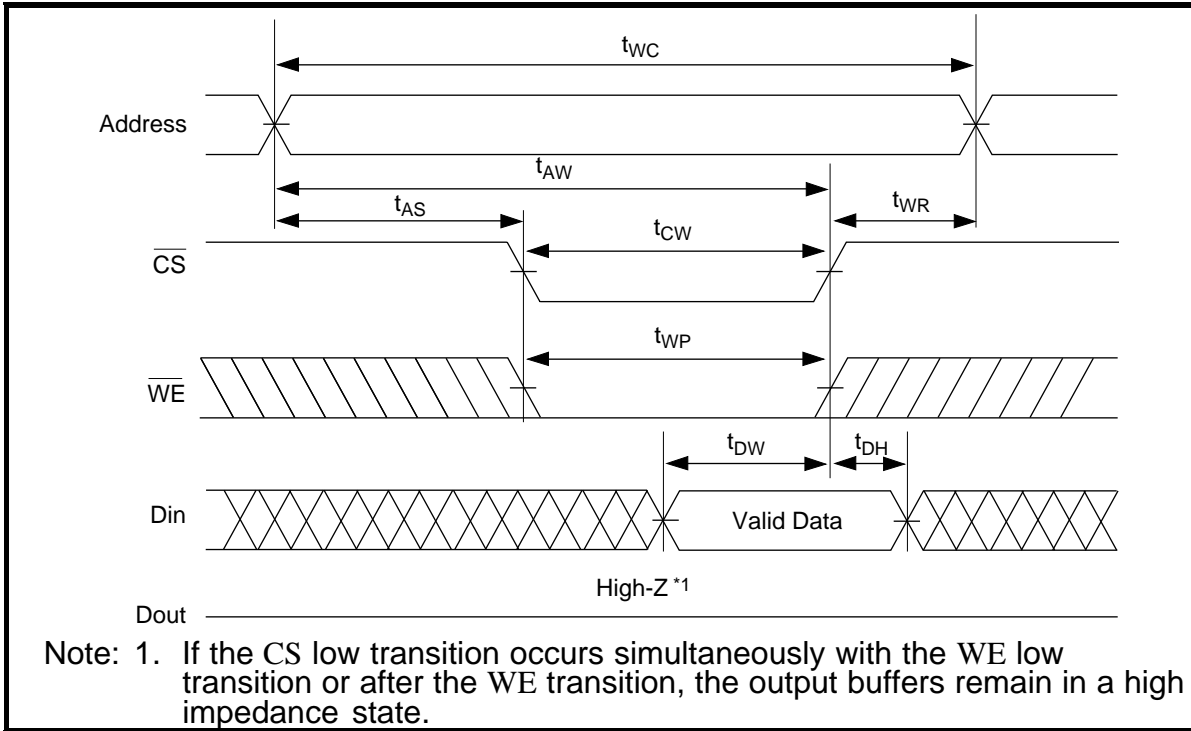
# HM621100A Series

## Write Timing Waveform (1) ( $\overline{WE}$ Controlled)





Write Timing Waveform (2) ( $\overline{CS}$  Controlled)



Low  $V_{CC}$  Data Retention Characteristics ( $T_a = 0$  to  $+70^\circ\text{C}$ )

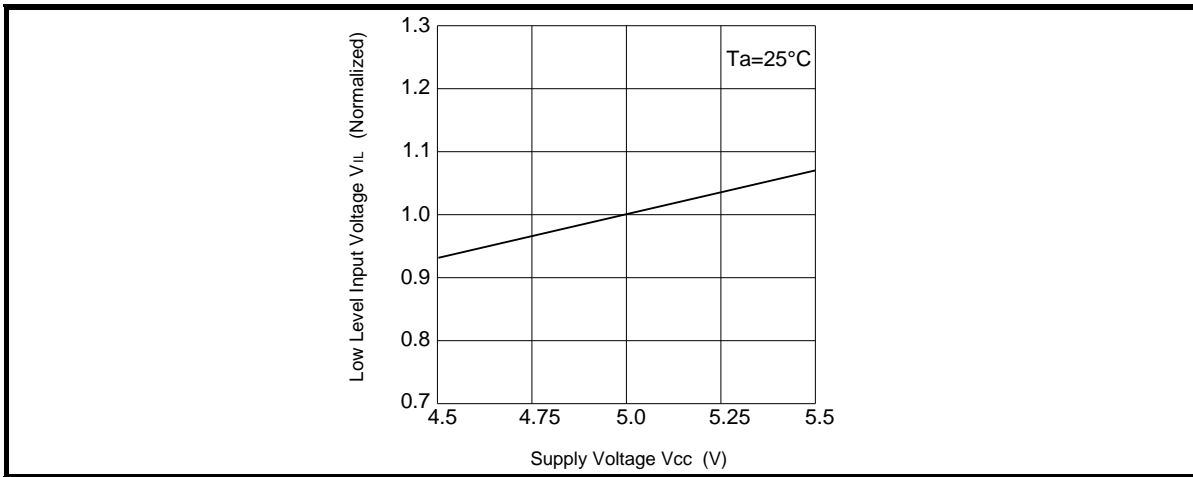
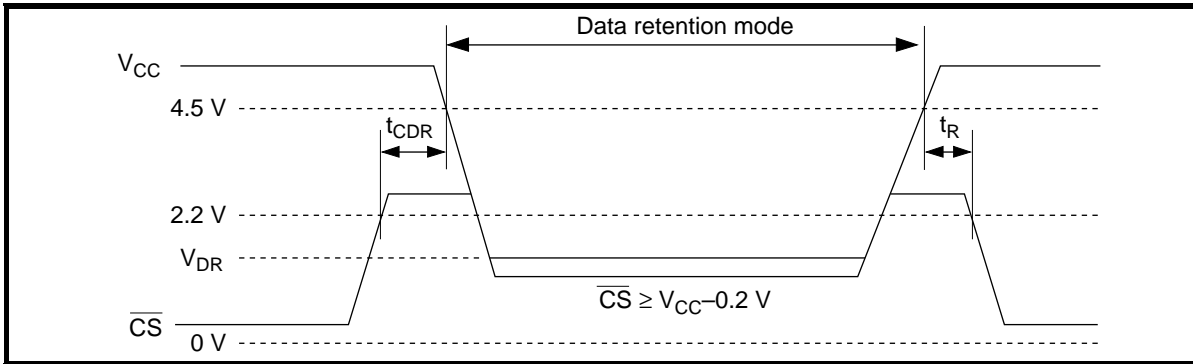
This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$CS \geq V_{CC} - 0.2 \text{ V}$ , $V_{in} \geq V_{CC} - 0.2 \text{ V}$ or $0 \text{ V} \leq V_{in} \leq 0.2 \text{ V}$
Data retention current	$I_{CCDR}$	—	2	$50^{*1}$	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	
Operation recovery time	$t_R$	5	—	—	ms	

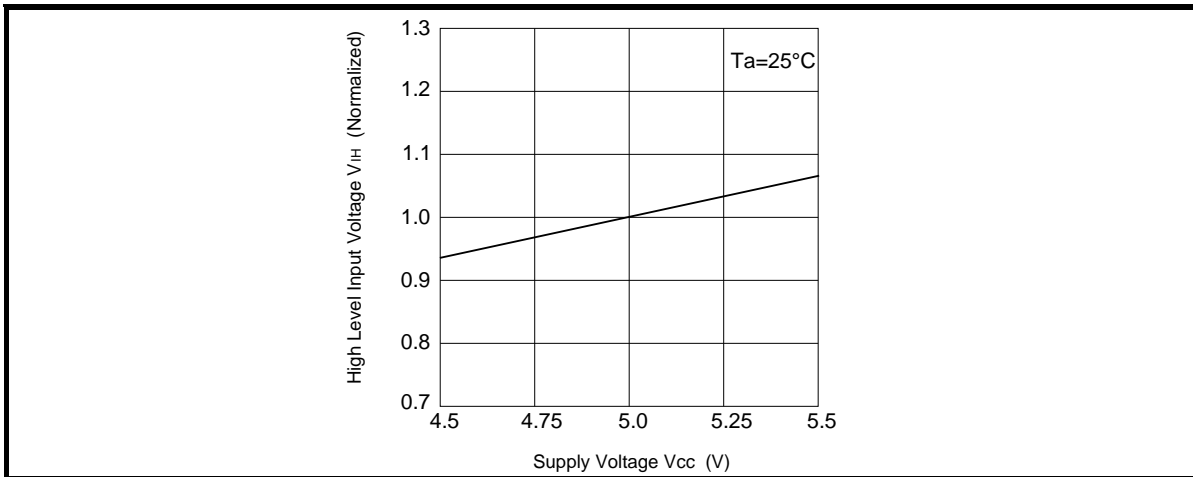
Note: 1.  $V_{CC} = 3.0 \text{ V}$

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## Low $V_{CC}$ Data Retention Timing Waveform

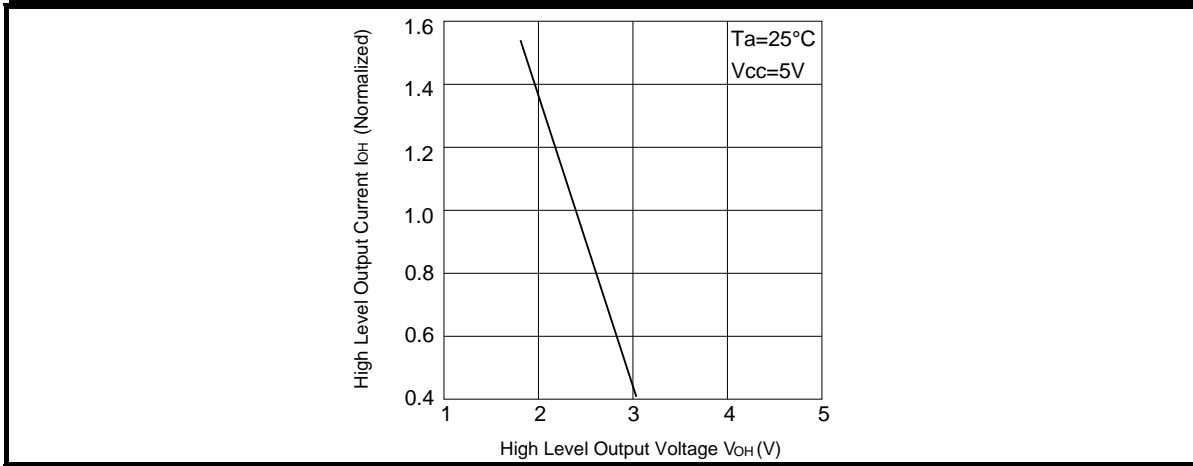


Low Level Input Voltage vs. Supply Voltage

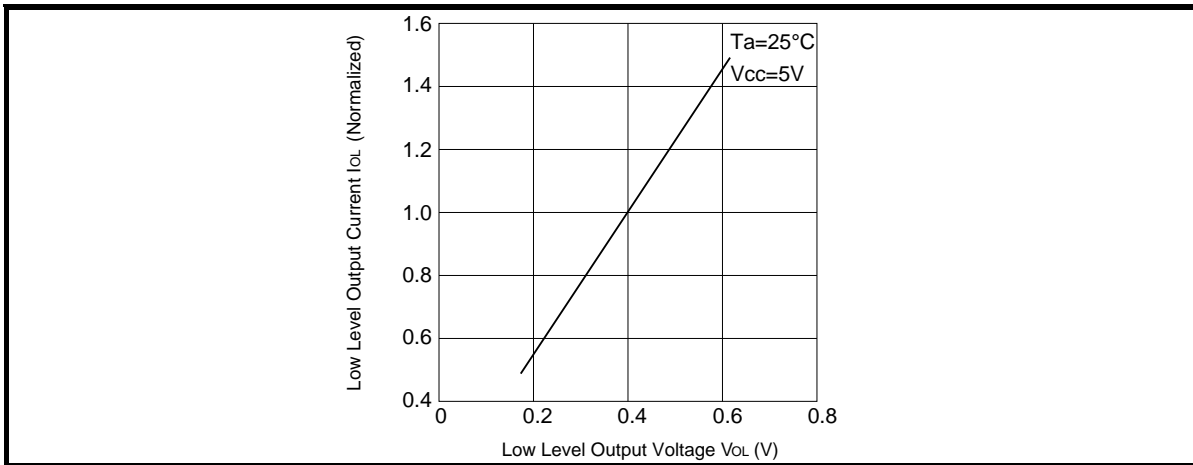


High Level Input Voltage vs. Supply Voltage

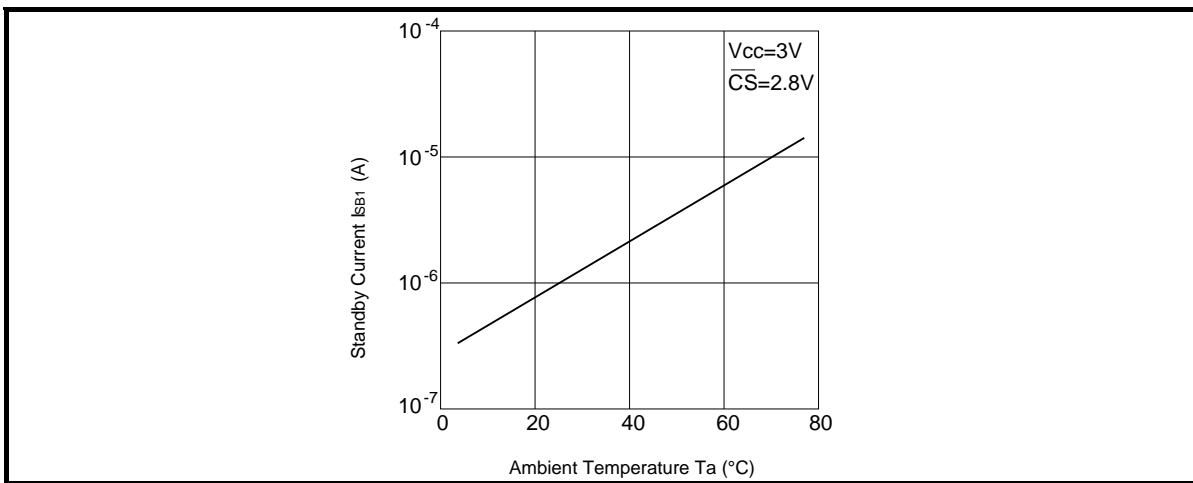
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**High Level Output Current vs. High Level Output Voltage**

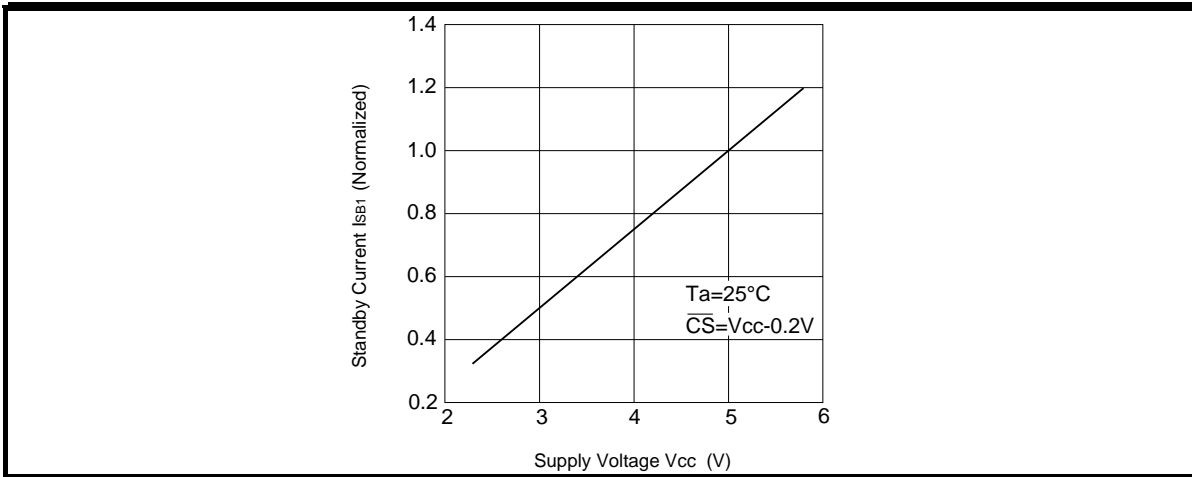


**Low Level Output Current vs. Low Level Output Voltage**

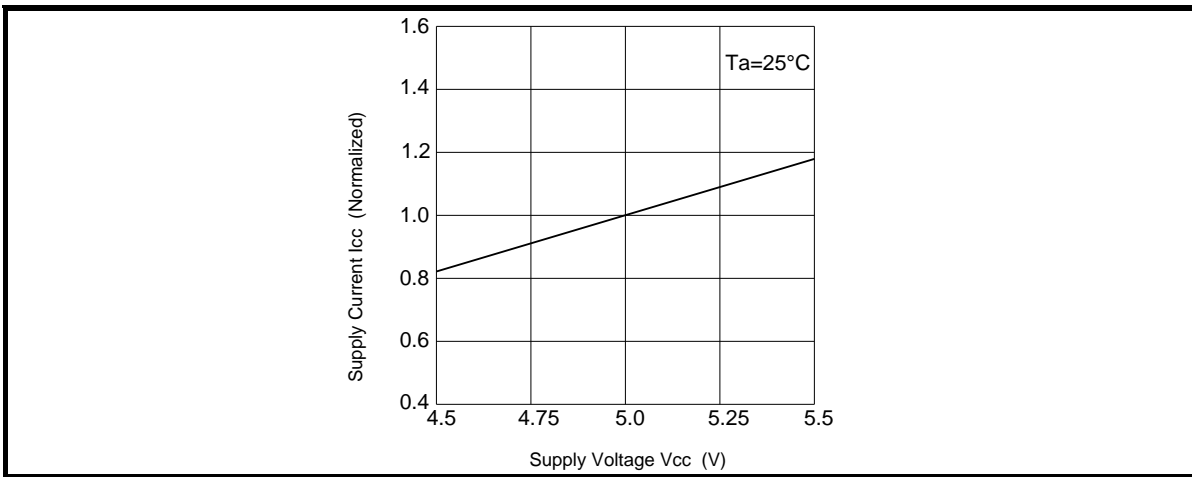


**Standby Current vs. Ambient Temperature**

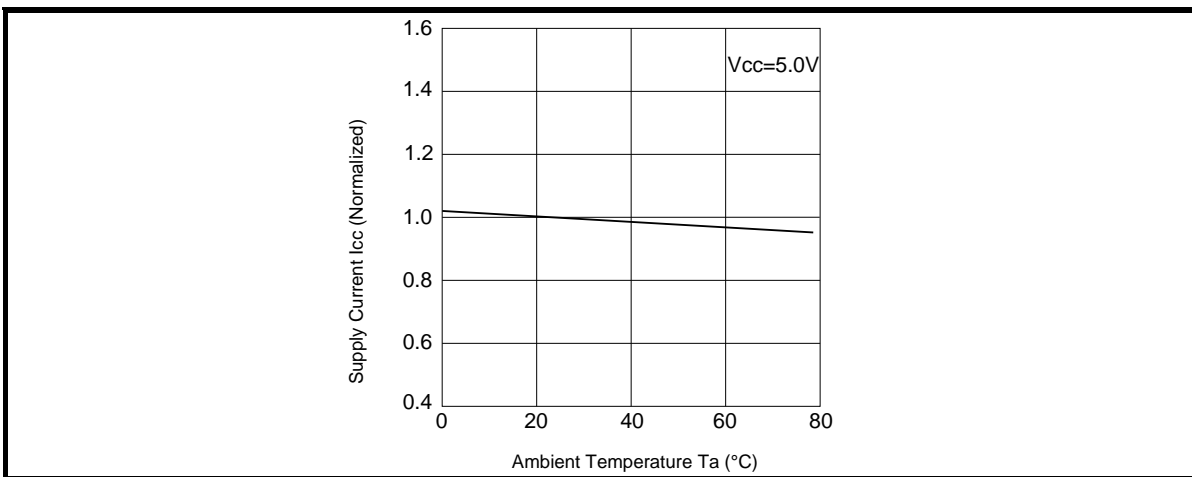
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**Standby Current vs. Supply Voltage**

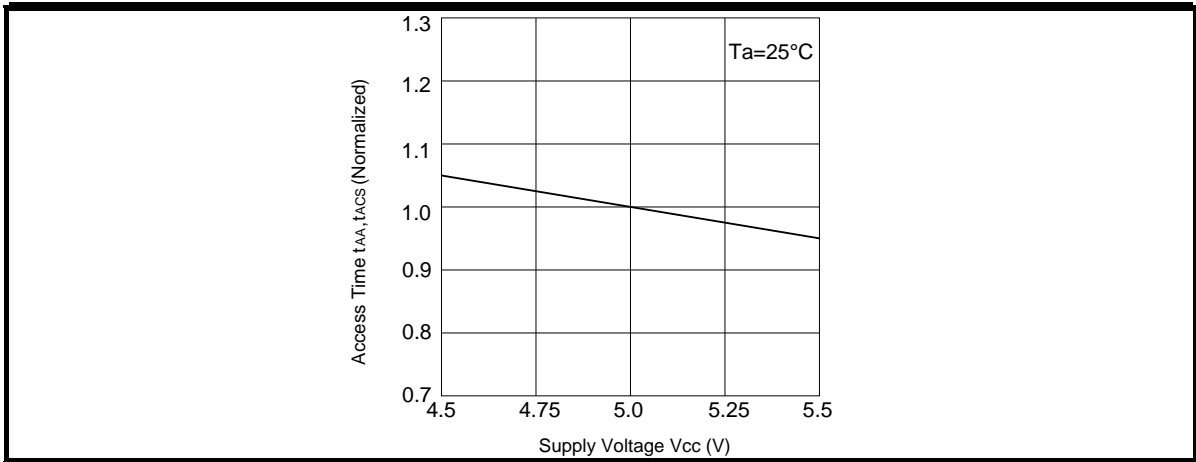


**Supply Current vs. Supply Voltage**

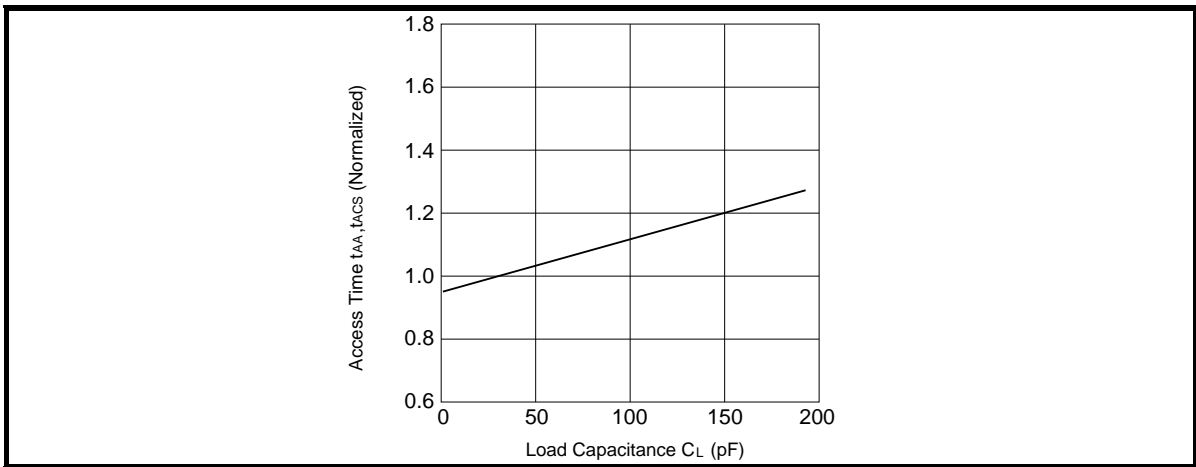


**Supply Current vs. Ambient Temperature**

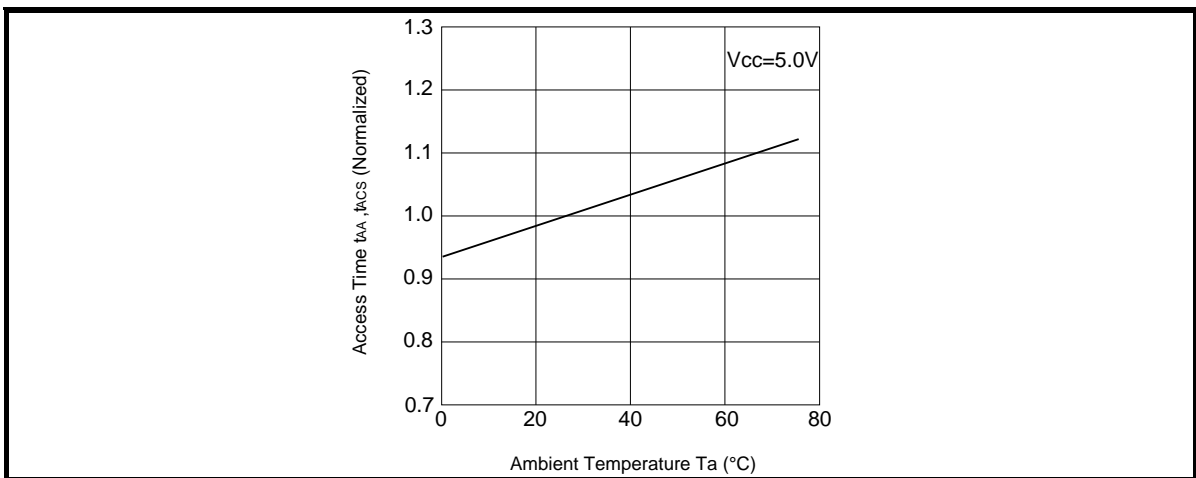
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**Access Time vs. Supply Voltage**

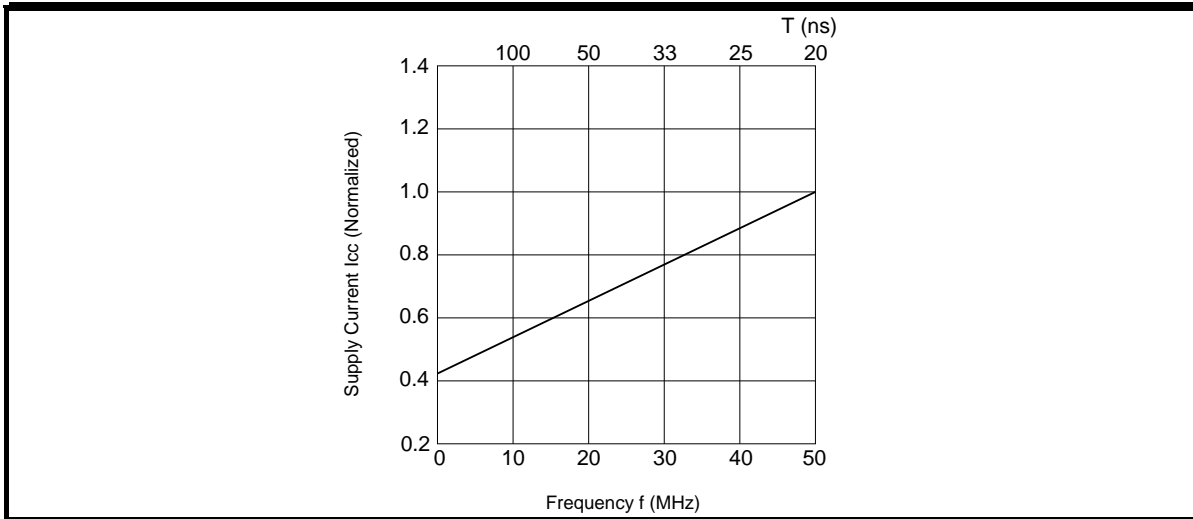


**Access Time vs. Load Capacitance**



**Access Time vs. Ambient Temperature**

## HM621100A Series



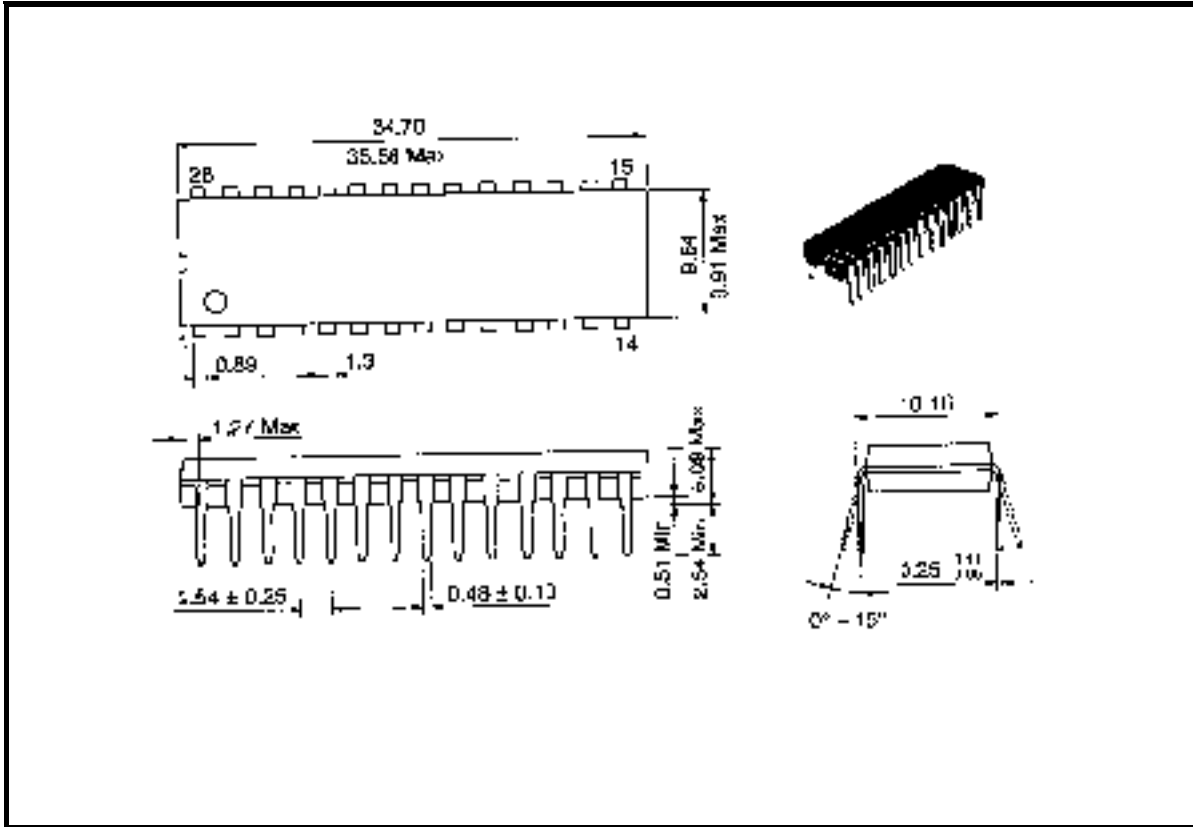
**Supply Current vs. Frequency**

# HM621100A Series

## Package Dimensions

HM621100AP/ALP Series (DP-28C)

Unit: mm



# HM621100A Series

HM621100AJP/ALJP Series (CP-28D)

Unit: mm

