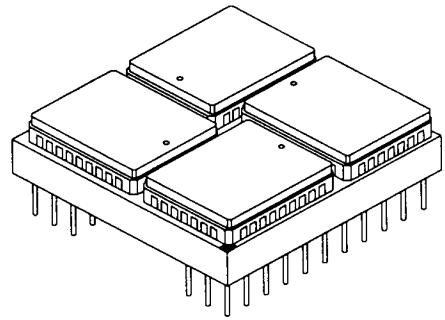
DPS832V
CMOS SRAM VERSAPAC MODULE

DESCRIPTION:

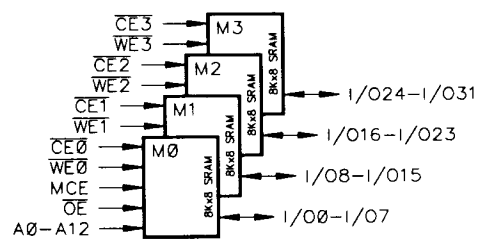
The DPS832V is a 66-pin Pin Grid Array (PGA) consisting of four 8K X 8 SRAM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matching thermal coefficients. The LCCs are mounted in a rotary pattern resulting in the smallest possible module outline.

The pins have been arranged around a central 0.6" gap which can accomodate a heat rail. In this central gap is a cavity containing four 0.1µf decoupling capacitors.

Provisions have been made in the pinout for use of 256K and 1MB SRAMs, providing an upgrade path to 128KX32 and to 256KX32 increasing the module density from four to thirty-two times.



FUNCTIONAL BLOCK DIAGRAM

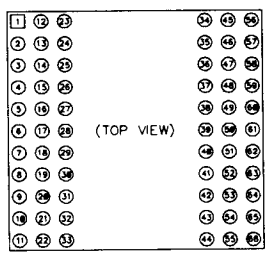


FEATURES:

- Organizations Available:
  32K X 8, 16K X 16 or 8K X 32
- Access Times:
  -25, -35, -45, -55, -70, -85, -100, -120, -150ns
- Low Data Retention: 2.0V min.
- Fully Static Operation - No clock or refresh required
- TTL-compatible
- 66-Pin PGA (Pin Grid Array) Package
- Same Package as other Versapac Versions (EEPROM, EPROM AND MIXED)
- Module Weight is 15 grams
- Module can be built with devices compliant to MIL-STD 883C

PIN NAMES	
A0 - A12	Address Inputs
I/O0 - I/O31	Data In/Out
$\overline{CE0}$ - $\overline{CE3}$	Chip Enables
MCE	Master Chip Enable
$\overline{WE0}$ - $\overline{WE3}$	Write Enables
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM



	1	I/O8	12	$\overline{WE1}$	23	I/O15	34	I/O24	45	VDD	56	I/O31
	2	I/O9	13	$\overline{CE1}$	24	I/O14	35	I/O25	46	$\overline{CE3}$	57	I/O30
	3	I/O10	14	VSS	25	I/O13	36	I/O26	47	$\overline{WE3}$	58	I/O29
† *	4	MCE	15	I/O11	26	I/O12	37	A6	48	I/O27	59	I/O28
*	5	N.C.	16	A10	27	$\overline{OE}$	38	A7	49	A3	60	A0
*	6	N.C.	17	A11	28	N.C.	39	N.C.	50	A4	61	A1
*	7	N.C.	18	A12	29	$\overline{WE0}$	40	A8	51	A5	62	A2
	8	N.C.	19	VDD	30	I/O7	41	A9	52	$\overline{WE2}$	63	I/O23
	9	I/O0	20	$\overline{CE0}$	31	I/O6	42	I/O16	53	$\overline{CE2}$	64	I/O22
	10	I/O1	21	N.C.	32	I/O5	43	I/O17	54	VSS	65	I/O21
	11	I/O2	22	I/O3	33	I/O4	44	I/O18	55	I/O19	66	I/O20

* Designers should connect these pins to A13, 14, A15 and A16 for future upgrades.
† To enable 8KX8 SRAM pin 4 (MCE) must be held in logic "1" condition.

FOR FURTHER INFORMATION
SEE CHAPTER 10
FOR COMPLETE DATA SHEET