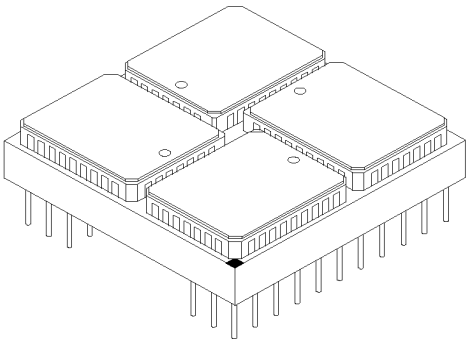
DENSE-PAC
MICROSYSTEMS

1 Megabit CMOS SRAM
DPS3232V-35I-TI

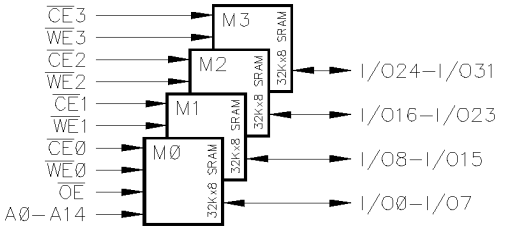


DESCRIPTION:
The DPS3232V-35I-TI is a 66-pin Pin Grid Array (PGA) consisting of four 32K x 8 SRAM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matching thermal coefficients. The LCCs are mounted in a rotary pattern resulting in the smallest possible module outline.

The pins have been arranged around a central 0.6" gap which can accomodate a heat rail. In this central gap is a cavity containing four 0.1µf decoupling capacitors.

This is a custom product for Raytheon TI Systems.

FUNCTIONAL BLOCK DIAGRAM



FEATURES:
- Organizations Available:
  128K X 8, 64K X 16 or 32K X 32
- Access Time: 35ns
- Fully Static Operation
  - No clock or refresh required
- TTL-compatible
- 66-Pin PGA (Pin Grid Array) Package
- Same Package as other Versapac Versions (EEPROM, EPROM AND MIXED)
- Module Weight is 15 grams

PIN NAMES	
A0-A14	Address Inputs
I/O0-I/O31	Data In/Out
$\overline{CE}$0 - $\overline{CE}$3	Chip Enables
$\overline{WE}$0 - $\overline{WE}$3	Write Enables
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM

1	I/O8	12	$\overline{WE}$1	23	I/O15					34	I/O24	45	VDD	56	I/O31
2	I/O9	13	$\overline{CE}$1	24	I/O14					35	I/O25	46	$\overline{CE}$3	57	I/O3Ø
3	I/O1Ø	14	VSS	25	I/O13					36	I/O26	47	$\overline{WE}$3	58	I/O29
4	A13	15	I/O11	26	I/O12					37	A6	48	I/O27	59	I/O28
5	A14	16	A1Ø	27	$\overline{OE}$					38	A7	49	A3	6Ø	AØ
6	N.C.	17	A11	28	N.C.		(TOP VIEW)			39	N.C.	5Ø	A4	61	A1
7	N.C.	18	A12	29	$\overline{WE}$Ø					4Ø	A8	51	A5	62	A2
8	N.C.	19	VDD	3Ø	I/O7					41	A9	52	$\overline{WE}$2	63	I/O23
9	I/OØ	2Ø	$\overline{CE}$Ø	31	I/O6					42	I/O16	53	$\overline{CE}$2	64	I/O22
1Ø	I/O1	21	N.C.	32	I/O5					43	I/O17	54	VSS	65	I/O21
11	I/O2	22	I/O3	33	I/O4					44	I/O18	55	I/O19	66	I/O2Ø

RECOMMENDED OPERATING RANGE [1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage [4]	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		$V_{DD}+0.3$	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V
T_A	Operating Temperature	-40	+25	+85	°C

TRUTH TABLE					
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
D_{OUT} Disable	L	H	H	HIGH-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	H*	D_{IN}	Active

L = LOW H = HIGH X = Don't Care

* If $\overline{OE}$ is LOW during Write, t_{WHZ} must be obserned before data is presented to the device.

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns**
Input and Output Timing Reference Levels	1.5V

** Transition between 0.8V and 2.2V.

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	30pF	except t_{CLZ}, t_{CHZ}, t_{OHZ}, t_{OLZ}, t_{WLZ} and t_{WHZ}
2	5pF	t_{CLZ}, t_{CHZ}, t_{OHZ}, t_{OLZ}, t_{WLZ} and t_{WHZ}

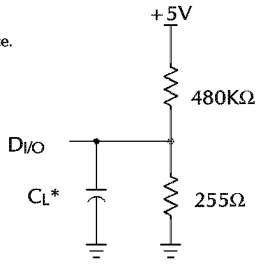
ABSOLUTE MAXIMUM RATINGS [3]			
Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to +7.0	°C
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to +7.0	V

CAPACITANCE [3]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{CE}	Chip Enable	40	pF	V_{IN} = 0V
C_{ADR}	Address Input	50		
C_{WE}	Write Enable	40		
C_{OE}	Output Enable	50		
$C_{I/O}$	Data Input/Output	40		

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH}=-4.0mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL}= +4.0mA	-	0.4	V

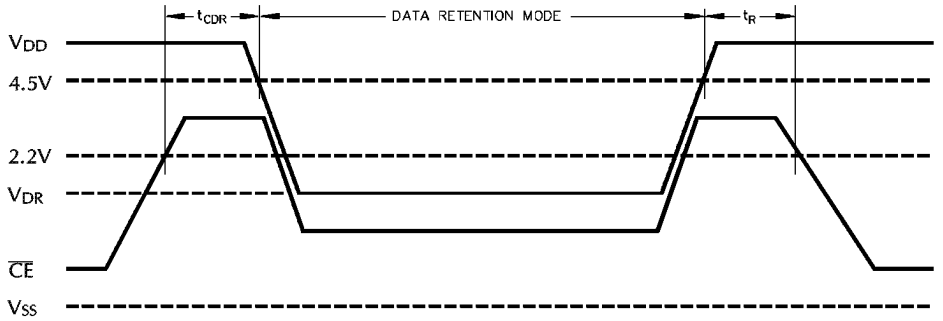
Figure 1. Output Load

*** Including Probe and Jig Capacitance.



DC OPERATING CHARACTERISTICS: Over operating ranges					
Symbol	Characteristics	Test Conditions	MIN.	MAX.	Unit
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} Max.	-40	+40	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0C to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-20	+20	µA
I_{CC1}	Operating Supply Current	Cycle = min., Duty = 100%, I_{OUT} = 0mA		800	mA
I_{SB1}	Full Standby Supply Current (CMOS)	$V_{IN} \geq V^{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2, $\overline{CE} \geq V_{DD}$ -0,2V		100	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}		240	mA
V_{OL}	Output Low Voltage	I_{OUT} = 4.0mA		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -4.0mA	2.4		V

DATA RETENTION WAVEFORM

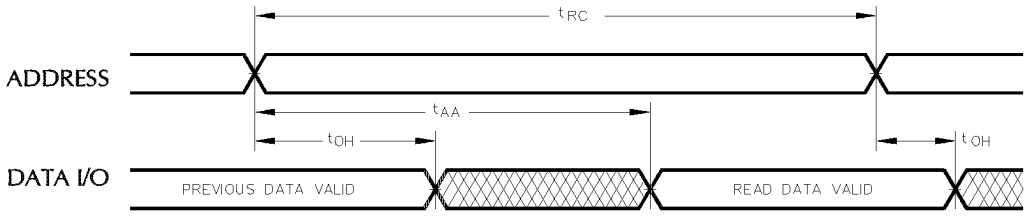


AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges					
No.	Symbol	Parameter	MIN.	MAX.	Unit
1	t_{RC}	Read Cycle Time	35		ns
2	t_{AA}	Address Access Time		35	ns
3	t_{CO}	Chip Enable to Output Valid		35	ns
4	t_{OV}	Output Enable to Output Valid		20	ns
5	t_{OH}	Output Hold from Address Change	3		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 6]	3		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [4, 6]	0		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 6]		25	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 6]		25	ns

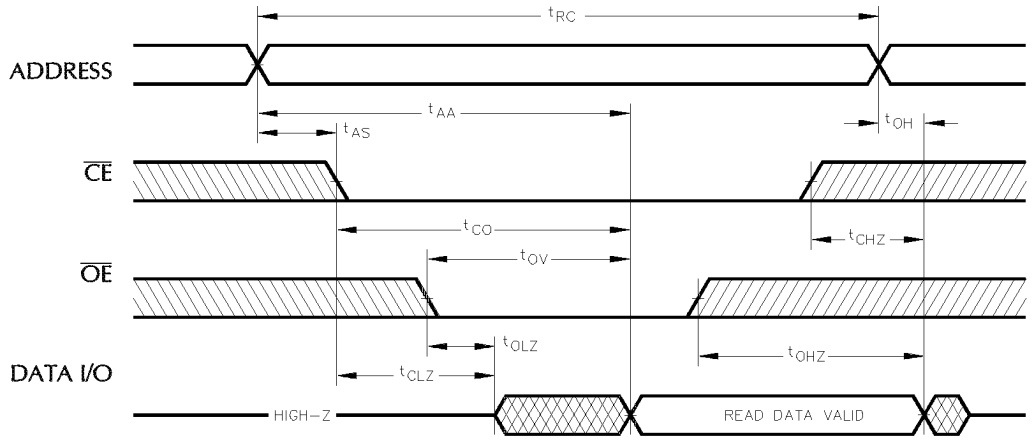
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [6, 7]: Over operating ranges					
No.	Symbol	Parameter	MIN.	MAX.	Unit
10	t_{WC}	Write Cycle Time	35		ns
11	t_{AW}	Address Valid to End of Write	30		ns
12	t_{CW}	Chip Enable to End of Write	30		ns
13	t_{DW}	Data to Write Time Overlap	20		ns
14	t_{DH}	Data Hold Time	3		ns
15	t_{WP}	Write Pulse Width	25		ns
16	t_{AS}	Address Set-Up Time *	0		ns
17	t_{AH}	Address Hold Time	0		ns
18	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 6]	0	30	ns
19	t_{WLZ}	Write Enable to Output in LOW-Z [4,65]	5		ns

* Valid for both Read and Write Cycles.

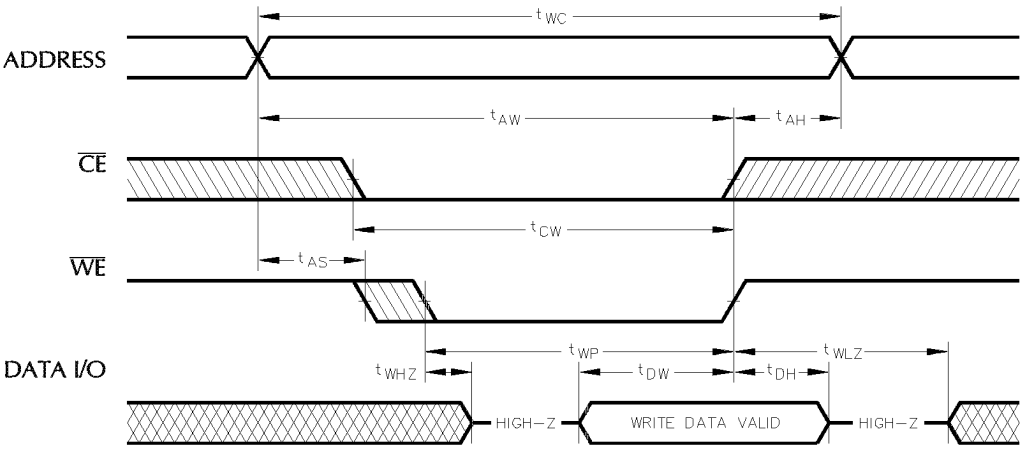
READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.



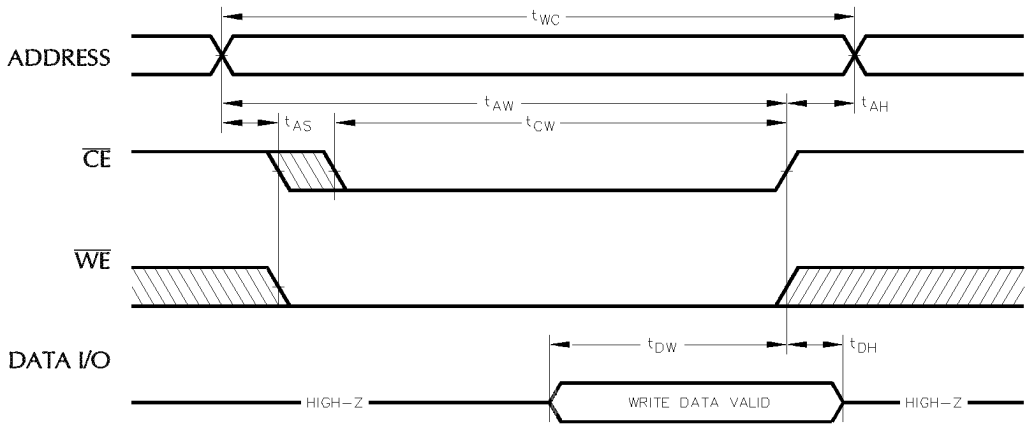
READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.



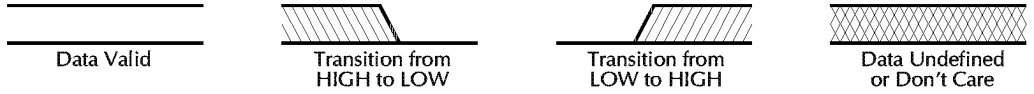
WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is HIGH.



NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

WAVEFORM KEY

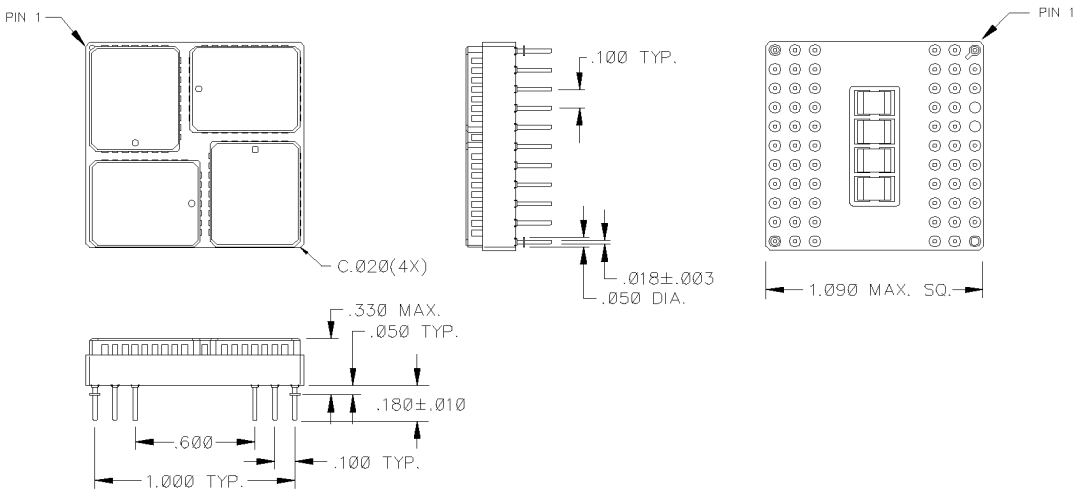


ORDERING INFORMATION

DP	S3232	V	– 35	I	TI
PREFIX	DEVICE TYPE	PACKAGE	SPEED	GRADE	CUSTOM

- CUSTOM FOR RAYTHEON TI SYSTEMS
- INDUSTRIAL –40°C to +85°C
- 35ns
- 66–PIN PGA VERSAPAC
- CMOS SRAM 128KX8, 64KX32 OR 32KX32

MECHANICAL DRAWING



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