

ACCUTEK

MICROCIRCUIT CORPORATION

AK632512W/AK632512Z 512K x 32 SRAM MODULE

DESCRIPTION

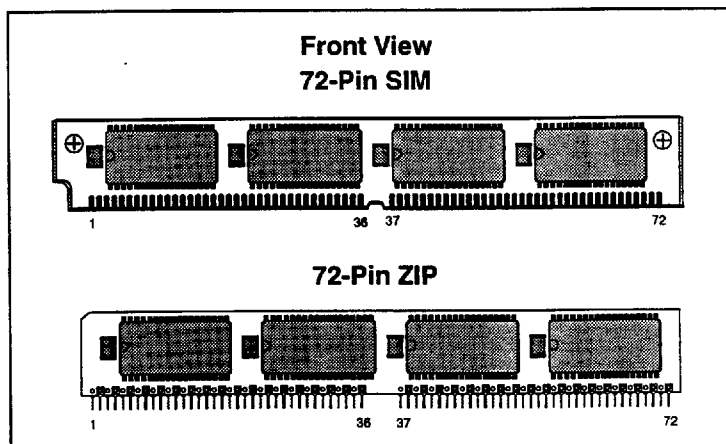
The Accuthek AK632512 SRAM Module consists of fast high performance SRAMs mounted on a low height, 72 pin SIM or ZIP Board. The module utilizes four 36 pin 512K x 8 SRAMs in 400 mil SOJ packages and four decoupling capacitors mounted on the front side of a printed circuit board.

The SRAMs used have common I/O functions and single output enable functions. Also, four separate chip select ($\overline{CE}$) connections are used to independently enable the four bytes. The modules can be supplied in a variety of access time values from 15 nSEC to 35 nSEC in CMOS or BiCMOS technology.

The Accuthek module is designed to have a maximum seated height of 0.620 inch SIM or 0.540 inch ZIP to provide for the lowest height off the board. Each conforms to JEDEC-standard sizes and pin-out configurations. Using four pins for module memory density identification, PD₀, PD₁, PD₂ and PD₃ minimizes interchangeability and design considerations when changing from one module size to the other in customer applications.

FEATURES

- 524,288 x 32 bit organization
- JEDEC Standard 72 pin SIM or ZIP format
- Common I/O, single $\overline{OE}$ and $\overline{WE}$ functions with four separate chip selects ($\overline{CE}$)
- Fast access times from 15 nSEC
- Low height, 0.620 inch SIM or 0.540 inch ZIP maximum
- Power
 - 720mA Max Active (20 nSEC)
 - 760mA Max Active (15 nSEC)
 - 800mA Max Active (12 nSEC)
 - 200mA Max Standby



- Presence Detect, PD₀, PD₁, PD₂ and PD₃ for identifying module density
- Downward compatible with 256K x 32 (AK632256), 128K x 32 (AK632128) and 64K x 32 (AK63264) 64 pin SIM or ZIP designs
- Upward compatible with 1 MEG x 32 (AK6321024)
- TTL-compatible inputs and outputs
- Single +5 Volt (10% power supply)
- Operating free air temperature 0° to 70°C

ELECTRICAL SPECIFICATIONS

Timing diagrams and basic electrical characteristics are those of the standard 512K x 8 SRAMs used to construct these modules. Accuthek's module design allows the flexibility of selecting industry-compatible 512K x 8 SRAMs from several SRAM manufacturers.

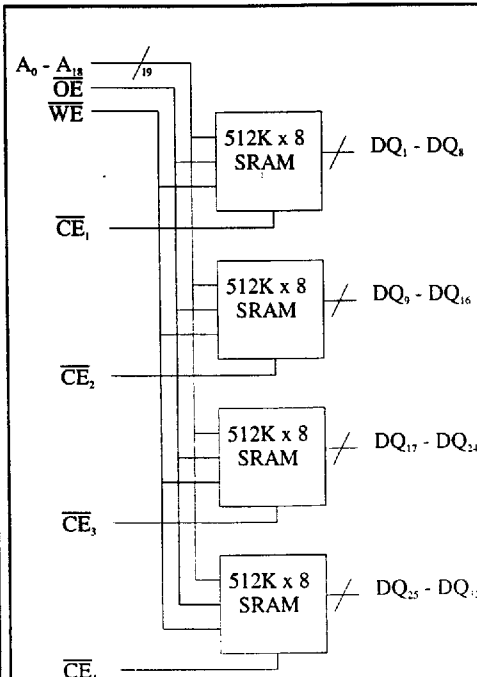
PIN NOMENCLATURE

A ₀ - A ₁₈	Address Inputs
$\overline{CE}_1 - \overline{CE}_4$	Chip Enable
DQ ₁ - DQ ₃₂	Data In/Data Out
$\overline{OE}$	Output Enable
PD ₀ - PD ₃	Presence Detect
V _{cc}	5v Supply
V _{ss}	Ground
$\overline{WE}$	Write Enable

PIN ASSIGNMENT

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	NC	19	A ₁	37	$\overline{CE}_4$	55	A ₅
2	NC	20	A ₆	38	$\overline{CE}_3$	56	A ₁₂
3	PD ₂	21	A ₂	39	A ₁₇	57	V _{cc}
4	PD ₃	22	A ₉	40	A ₁₆	58	A ₁₃
5	V _{ss}	23	DQ ₁₃	41	$\overline{OE}$	59	A ₆
6	PD ₀	24	DQ ₅	42	V _{ss}	60	DQ ₂₁
7	PD ₁	25	DQ ₁₄	43	DQ ₂₅	61	DQ ₂₉
8	DQ ₁	26	DQ ₆	44	DQ ₁₇	62	DQ ₂₂
9	DQ ₉	27	DQ ₁₅	45	DQ ₂₆	63	DQ ₃₀
10	DQ ₂	28	DQ ₇	46	DQ ₁₈	64	DQ ₂₃
11	DQ ₁₀	29	DQ ₁₆	47	DQ ₂₇	65	DQ ₃₁
12	DQ ₃	30	DQ ₈	48	DQ ₁₉	66	DQ ₂₄
13	DQ ₁₁	31	V _{ss}	49	DQ ₂₇	67	DQ ₃₂
14	DQ ₄	32	$\overline{WE}$	50	DQ ₂₀	68	V _{ss}
15	DQ ₁₂	33	A ₁₅	51	A ₃	69	A ₁₈
16	V _{cc}	34	A ₁₄	52	A ₁₀	70	NC
17	A ₀	35	$\overline{CE}_2$	53	A ₄	71	NC
18	A ₇	36	$\overline{CE}_1$	54	A ₁₁	72	NC
PD ₁		OPEN		PD ₃		V _{ss}	
PD ₂		OPEN		PD ₄		OPEN	

FUNCTIONAL DIAGRAM



MODULE OPTIONS

Leadless SIM: AK632512W

Leaded SIP: AK632512G

Leaded ZIP: AK632512Z

