MOTOROLA

Advance Information

32K x 8 Bit Fast Static Random Access Memory

ELECTRICALLY TESTED PER:
MPG6206C

6206C

Commercial Plus and Mil/Aero Applications

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 6206C - XX/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: DIL: X
FP: Y

XX = Speed in ns
(15, 20, 25, 25, 45, 55, 70, 100)

The 6206C is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using Motorola's third-generation high-performance silicon-gate CMOS (HCMOS IV) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after E goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as E remains high. This feature provides significant system-level power savings. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 8 ns (6206C-15).

The 6206C is packaged in a 600 mil, 28 pin ceramic dual-in-line package, and a 740 x 520 mil, 28 pin Flat-Pack package.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Time — 15, 20, 25, 35, 45, 55, 70, 100 ns
- Low Power Operation: 135-165 mA Maximum ac
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) feature for Increased System Flexibility and to eliminate bus connection problems
- Fully TTL Compatible — Three State Outputs

BURN-IN CONDITIONS:

V_{CC} = 5.0 V(min)/ 6.0 V(max), R_1 = 39.2 kΩ ± 20%, C_1 = 0.1 µF ± 20%,
V_H = 3.0 V(min)/5.0 V(max), V_L = – 0.5 V(min)/0.0 V(max),

CP1:	100 KHz	CP6:	3.125 KHz	CP11:	97.66 Hz	CP16:	3.052 Hz
CP2:	50 KHz	CP7:	1.563 KHz	CP12:	48.83 Hz	CP17:	1.526 Hz
CP3:	25 KHz	CP8:	0.781 KHz	CP13:	24.41 Hz		
CP4:	12.5 KHz	CP9:	0.391 KHz	CP14:	12.21 Hz		
CP5:	6.25 KHz	CP10:	0.195 KHz	CP15:	6.104 Hz		

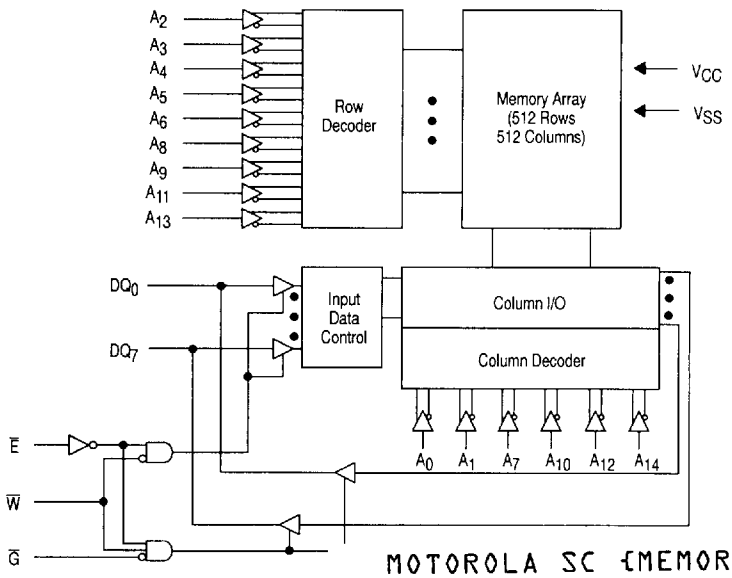
PIN NAME and FUNCTIONS

$A_0 - A_{14}$	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$DQ_0 - DQ_7$	Data Input/Output
V_{CC}	+ 5.0 V Power Supply
V_{SS}	Ground
N.C.	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN ASSIGNMENTS			
Function	**DIL Case 719-01**	**FP Case 876-01**	**Burn-In (Condition-D)**
A_{14}	1	1	CP17
A_{12}	2	2	CP4
A_7	3	3	CP5
A_6	4	4	CP6
A_5	5	5	CP7
A_4	6	6	CP8
A_3	7	7	CP9
A_2	8	8	CP10
A_1	9	9	CP11
A_0	10	10	CP12
DQ_0	11	11	CP18 to R_1
DQ_1	12	12	CP18 to R_1
DQ_2	13	13	CP18 to R_1
V_{SS}	14	14	GND
DQ_3	15	15	CP18 to R1
DQ_4	16	16	CP18 to R1
DQ_5	17	17	CP18 to R_1
DQ_6	18	18	CP18 to R_1
DQ_7	19	19	CP18 to R_1
$\overline{E}$	20	20	CP2
A_{10}	21	21	CP13
$\overline{G}$	22	22	CP1
A_{11}	23	23	CP14
A_9	24	24	CP15
A_8	25	25	CP16
A_{13}	26	26	CP3
$\overline{W}$	27	27	CP1
V_{CC}	28	28	V_{CC}, C_1 to GND

BLOCK DIAGRAM



TRUTH TABLE					
$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{OUT}
L	X	L	Write	I_{CC}	D_{IN}

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS: (See Note)			
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to +7.0	V
Voltage Relative to V_S for Any Pin Except V_{CC}	V_{IN}, V_{OUT}	– 0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{OUT}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	–55 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Temperature Range	T_A	–55 to +125	°C
Maximum Junction Temperature	T_J	+150	°C
Thermal Resistance, Junction to Case	θ_{JD}	per MIL-M-38510 appendix C	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could effect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = –55°C to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameters	Symbol	Min	Typical	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	–0.5*	—	0.8	V

* V_{IL} (max) = + 0.6 Vdc for output enable (B) and Chip Enable ($\overline{E}$)

** V_{IH} (max) = V_{CC} + 0.3 Vdc; V_{IH} (max) = V_{CC} + 2.0 Vdc (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameters		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 10	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, or $\overline{G}$ = V_{IH}, V_{OUT} = 0 to 5.5 V)		$I_{lkg(O)}$	—	± 10	µA
Power Supply Current ($\overline{E}$ = V_{IL}, V_{IN} = V_{IH}, or V_{IL}, I_{OUT} = 0), F = 1/t_{AVAV}	15 ns	I_{CCA}	—	165	mA
	20 ns	I_{CCA}	—	150	
	25 ns	I_{CCA}	—	140	
	35 ns	I_{CCA}	—	135	
	45 ns	I_{CCA}	—	125	
	55 ns	I_{CCA}	—	120	
	70 ns	I_{CCA}	—	110	
	100 ns	I_{CCA}	—	105	
Standby Current ($\overline{E}$ = V_{IH}) (TTL Levels)	15 ns	I_{SB1}	—	50	mA
	20 ns	I_{SB1}	—	45	
	25 ns	I_{SB1}	—	40	
	35 ns	I_{SB1}	—	40	
	45 ns	I_{SB1}	—	35	
	55 ns	I_{SB1}	—	35	
	70 ns	I_{SB1}	—	30	
	100 ns	I_{SB1}	—	30	
Standby Current ($\overline{E}$ ≥ V_{CC} – 2.0 V) (CMOS Levels)		I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristics		Symbol	Max	Unit
Input Capacitance (Control Pins)	$\overline{E}$, $\overline{G}$, $\overline{W}$	C_{in}	8	pF
Output Capacitance		C_{Out}	8	pF

AC TEST LOADS OR EQUIVALENT

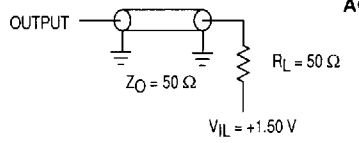


Figure 1A.

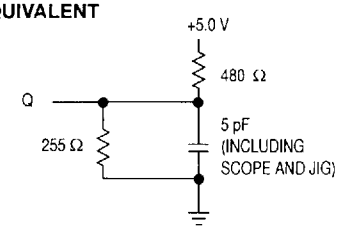


Figure 1B.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 55°C to + 125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level	1.5 V
Input Pulse levels	0 to 3.0 V
Input Rise/Falls Time	≥ 5.0 ns
Output Timing Measurement Reference Level	1.5 V
Output Load	See Figure 1

READ CYCLE (See Note 1)

Parameters	Symbol	Alternate Symbol	6206C-15		6206C-20		6206C-25		6206C-35		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	15	—	20	—	25	—	35	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	15	—	20	—	25	—	35	ns	—
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	—	15	—	20	—	25	—	35	ns	3
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	8	—	10	—	12	—	15	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	ns	4, 5, 6
Chip Enable to Output Low-Z	t_{ELQX}	t_{LZ}	4	—	4	—	4	—	4	—	ns	4, 5, 6
Output Enable to Output Low-Z	t_{GLQX}	t_{LZ}	0	—	0	—	0	—	0	—	ns	4, 5, 6
Chip Enable to Output High-Z	t_{EHQZ}	t_{HZ}	0	8	0	9	0	10	0	11	ns	4, 5, 6
Output Enable to Output High-Z	t_{GHQZ}	t_{HZ}	0	7	0	8	0	10	0	11	ns	4, 5, 6

READ CYCLE (See Note 1)

Parameters	Symbol	Alternate Symbol	6206C-45		6206C-55		6206C-70		6206C-100		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	45	—	55	—	70	—	100	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	45	—	55	—	70	—	100	ns	—
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	—	45	—	55	—	70	—	100	ns	3
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	18	—	21	—	26	—	35	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	ns	4, 5, 6
Chip Enable to Output Low-Z	t_{ELQX}	t_{LZ}	4	—	4	—	4	—	4	—	ns	4, 5, 6
Output Enable to Output Low-Z	t_{GLQX}	t_{LZ}	0	—	0	—	0	—	0	—	ns	4, 5, 6
Chip Enable to Output High-Z	t_{EHQZ}	t_{HZ}	0	12	0	13	0	14	0	15	ns	4, 5, 6
Output Enable to Output High-Z	t_{GHQZ}	t_{HZ}	0	12	0	13	0	14	0	15	ns	4, 5, 6

NOTES:

1. $\overline{W}$ is high for read cycles.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ}(max) is less than t_{ELQX}(min), and t_{GHQZ}(max) is less than t_{GLQX}(min), both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 55°C to + 125°C, Unless Otherwise Noted)

WRITE CYCLE 1 & 2 (See Note 1 and 2, $\overline{W}$ controlled)

Parameters	Symbol	Alternate Symbol	6206C-15		6206C-20		6206C-25		6206C-35		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	25	—	35	—	ns	3
Address Setup to Write Low Address Setup to Enable Low	t_{AVWL} t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	—
Address Valid to Write High Address Valid to Enable High	t_{AVWH} t_{AVEH}	t_{AW}	12	—	15	—	20	—	25	—	ns	—
Data Valid to Write High Data Valid to Enable High	t_{DVWH} t_{DVEH}	t_{DW}	7	—	8	—	10	—	12	—	ns	—
Data Hold from Write High Data Hold from Enable High	t_{WHDX} t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	—
Write Recovery Time Enable Recovery Time	t_{WHAX} t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	—
Chip Enable to End of Write Enable Low to Enable High	t_{ELWH} t_{ELEH}	t_{CW}	10	—	12	—	15	—	10	—	ns	8, 9
Write Pulse Width	t_{WLWH}	t_{WP}	12	—	15	—	20	—	25	—	ns	4
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	7	0	8	0	10	0	11	ns	6, 7
Write High to Output Low-Z	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	ns	6, 7

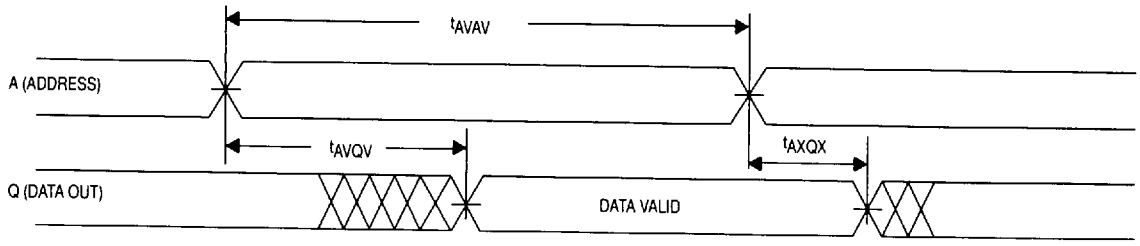
WRITE CYCLE 1 & 2 (See Note 1 and 2, $\overline{W}$ controlled)

Parameters	Symbol	Alternate Symbol	6206C-45		6206C-55		6206C-70		6206C-100		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	45	—	55	—	70	—	100	—	ns	3
Address Setup to Write Low Address Setup to Enable Low	t_{AVWL} t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	—
Address Valid to Write High Address Valid to Enable High	t_{AVWH} t_{AVEH}	t_{AW}	30	—	35	—	40	—	45	—	ns	—
Data Valid to Write High Data Valid to Enable High	t_{DVWH} t_{DVEH}	t_{DW}	14	—	16	—	18	—	20	—	ns	—
Data Hold from Write High Data Hold from Enable High	t_{WHDX} t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	—
Write Recovery Time Enable Recovery Time	t_{WHAX} t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	—
Chip Enable to End of Write Enable Low to Enable High	t_{ELWH} t_{ELEH}	t_{CW}	12	—	15	—	18	—	20	—	ns	8, 9
Write Pulse Width	t_{WLWH}	t_{WP}	30	—	35	—	40	—	45	—	ns	4
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	12	0	13	0	16	0	24	ns	6, 7
Write High to Output Low-Z	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	ns	6, 7

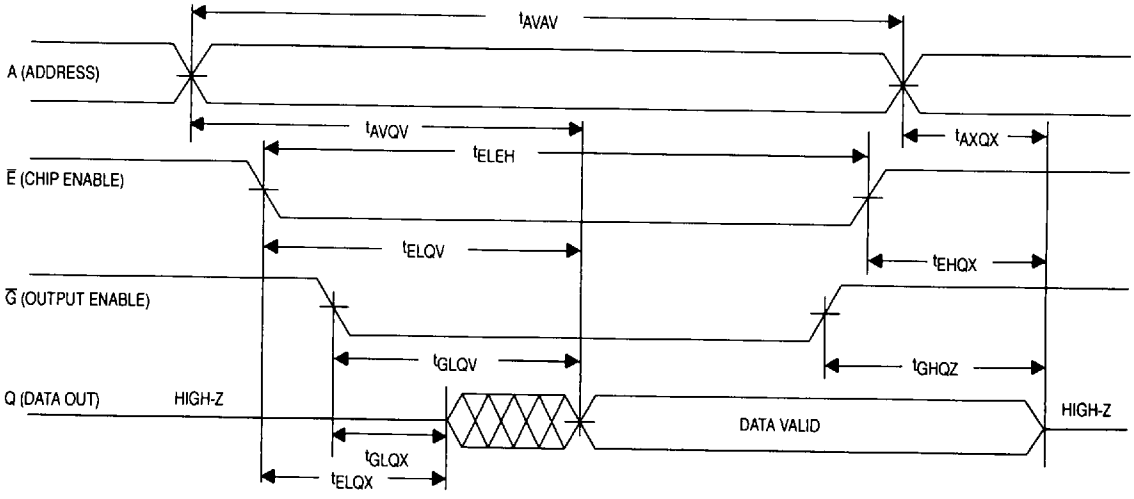
NOTES:

1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ}(max) is less than t_{WHQX}(min), both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
9. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

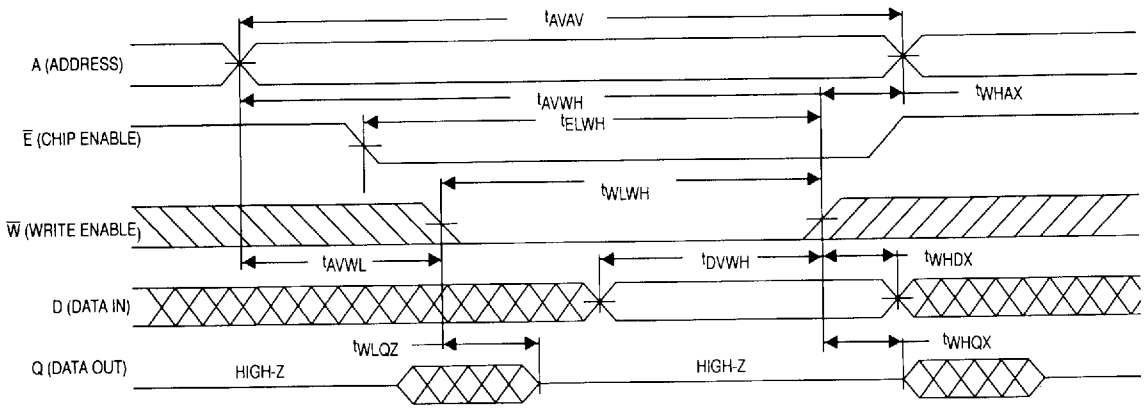
READ CYCLE 1 ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL})



READ CYCLE 2



WRITE CYCLE 1 ($\overline{W}$ Controlled)



WRITE CYCLE 2 ($\overline{E}$ Controlled)