REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																									
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REV STATUS OF SHEETS	REV																								
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14										

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE: 91-12-30

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, DIGITAL, 2 K X 8 REGISTERED UVEPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89815

SHEET 1 OF 14

DESC FORM 193
SEP 87

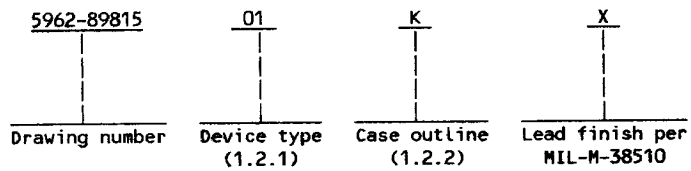
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1803

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Setup time
01		2K x 8 registered UV EPROM	35 ns
02		2K x 8 registered UV EPROM	25 ns
03		2K x 8 registered UV EPROM	18 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24-lead, .640" x .420" x .090"), flat package 2/
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package 2/
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package 2/

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs in high Z state	-0.5 V dc to +7.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
DC program voltage	13.0 V dc
Maximum power dissipation 3/	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C
Endurance	10 cycles/byte, minimum
Data retention	10 years, minimum

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.0 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.
2/ Lid shall be transparent to permit ultraviolet light erasure.
3/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed or erased devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2) group A, C, or D (see 4.3), the devices shall be programmed by the manufacturer prior to test with a checkerboard pattern or equivalent (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA $V_{IN} = V_{IH}, V_{IL}$	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 16.0 mA $V_{IN} = V_{IH}, V_{IL}$	1, 2, 3	All		0.4	V
Input high voltage 1/	V_{IH}		1, 2, 3	All	2.0		V
Input low voltage 1/	V_{IL}		1, 2, 3	All		0.8	V
2Input leakage current	I_{IX}	$V_{IN} = V_{CC}$ to GND	1, 2, 3	All	-10	+10	µA
Output leakage current 3/	I_{OZ}	$V_{OUT} = V_{CC}$ to GND	1, 2, 3	All	-40	+40	µA
Output short circuit current 4/ 5/	I_{OS}	V_{CC} = 4.5 V, and 5.5 V V_{OUT} = 0.0 V	1, 2, 3	All	-20	-90	mA
Power supply current	I_{CC}	$\overline{E}/\overline{ES} = V_{IL}$, $\overline{INIT} = V_{IH}$, addresses cycling between 0 V and 3 V; $f = \frac{1}{2\ t_{PWC}}$ V_{CC} = 5.5 V	1, 2, 3	All		120	mA
Input capacitance 5/	C_{IN}	V_{CC} = 5.0 V, V_{IN} = 0 V T_A = +25°C, f = 1 MHz (see 4.3.1c)	4	All		10	pF
Output capacitance 5/	C_{OUT}	V_{CC} = 5.0 V, V_{OUT} = 0 V T_A = +25°C, f = 1 MHz (see 4.3.1c)	4	All		10	pF
Functional tests		See 4.3.1e	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Address setup to clock high	t_{SA}	See figures 3 and 4 6/	9, 10, 11	01	35		ns
				02	25		
				03	18		
Address hold from clock high	t_{HA}		9, 10, 11	All	0		ns
Clock high to valid output	t_{CO}		9, 10, 11	01		15	ns
				02, 03		12	
Clock pulse width 5/	t_{PWC}		9, 10, 11	01	20		ns
				02	15		
				03	12		
$\overline{E}_S$ setup to clock high 5/	t_{SES}		9, 10, 11	01	15		ns
				02	12		
				03	10		
$\overline{E}_S$ hold from clock high 5/	t_{HES}		9, 10, 11	All	5		ns
Delay from $\overline{INIT}$ to valid output	t_{DI}		9, 10, 11	All		20	ns
$\overline{INIT}$ recovery to clock high	t_{RI}		9, 10, 11	01	20		ns
				02, 03	15		
$\overline{INIT}$ pulse width	t_{PWI}		9, 10, 11	01	20		ns
				02, 03	15		
Valid output from clock high 5/ 7/	t_{COS}		9, 10, 11	01		20	ns
				02, 03		15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Inactive output from clock high 5/ 7/ 8/	t_{HZC}	See figures 3 and 4 6/	9, 10, 11	01		20	ns
				02, 03		15	
Valid output from $\overline{E}$ low 9/	t_{DOE}		9, 10, 11	01		20	ns
				02, 03		15	
Inactive output from $\overline{E}$ high 5/ 8/ 9/	t_{HZE}		9, 10, 11	01		20	ns
				02, 03		15	

1/ These are absolute voltages with respect to device ground pin and include all overshoots due to system or tester noise.

2/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 3.

3/ For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.

4/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

5/ This parameter tested initially and after any design or process changes which could affect this parameter, and therefore shall be guaranteed to the limits specified in table I.

6/ See figure 3, circuit A, for all switching characteristics except t_{HZ}.

7/ Applies only when the synchronous ($\overline{E}_S$) function is used.

8/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input with the output load on figure 3, circuit B.

9/ Applies only when the asynchronous ($\overline{E}$) function is used.

Device types	All	
Case outlines	K, L	3
Terminal number	Terminal symbol	
1	A_7	NC
2	A_6	A_7
3	A_5	A_6
4	A_4	A_5
5	A_3	A_4
6	A_2	A_3
7	A_1	A_2
8	A_0	A_1
9	O_0	A_0
10	O_1	NC
11	O_2	O_0
12	GND	O_1
13	O_3	O_2
14	O_4	GND
15	O_5	NC
16	O_6	O_3
17	O_7	O_4
18	CP	O_5
19	$\overline{E}/\overline{E}_S$	O_6
20	$\overline{INIT}$	O_7
21	A_{10}	NC
22	A_9	CP
23	A_8	$\overline{E}/\overline{E}_S$
24	V_{CC}	$\overline{INIT}$
25	---	A_{10}
26	---	A_9
27	---	A_8
28	---	V_{CC}

FIGURE 1. Terminal connections.

Mode		Pin function					Outputs
	Read or output disable	A_3	CP	$\overline{E}/\overline{E}_S$	$\overline{INIT}$	A_0	Outputs
	Program or verification	A_3	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	A_0	Outputs
Read 2/ 3/		X	X	V_{IL}	V_{IH}	X	Data out
Output disable 5/		X	X	V_{IH}	V_{IH}	X	High Z
Program 1/ 4/ 6/		X	V_{ILP}	V_{IHP}	V_{PP}	X	Data in
Program verify 1/ 4/ 6/		X	V_{IHP}	V_{ILP}	V_{PP}	X	Data out
Program inhibit 1/ 4/ 6/		X	V_{IHP}	V_{IHP}	V_{PP}	X	High Z
Intelligent program 1/ 4/ 6/		X	V_{ILP}	V_{IHP}	V_{PP}	X	Data in
Program synch enable 4/ 6/		V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	V_{PP}	High Z
Program initial byte 4/ 6/		V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	V_{PP}	Data in

1/ X = Don't care but not to exceed V_{PP}.

2/ During read operation, the output latches are loaded on a "0" to "1" transition of CP.

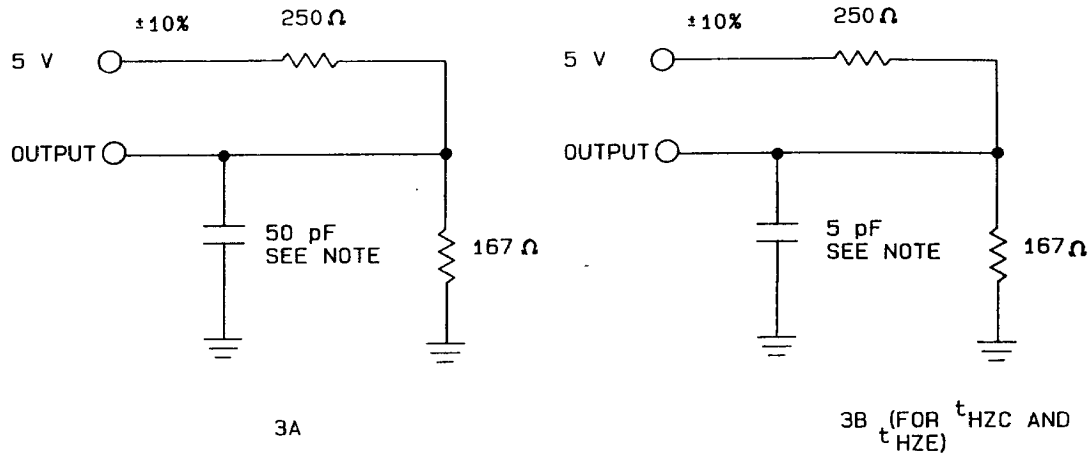
3/ In the synchronous mode, pin $\overline{E}_S$ must be low prior to the "0" to "1" transition on CP that loads the register.

4/ During programming and verification, all unspecified pins to be at V_{ILP}.

5/ In the synchronous mode, pin $\overline{E}_S$ must be high prior to the "0" to "1" transition on CP that loads the register.

6/ For V_{ILP}, V_{IHP} and V_{PP} (see 4.5).

FIGURE 2. Truth table.

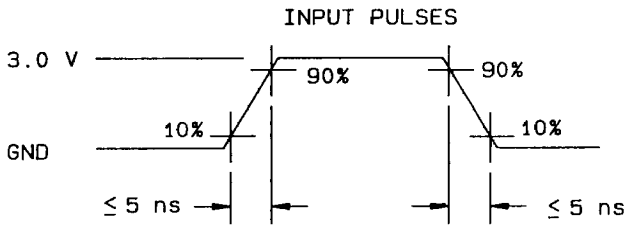


3A

3B (t_{HZE}) (FOR t_{HZC} AND t_{HZE})

OUTPUT LOAD

NOTE: INCLUDING SCOPE AND JIG. (MINIMUM VALUES)



Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit and test conditions.

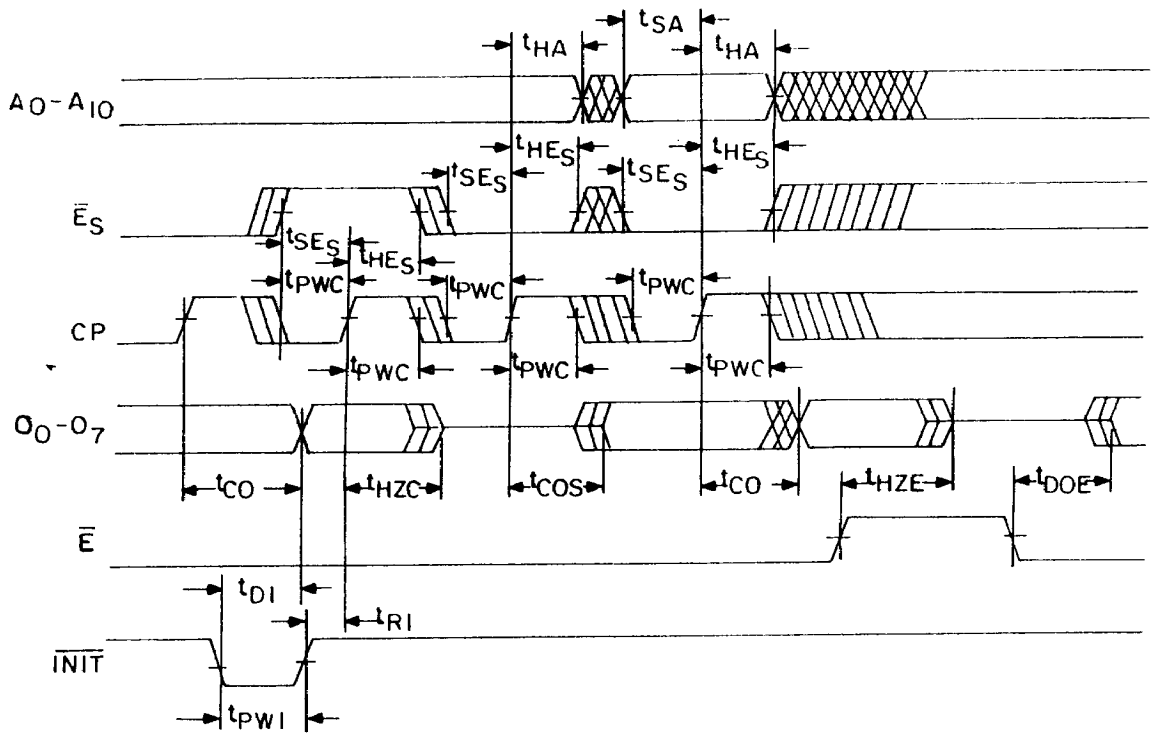


FIGURE 4. Switching waveforms.

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3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EPROM's. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPROM's. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.10.2 Programmability of EPROM's. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.10.3 Verification of erasure or programmed EPROM's. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

d. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps: (Steps 1 through 5 may be performed at the wafer level. The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.)

Margin test method.

(1) Program a minimum of 50 percent of the total number of bits (example, checkerboard) (see 3.10.2).

(2) Perform margin test and find maximum V_m. Store value in EPROM. Fail if V_m < +5.0 V.

(3) Bake, unbiased, for 72 hours at +140°C, for 48 hours at +150°C, for 8 hours at +200°C, or for 2 hours at +300°C for unassembled devices only.

(4) Perform margin test and find maximum V_m. Fail if V_m < +5.0 V. Calculate delta V_m from value stored in (2). Fail if delta > 0.8 V.

(5) Erase (see 3.10.1).

(6) Program a minimum of 50 percent of the total number of bits (example, checkerboard) (see 3.10.2).

(7) Perform margin test using V_m = +5.5 V and a margin test using V_m = +2.0 V at +25°C using loose timing (i.e., t_{AA} = 1 μs).

(8) Perform dynamic burn-in (see 4.2a).

(9) Perform margin test using V_m = +5.5 V and a margin test using V_m = +2.0 V at +25°C using loose timing (i.e., t_{AA} = 1 μs).

(10) Perform electrical tests (see 4.2b).

(11) Repeat steps 9 and 10 at +125°C and -55°C.

(12) Erase (see 3.10.1). Devices may be submitted for groups A, C, and D testing prior to erasure provided the devices have been 100-percent seal tested in accordance with method 5004 of MIL-STD-883.

(13) Verify erasure (see 3.10.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial characterization and after any process or design changes which may affect input or output capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

e. Subgroups 7 and 8 shall include verification of the truth table and the EPROM pattern specified in 4.3.1d.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) The devices selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

(2) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(3) T_A = +125°C, minimum.

(4) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. A reprogrammability test shall be added to group C inspection prior to performing the steady-state life test (see 4.3.2b). The devices to be submitted to the steady-state life testing shall be subjected to the following tests and examinations;

Each device in the sample shall be subjected to a minimum of 50 program and erase cycles.

(1) All devices selected for testing shall be programmed with a checkerboard pattern or equivalent.

(2) Verify pattern (see 3.10.3).

(3) Erase (see 3.10.1).

(4) Verify pattern erasure (see 3.10.3).

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7*,8A, 8B,9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7, 8A,8B,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8A,8B

1/ * Indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ ** See 4.3.1c.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using an ultraviolet lamp with a 12,000 uW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12,000 uW/cm^2). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.