

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Product Preview 32K x 32 Bit Fast SRAM Module

The 46206 is a 1,048,576 bit static random access memory organized as 32,768 words of 32 bits. The module is constructed using four 6206 (32K x 8) static RAM's in leadless carriers mounted in either a multilayer sidebrazed DIL or a double sided multilayer Polyimide substrate.

The 6206 is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using Motorola's third-generation high-performance silicon-gate CMOS (HCMOS IV) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

Chip enable (\bar{E}) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after \bar{E} goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as \bar{E} remains high. This feature provides significant system-level power savings. Another control feature, output enable (\bar{G}) allows access to the memory contents as fast as 20 ns (6206-35).

The 46206 is equipped with output enables (\bar{G}_0 - \bar{G}_3) and four separate byte enables (\bar{CS}_0 - \bar{CS}_3) inputs, allowing for greater system flexibility. The (\bar{G}) input, when high will force the output to a high impedance.

- High Density 1.0 Megabit SRAM (32K x 32) Module
- High Speed CMOS SRAMs
- Fast Access Time — Military 35 ns (max)
- Available in: 64 pin, 600 mil x 3.2 inch DIL Sidebrazed
64 pin PGA — 1.0 inch x 1.6 inches
(2.9 square inches of board space)
- Individual Byte Wide Select
- Fully TTL Compatible
- Single 5.0 V ($\pm 10\%$) Power Supply
- Fully Static — No Clock or Timing Strokes Necessary
- Two Module Controls: \bar{CS} for Automatic Power Down
 \bar{G} for Fast Access to Data
- Three State Outputs

PIN NAMES and FUNCTION

A ₀ -A ₁₄	Address Inputs
\bar{W}_0 - \bar{W}_3	Write Enable
\bar{CS}_0 - \bar{CS}_3	Byte Enable
\bar{G}_0 - \bar{G}_3	Output Enable
I/O ₀ -I/O ₃	Data I/O
V _{CC}	+ 5.0 V Power Supply
GND	Ground

All power supply and ground pins must be connected for proper operation of the device.

Military 46206

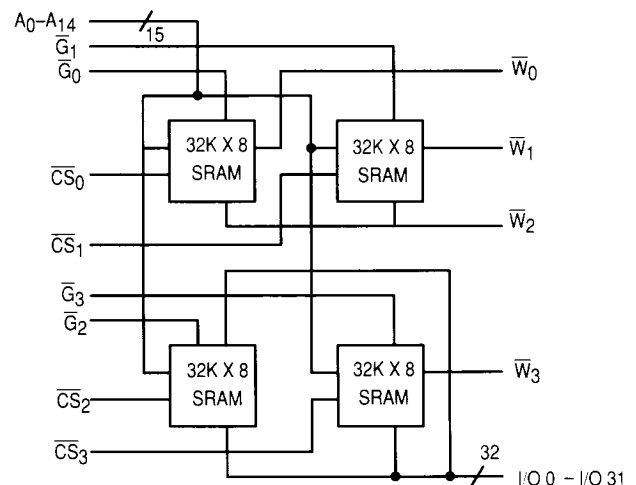


AVAILABLE AS

- 1) JAN: N/A
 - 2) SMD: N/A
 - 3) 883C: Planned
- X = CASE OUTLINE AS FOLLOWS:
PACKAGE: DIL: 46206-35/BXAJC
PGA: 46206-35/BZAJC

XX = Speed in ns (35, 45, 55, 70)

BLOCK DIAGRAM



TRUTH TABLE

\bar{CS}	\bar{G}	\bar{W}	Mode	Supply	I/O Pin
H	X	X	Not Selected	I _{SB}	High-Z
L	H	H	Output Disable	I _{CC}	High-Z
L	L	H	Read	I _{CC}	DOUT
L	X	L	Write	I _{CC}	DIN

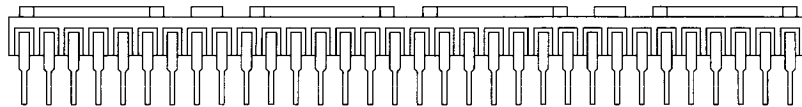
X = Don't Care

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PIN ASSIGNMENTS

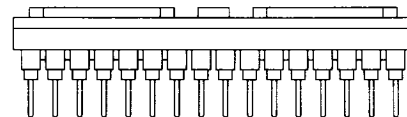
DIL SIDEBRAZE



DIL

V _{CC}	1	64	GND
\bar{G}_0	2	63	\bar{G}_1
A0	3	62	I/O 31
I/O 0	4	61	I/O 30
I/O 1	5	60	I/O 29
I/O 2	6	59	I/O 28
I/O 3	7	58	\bar{W}_1
\bar{CS}_0	8	57	\bar{W}_2
A1	9	56	\bar{CS}_1
I/O 4	10	55	I/O 27
I/O 5	11	54	I/O 26
I/O 6	12	53	I/O 25
I/O 7	13	52	I/O 24
A2	14	51	GND
A3	15	50	A14
\bar{W}_0	16	49	\bar{W}_3
A4	17	48	A13
A5	18	47	A12
I/O 8	19	46	I/O 23
I/O 9	20	45	I/O 22
I/O 10	21	44	I/O 21
I/O 11	22	43	I/O 20
A6	23	42	A11
A7	24	41	A10
\bar{CS}_2	25	40	\bar{CS}_3
I/O 12	26	39	I/O 19
I/O 13	27	38	I/O 18
I/O 14	28	37	I/O 17
I/O 15	29	36	I/O 16
A8	30	35	A9
\bar{G}_2	31	34	\bar{G}_3
GND	32	33	V _{CC}


PGA



PGA

\bar{W}_3	1	17	I/O 3	I/O 2	33	64	I/O 1
I/O 4	2	18	I/O 5	A7	34	63	I/O 0
I/O 6	3	19	I/O 7	A9	35	62	A8
\bar{CS}_0	4	20	\bar{G}_3	A10	36	61	A11
\bar{CS}_3	5	21	\bar{G}_0	A13	37	60	A12
I/O 30	6	22	I/O 31	I/O 27	38	59	A14
I/O 28	7	23	I/O 29	I/O 25	39	58	I/O 24
\bar{W}_0	8	24	GND	V _{CC}	40	57	I/O 26
\bar{W}_2	9	25	V _{CC}	GND	41	56	I/O 10
I/O 12	10	26	I/O 13	I/O 9	42	55	I/O 8
I/O 14	11	27	I/O 15	I/O 11	43	54	A0
\bar{CS}_1	12	28	\bar{G}_2	A1	44	53	A2
\bar{CS}_2	13	29	\bar{G}_1	A3	45	52	A4
I/O 22	14	30	I/O 23	A5	46	51	A6
I/O 20	15	31	I/O 21	I/O 17	47	50	I/O 16
N/C	16	32	\bar{W}_1	I/O 19	48	49	I/O 18

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