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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Military 46206

Product Preview

32K x 32 Bit Fast SRAM Module

MPO
SRAM MODULE

The 46206 is a 1,048,576 bit static random access memory organized as 32,768 words of 32 bits. The module is constructed using four 6206 (32K x 8) static RAM's in leadless carriers mounted in either a multilayer sidebraze DIL or a double sided multilayer Polyimide substrate.

The 6206 is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using Motorola's third-generation high-performance silicon-gate CMOS (HCMOS IV) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after E goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as E remains high. This feature provides significant system-level power savings. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 20 ns (6206-35).

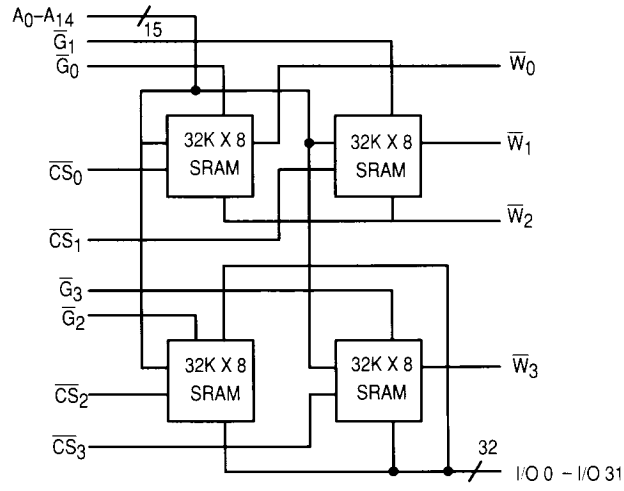
The 46206 is equipped with output enables ($\overline{G}_0$-$\overline{G}_3$) and four separate byte enables ($\overline{CS}_0$-$\overline{CS}_3$) inputs, allowing for greater system flexibility. The ($\overline{G}$) input, when high will force the output to a high impedance.

AVAILABLE AS
1) JAN: N/A
2) SMD: N/A
3) 883C: Planned
X = CASE OUTLINE AS FOLLOWS:
PACKAGE: DIL: 46206-35/BXAJC
PGA: 46206-35/BZAJC

XX = Speed in ns (35, 45, 55, 70)

- High Density 1.0 Megabit SRAM (32K x 32) Module
- High Speed CMOS SRAMs
- Fast Access Time — Military 35 ns (max)
- Available in: 64 pin, 600 mil x 3.2 inch DIL Sidebraze
  64 pin PGA — 1.0 inch x 1.6 inches
  (2.9 square inches of board space)
- Individual Byte Wide Select
- Fully TTL Compatible
- Single 5.0 V (± 10%) Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Two Module Controls: $\overline{CS}$ for Automatic Power Down
  $\overline{G}$ for Fast Access to Data
- Three State Outputs

BLOCK DIAGRAM



PIN NAMES and FUNCTION	
A_0-A_{14}	Address Inputs
$\overline{W}_0$-$\overline{W}_3$	Write Enable
$\overline{CS}_0$-$\overline{CS}_3$	Byte Enable
$\overline{G}_0$-$\overline{G}_3$	Output Enable
I/O_0-I/O_3	Data I/O
V_{CC}	+ 5.0 V Power Supply
GND	Ground

All power supply and ground pins must be connected for proper operation of the device.

TRUTH TABLE					
$\overline{CS}$	$\overline{G}$	$\overline{W}$	Mode	Supply	I/O Pin
H	X	X	Not Selected	I_{SB}	High-Z
L	H	H	Output Disable	I_{CC}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	X	L	Write	I_{CC}	D_{IN}

X = Don't Care

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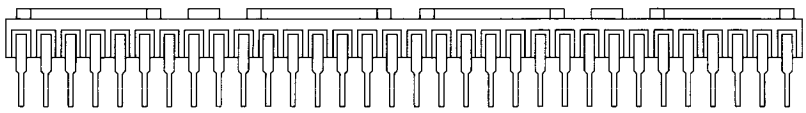
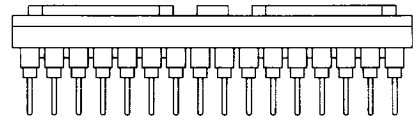
PIN ASSIGNMENTS

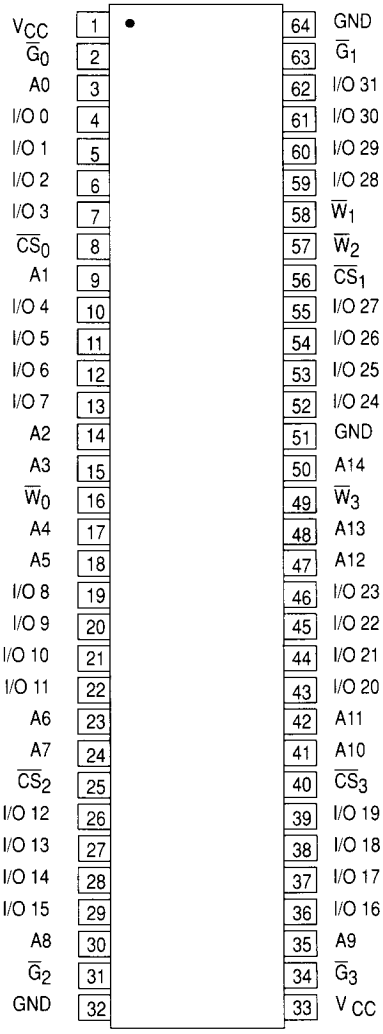
DIL SIDEBRAZE



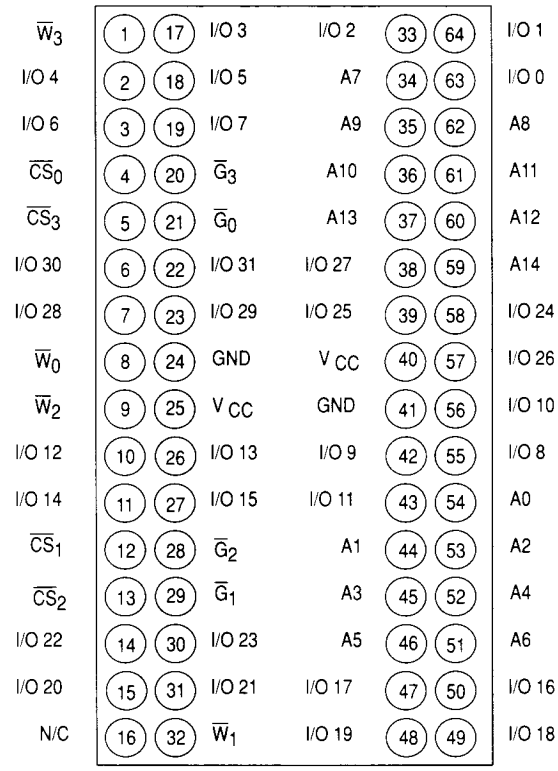
PGA



DIL



PGA



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